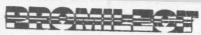
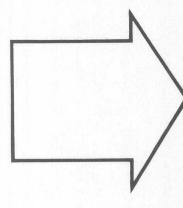
LSI Databook



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LSI DATABOOK

Introduction

This book has been prepared to give the user a concise list of all LSI Products offered by Monolithic Memories. It is divided by products into sections on Military Products Division, PROMs, PLETM devices, PAL® devices, HAL®/ZHAL devices, System Building Blocks/HMSITM, FIFOs, Memory Support, Arithmetic Elements and Logic, Multipliers, 8-Bit Interface, Double-Density PLUS Interface, (CMOS products included), Logic Cell Array, ECL10KH products and a General Information Section which has definition of Terms and Waveforms. Each section has been designed to allow the user the most useable format for the products described. Cross reference and selection guides are given where applicable. FIFO, PAL devices, System Building Blocks/HMSITM, Multipliers, 8-Bit Interface, Double-Density PLUS Interface and ECL10KH data sheets are shown in detail for each product. Advance Information Sheets are included to inform you of soon-to-be released products. This LSI databook was formatted with you, the user, in mind.

For more information, contact the local Monolithic Memories sales representative or franchised distributor. In section 19 of this book Monolithic Memories Sales Reps and Franchised Distributors are listed, for your convenience.

Products listed in the Advance Information section were due for imminent release at the time of printing. Please contact Monolithic Memories for current availability and full parametric specifications.

Prices

All prices are in U.S. dollars and are subject to change without notice.

Terms

70%/30 days, 30%/45 days from date of invoice, FOB Sunnyvale, California.

Minimum Order Requirements

For all orders placed in the factory there is a minimum order requirement of \$1000 (\$100 per line item) except for the

HAL® Circuits—A Non-Recurring Engineering (NRE) charge is made to cover mask and test vector generation. This charge may be amortized over the initial production commitment. Minimum production commitments and NRE charges are

	NRE	MIN. ANNUAL QTY	MIN. QTY PER DELY
20 and 24 pin HAL devices:			
Combinatorial patterns	\$2.5K	5,000 pcs	2,000 pcs
Sequential patterns	\$2750	5,000 pcs	2,000 pcs
ZHAL™20/20A/24A MegaHAL™:	\$4K	5,000 pcs	2,500 pcs
HAL32R16	\$5K	2,500 pcs	500 pcs
ZHAL64R32	\$5K	1,000 pcs	200 pcs

ProPAL™ Circuits - ProPAL circuits are programmed PAL devices which are functionally tested by Monolithic Memories prior to shipment. The NRE charge covers setup and test vector generation costs and may be amortized over the initial production commitment quantities. A nominal per unit programming and testing charge is also made and varies according to device type. NREs and minimum order requirements for ProPAL circuits are as follows:

	NRE	MIN. ANNUAL QTY	MIN. QTY PER DELY
20 and 24 pin devices:			
Combinatorial patterns	\$500	2,500 pcs	500 pcs
Sequential patterns MegaPAL™:	\$750	2,500 pcs	500 pcs
PAL32R16	\$1K	1,000 pcs	200 pcs
PAL64R32	\$1K	500 pcs	100 pcs

Unless otherwise specified, the standard packages are "J" or "N" packages. In some instances the "D" package is the only package available. Other non-standard packages and military Level 883B devices not listed may be available. Contact a sales representative of Monolithic Memories, Non-standard

devices are considered nonreturnable by distribution to

Monolithic Memories. In-House PROM Programming Guidelines

1) Minimum Order Size.

1/4K-8K 5K pcs/yr/pattern 500 pcs/shipment

16K-32K 2.5K pcs/yr/pattern

250 pcs/shipment

- 2) Lead Time: Initial code acceptance six weeks. Standard lead time plus two weeks after code acceptance.
- 3) Cancellations: 60 Days
- 4) Schedule Change: 30 Days
- 5) Price Adder:

A nominal per unit programming and testing charge is made and varies according to device type. Price includes ink marking with customer pattern number.

6) Inputs: Truth Table, Paper Tape, Disk, Master; a combination of two inputs are required. If only one input is supplied, a sample lot must be signed off by the customer.

Commercial/Industrial/Military Codes

The letter codes "C," "I," and "M" are used to denote commercial, industrial, and military device limits as follows:

Commercial $-T_A = 0$ °C to +75°C $V_{CC} = 5V \pm 5\%$ Industrial $-T_A = -40$ °C to +85°C $V_{CC} = 5V \pm 10\%$ Military $-T_A = -55^{\circ}C$ to $+125^{\circ}C$ $V_{CC} = 5V \pm 10\%$

Package Codes

All devices ordered must include a package code as a suffix to the part number. The package code definitions are shown below.

PACKAGE	bragging in a fa
CODE	DESCRIPTION
J	Ceramic dual-in-line
JS	Ceramic dual-in-line
	SKINNYDIP®
N	Plastic dual-in-line
NS	Plastic dual-in-line
	SKINNYDIP®
NL	Molded leaded chip carrier
D	Side brazed ceramic dual-in-line
F	Flat Pack—Bottom Brazed
L	Leadless—Ceramic chip carrier
T	Inverted "D" package
P seven	Pin Grid Array
W	Cerpack

See "Part Numbering Systems" for complete part descriptions.

DIP Package Width Configuration

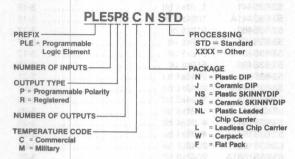
	300 mil	600 mil	900 mil
16, 18, 20 pin	N, J		
24 pin	NS, JS	N, J	
28, 40, 48, 52 pin		N, J	
64 pin			D

Screening Options

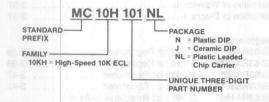
PROCESS LEVEL	PART MARKING
MIL-STD-883	
Method 5004 and 5005	883B
Level B	(Suffix)

TOTA BD days 300 A65 days from date of Invoice, FO ... **Programmable Array Logic Circuits** Minimum Order Regularine its PAL 16 L 8 B -4 C N STD H01234 0 000 ft of the manufacture of the contraction of the cont STO VICE IS SHOULD BE SEE FAMILY TYPE PAL = Programmable Array Logic
PAL10H = ECL 10KH Programmable Array Logic HAL = Hard Array Logic it is the amortised over the in ZHAL = Zero-power Hard Array Logic NUMBER OF ARRAY INPUTS OUTPUT CELL O COME TO OUTPUT CELL O CAN SO C H = Active High 100 = Complementary = Programmable Polarity RP = Registered Programmable Polarity = Shared S RS = Registered Shared ang 040,3 X = Exclusive-OR A = Arithmetic VX = Varied Exclusive-OR 310 OUD, 7 ECONO DECIS RA = Registered Asynchronous Package Codes office a as obcit agentos NUMBER OF OUTPUTS-SPEED Blank = Standard Α = High Speed = Very High Speed В D = Ultra High Speed ad v. m POWER -Blank = Standard = 1/2 Power cocording to device type, NREE c. J. no. no. = 1/4 Power -4 monte for Profit dargers are are a larger **OPERATING CONDITIONS** C = Commercial 1.3% M = Military PACKAGE N = Plastic DIP J = Ceramic DIP NS = Plastic SKINNYDIP JS = Ceramic SKINNYDIP NL = Plastic Leaded Chip Carrier = Pin Grid Array 200 000 = Leadless Chip Carrier 800 008 and their casts had etalomo Wint Cerpack vol prefredment the 9" de 3. F = Flat Pack PROCESSING T STD = Standard to "1" and degrations to start the "1" or XXXX = Other in some instances like "D" declarate file only BIT PATTERN NUMBER -

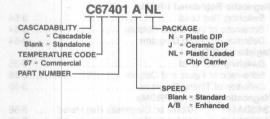
PLE™ Programmable Logic Element



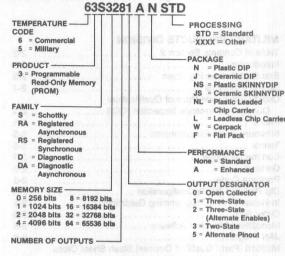
ECL 10KH Logic



FIFOs



High Performance PROMs



Memory Support/Arithmetic/ HSMI/ Double-Density PLUS™ Interface

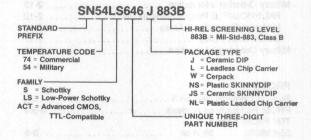


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Monolithic Memories

Terms and Conditions of Sale

General Provisions

- 1. ACCEPTANCE THE TERMS OF SALE CONTAINED HEREIN APPLY TO ALL QUOTATIONS MADE AND PURCHASE ORDERS ENTERED INTO BY THE SELLER. SOME OF THE TERMS SET OUT HERE MAY DIFFER FROM THOSE IN BUYER'S PURCHASE ORDER AND SOME MAY BE NEW. THIS ACCEPTANCE IS CONDITIONAL ON BUYER'S ASSENT TO THE TERMS SET OUT HERE IN LIEU OF THOSE IN BUYER'S PURCHASE ORDER. SELLER'S FAILURE TO OBJECT TO PROVISIONS CONTAINED IN ANY COMMUNICATION FROM BUYER SHALL NOT BE DEEMED A WAIVER OF THE PROVISIONS OF THIS ACCEPTANCE. ANY CHANGES IN THE TERMS CONTAINED HEREIN MUST SPECIFICALLY BE AGREED TO IN WRITING BUY AN OFFICER OF THE SELLER BEFORE BECOMING BINDING ON EITHER THE SELLER OR THE BUYER. All orders or contracts must be approved and accepted by the Seller at its home office. These terms shall be applicable whether or not they are attached to or enclosed with the products to be sold hereunder.
- 2. TAXES Unless otherwise specifically provided herein, the amount of any present or future sales, revenue, excise or other tax applicable to the products covered by this order or the manufacture of sale thereof, shall be added to the purchase price and shall be paid by the Buyer, or in lieu thereof the Buyer shall provide the Seller with a tax exemption certificate acceptable to the taxing authorities. In the event Seller is required to pay any such tax, fee, or charge, at the time of sale or thereafter, the Buyer shall reimburse Seller therefore.
- 3. RELEASE Prices apply only if the quantity hereunder is released within twelve (12) months and shipments scheduled no more than eighteen (18) months from the date of Seller's receipt of Buyer's order; otherwise, Seller's standard prices in effect at the time of release date shall apply to the quantity shipped, and Buyer shall be invoiced for the difference in price, if any.
- 4. FOB POINT Shipments of goods within and outside the U.S. shall be delivered FOB Seller's plant, and title and liability for loss or damage thereto shall pass to Buyer upon Seller's tender of delivery of the goods to a carrier for shipment to Buyer, and any loss or damage thereafter shall not relieve Buyer of any obligation hereunder. Buyer shall reimburse Seller for taxes and any other expenses incurred or licenses or clearance required at port of entry and destination. Seller may deliver the goods in installments. Unless otherwise agreed, all items shall be packaged and packed in accordance with Seller's normal practices.
- 5. DELIVERY All shipping dates are estimates only and are dependent upon prompt receipt of all necessary information from Buyer. Shipments may be made in installments. Seller shall be excused from performance and shall not be liable for any delay in delivery or for nondelivery, in whole or in part, caused by the occurrence of any contingency beyond the reasonable control of Seller, including but not limited to, war (whether or not an actual declaration thereof is made), sabotage, insurrection, riot or other act of civil disobedience, act of a public enemy, failure or delay in transportation, act of any government or any agency or subdivision thereof affecting the terms of this contract or otherwise, judicial action, labor dispute, accident, defaults of suppliers, fire, explosion, flood, storm or other acts of God, shortage of labor, fuel, raw material or machinery or technical or yield failures where Seller has exercised ordinary care in the prevention thereof. If any such contingency occurs, Seller may at its sole discretion allocate production and delivery among Seller's customers.
- 6. PAYMENT TERMS (a) Unless otherwise agreed, payment terms are 70% thirty (30) days; 30% forty-five (45) days after date of invoice. No discounts are authorized. Shipments, deliveries, and performance of work shall at all times be subject to the approval of the Seller's credit department and the Seller may at any time decline to make any shipments or deliveries or perform any work except upon receipt of payment or upon terms and condition or security satisfactory to such department.
- (b) If in the judgment of the Seller, the financial condition of the Buyer at any time does not justify continuation of production or shipment on the terms of payment originally specified, the Seller may require full or partial payment in advance and, in the event of the bankruptcy or insolvency of the Buyer or in the event any proceeding is brought by or against the Buyer under the bankruptcy or insolvency laws, the Seller shall be entitled to cancel any order then outstanding and shall receive relimbursement for its cancellation charges.
- (c) Each shipment shall be considered a separate and independent transaction, and payment therefore shall be made accordingly. If shipments are delayed by the Buyer, payments shall become due on the date when the Seller is prepared to make shipment. If the work covered by the purchase order is delayed by the Buyer, payments shall be made based on the purchase price and the percentage of completion. Products held for the Buyer shall be at the risk and expense of the Buyer.

- 7. INSPECTION Unless otherwise specified and agreed upon, the material to be furnished under this order shall be subject to the Seller's standard inspection at the place of manufacture. If it has been agreed upon and specified in this order that Buyer is to inspect or provide for inspection at place of manufacture such inspection shall be so conducted as to not interfere unreasonably with Seller's operations and consequent approval or rejection shall be made before shipment of the materials. Notwithstanding the foregoing, if, upon receipt of such material by Buyer, the same shall appear not to conform to the contract, the Buyer shall immediately notify the Seller of such conditions and afford the Seller a reasonable opportunity to inspect the material. No material shall be returned without Seller's consent. Seller's Return Material Authorization form must accompany such returned material.
- 8. LIMITED WARRANTY AND LIMITED REMEDY The Seller warrants that the products to be delivered under this purchase order will be free from defects in material and workmanship under normal use and service. Seller's obligations under this Warranty are limited to replacing or repairing or giving credit for, at its option, at its factory, any of said products which shall, within one (1) year after shipment, be returned to the Seller's factory of origin, transportation charges prepaid, and which are, after examination, disclosed to the Seller's satisfaction to be thus defective. THIS WARRANTY IS EXPRESSED IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, STATUTORY OR IMPLIED, INCLUDING THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE, AND OF ALL OTHER OBLIGATIONS OR LIABILITIES ON THE SELLER'S PART, AND IT NEITHER ASSUMES NOR AUTHORIZES ANY OTHER PERSON TO ASSUME FOR THE SELLER ANY OTHER LIABILITIES IN CONNECTION WITH THE SALE OF THE SAID ARTICLES. This Warranty shall not apply to any of such products which has liable vabeen repaired or altered, except by the Seller, or which shall have been repaired or engligence, or accident. The aforementioned provisions do not extend the original warranty period of any product which has either been repaired or replaced by Seller.

It is understood that if this order calls for the delivery of semiconductor devices which are not furnished and fully encapsulated, that no warranty, statutory, expressed or implied, including the implied warranty of merchantability and fitness for a particular purpose, shall apply. All such devices are sold as-is, where-is.

- 9. PATENT INDEMNIFICATION Buyer shall hold Seller harmless from and defend Seller against any cost, expenses, damages or liabilities arising from Seller's compliance with Buyer's designs or specifications. Except as set forth above, the Seller agrees to protect and hold harmless the Buyer from any and all claims demands, proceedings, actions, liabilities and costs resulting from any alleged infringement of patents in the United States owned by third parties by Products purchased by Buyer from Seller, provided the Buyer gives to Seller prompt notice of any such claim made against the Buyer and authorizes the Seller to settle or defend any such claim, demand, proceeding or action and assists the Seller in so doing (at the Seller's expense) upon request by the Seller. Should, as a result of any such claim, demand, proceeding or action, the Buyer be enjoined from selling or using the product, the Seller shall either (1) procure for the Buyer the right to use or sell the product; (2) modify the product so that it becomes noninfringing; (3) upon return of the product provide to the Buyer a noninfringing product meeting the same functional specifications as the product; or (4) authorize the return of the product to the Seller and upon its receipt refund to the Buyer the cost of the product plus transportation charges. The foregoing states the entire liability of the Seller for infringement of the patents of third parties and, in particular, the Seller has no obligation to indemnify the buyer for infringement of patents resulting from combinations of the product with other products whether or not supplied by the Seller.
 THIS PROVISION IS STATED IN LIEU OF ANY OTHER EXPRESSED. IMPLIED. OR STATUTORY WARRANTY AGAINST INFRINGEMENT AND SHALL BE THE SOLE AND EXCLUSIVE REMEDY FOR PATENT INFRINGEMENT OF ANY
- 10. DAMAGE LIMITATION INDEPENDENTLY OF ANY OTHER LIMITATION HEREOF AND REGARDLESS OF WHETHER THE PURPOSE OF SUCH LIMITATION IS SERVED, IT IS AGREED THAT IN NO EVENT SHALL SELLER BE LIABLE FOR SPECIAL, INCIDENTAL OR CONSEQUENTIAL DAMAGES OF ANY KIND UNDER THIS ORDER.
- 11. SALE CONVEYS NO LICENSE Seller's products are offered for sale and are sold by Seller subject in every case to the condition that such sale does not convey any license, expressly or by implication, estoppel or otherwise, under any patent claim with respect to which Seller can grant licenses covering a completed equipment, or any assembly, circuit, combination, method or process in which any such products are used as components (notwithstanding the fact that such products may have been designed for use in or may only be useful in, such patented

Monolithic Memories

Terms and Conditions of Sale

General Provisions

equipment, assembly, circuit, combination, method or process and that such products may have been purchased and sold for such use). Seller expressly reserves all lits rights under such patent claims.

- 12. RETURNS AND ADJUSTMENTS Products may only be returned with prior written approval of Seller. Adjustments for defective products are subject to Seller's concurrence that the alleged defects exist, to Seller's satisfaction, after suitable inspection and test by Seller. Adjustments may include credit or replacement at the option of the Seller.
- 13. TERMINATION AND CANCELLATION (a) Buyer may terminate this contract in whole or, from time to time, in part upon written notice to Seller. In such event Buyer shall be liable for termination charges which shall include a price adjustment based on the quantity of goods actually delivered, and all costs, direct and indirect, incurred and committed for this contract together with a reasonable allowance for prorated expenses and anticipated profits.
- (b) Unless otherwise specified on the face hereof, all quantities must be released no more than twelve (12) months and shipments scheduled no more than eighteen (18) months from the date of Seller's receipt of Buyer's order, otherwise this contract may be cancelled by Seller and Buyer shall be liable for termination charges as provided herein.
- 14. NONWAIVER OF DEFAULT In the event of any default by Buyer, Seller may decline to make further shipments. If Seller elects to continue to make shipments, Seller's action shall not constitute remedies for any such default.
- 15. APPLICABLE LAW The validity, performance and construction of this contract shall be governed by the laws of the State of California.
- 16. U.S. GOVERNMENT CONTRACTS If Buyer's original purchase order indicates by contract number, that it is placed under a government contract, only the following provisions of the current Federal Acquisition Regulations are applicable in accordance with the terms thereof, with an appropriate substitution of parties, as the case may be—i.e., "Contracting Officer" shall mean "Buyer," "Contractor" shall mean "Buyer," "Contractor" shall mean this order.
- 52.202-1. Definitions: 52.232-11, Extras; 52.212-9, Variation in Quantity; 52.232-23, Assignment of Claims; 52.228-2, Additional Bond Security; 52.225-11, Certain Communist Areas; 52.222-4, Contract Work Hours and Safety Standards Act —Overtime Compensation; 52.222-20, Walsh-Healy Public Contracts Act; 52.22-25, Equal Opportunity; Officials Not to Benefit; 52.203-5, Covenant Against Contin-

- gent Fees; 52.249-1, Termination for Convenience of the Government (Fixed Price) (Short Form) (only to the extent that Buyer's contract is terminated for the convenience of the government); 52.2-1, Contractor Inspection Requirements; 52.227-1, Authorization and Consent; 52.227-2, Notice and Assistance Regarding Patent and Copyright Information; 52.247-1, Commercial Bills of Lading Notations; 52.223-35, Affirmative Action for Special Disabled and Vietnam Era Veterans; 52.222-1, Notice to the Government of Labor Disputes; 52.215-1, Examination of Records by Comptroller General; 52.220-3, Utilization of Labor Surplus Area Concerns.
- 17. ASSIGNMENT This contract shall be binding upon and inure to the benefit of the parties and the successors and assigns of the entire business and good will of either Seller or Buyer, or of that part of the business of either used in the performance of this contract, but shall not be otherwise assignable.
- 18. MODIFICATION This contract constitutes the entire agreement between the parties relating to the sale of goods described on the face hereof, and no addition to or modification of any provision upon the face or reverse of this contract shall be binding upon Seller unless made in writing and signed by a duly authorized representative of Seller located in Santa Clara, California. Buyer hereby acknowledges that he has not entered into this agreement in reliance upon any warranty or representation by any person or entity except for the warranties or representations specifically set forth herein.
- 19. GENERAL The Seller represents that with respect to the production of the articles and/or the performance of the services covered by this order, it will fully comply with all requirements of the Fair Labor Standards Act of 1938, as amended.
- 20. PROPERTY RIGHTS AND TOOLING The design, development or manufacture by Seller of a product for a specific customer shall not be deemed to produce a work made for hire and shall not give to the customer any copyright interest in the product or any interest in all or any portion of the mask works relating to the product. All such rights shall remain the property of Seller. Notwithstanding the foregoing, Seller will provide a custom product (e.g., personalized gate array, cell library or full custom) utilizing a logic design supplied by a customer exclusively to that customer absent written agreement to the contrary with the customer.
- 21. VARIATION IN QUANTITY If this order calls for a product not listed in Seler's current catalog, or for a product which is specially programmed for Buyer, it is agreed that Seller may ship a quantity which is five percent (5%) more or less than the ordered quantity and that such quantity shipped will be accepted and paid for in full satisfaction of each party's obligation hereunder for the quantity ordered.

Quality System

The quality system at Monolithic Memories is based on MIL-Q-9858, "Quality Program Requirements," MIL-I-45208, "Inspection System Requirements," and MIL-M-38510, Appendix A, "Product Assurance Program." Mil-M-38510 plays a significant role in structuring Monolithic Memories' Quality Program as specified herein.

Monolithic Memories has facilities certified by DESC, Defense Electronics Supply Center, to qualify and manufacture Class B Schottky Bipolar PROMS and Programmable Array Logic devices, in accordance with the requirements of MIL-M-38510. This certification included a successful audit of our quality system to the stringent requirements of Appendix A of MIL-M-38510 which defines a Product Assurance Program tailored for integrated circuit manufacturers by DESC. This same quality system has also met the strict requirements of both "controlled" and "captive" line programs connected with our special Hi-Rel programs.

The quality accent at Monolithic Memories is on process control as reflected in the use of many monitors and audits rather than gate inspection. This philosophy is consistent with building in quality and reliability rather than attempting to screen for it

Process Control

Monolithic Memories manufacturing process uses advanced techniques to reduce random defects and produce consistent optimum quality. Typical techniques employed are:

- · Redundant Masking
- Pellicalized Masks
- · Direct Step on Wafer Processing

These processes although more costly, result in significant quality and reliability improvements. During the initial production stages of new designs and periodically thereafter, engineering characterizes the design process compatibility by careful sample selection of lots reflecting process variable extremes.

Product Reliability Programs

Monolithic Memories has an ongoing reliability program for military and commercial products, each utilizing the appropriate test methods of MIL-STD-883. This program provides for a consistent database in the following areas:

- Product/Process Reliability Data
- Qualification of Raw Materials

- Customer Quality Conformance
- Reliability verification of state of the art design and production techniques.

Quality Monitors

MMI constantly monitors product quality and reliability through the following ongoing programs:

- Reliability assessments of all products, processes and packages.
- Inprocess and Final product quality measurements.
- Process and product quality feedback at all key manufacturing points.
- Positive corrective action and verification.

Screening

Much of the assembly and processing is performed offshore at facilities owned by or qualified by MMI. These facilities are routinely monitored by Monolithic Memories personnel to our quality system requirements.

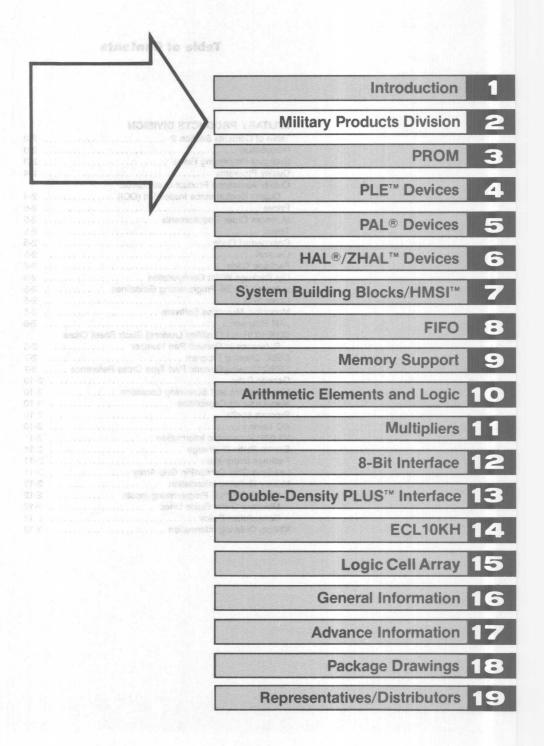
Standard Commercial product receives the following screens and monitors to insure the highest possible quality.

- Constant Acceleration confirm the AQL levels are met
- Fine and Gross Leak or exceeded.
- Final Electrical Test
- Visual and Mechanical Inspection

The standard product AQL levels which Monolithic Memories guarantees are listed in the table on this page.

Quality Assurance (AQL) Levels

TEST	AQL TEMPERANCE	
Hermeticity (includes fine and gross) Electrical	.1	
DC at 25°C	.065	
Functional at 25°C	.065	
AC at 25°C	.25	
DC at Temperature Extremes	.25	
Functional at Temperature Extremes	.25	
AC at Temperature Extremes	.25	



MILITARY PRODUCTS DIVISION

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Introduction

In August, 1982 Monolithic Memories Inc. formed a Military Products Division. Although Monolithic Memories has participated in the defense market for some time, we feel that by focusing on this very demanding customer base with a totally dedicated resource, we can provide aerospace and military systems manufacturers with a new industry standard of service and responsiveness.

Monolithic Memories offers devices to a full complement of military screening levels:

Monolithic Memories Inc. Level S
JAN 38510 Class B
DESC Drawing Program
Mil-Std-883 Class B
Monolithic Memories Inc Mil-Temp Product

In addition, we welcome the opportunity to review and quote to customer source control drawings. Our spec Review group is measured to a 2 week turn-around time on drawing reviews, so our customers will receive a timely response on our ability to meet custom requirements.

Monolithic Memories is Certified by the Defense Electronics Supply Center to assemble and test JAN 38510 Class B devices at its Sunnyvale, California.

Offshore Assembly facilities for Mil-Std-883 Class B devices are located in Penang, Malaysia.

Standard Processing Flows

Monolithic Memories Processing and Screening flows are organized to provide a broad selection of processing options, structured around the most commonly requested customer flows.

Standard processing flows which the Military Products Division currently operates to include:

Monolithic Memories Inc. Modified Level S
JAN 38510 Class B
DESC Drawing Program
Mil-Std-883 Class B
Monolithic Memories Inc. Mil-Temp Product

In addition, these flows are expanded to provide for factory programming on PAL circuits and PROMS, when required by our customers.

Major benefits can be realized by ordering product to standard flows whenever possible:

- Minimize need for source control drawings.
- Cost savings on unit cost no price adders for custom processing.
- Improved lead time no spec review or negotiation time, plus the ability to pull product from various work-in-process stages or purchase product from finished goods inventory.

It is the policy of Monolithic Memories to always operate to the most current revision of Mil-Std-883.



Quality Programs

The Military Product Division quality system conforms to the following Mil-Standards:

Mil-M-38510, Appendix A, "Product Assurance Program" Mil-Q-9858, "Quality Program Requirements" Mil-I-45208, "Inspection System Requirements"

Monolithic Memories facilities in Sunnyvale are certified by the Defense Electronics Supply Center (DESC), to manufacture and qualify Schottky Bipolar PROMs and PAL circuits in accordance with Mil-M-38510 Class B. This certification was a result of a successful audit of our production and quality systems to the stringent requirements of Mil-M-38510. Monolithic Memories has also demonstrated compliance with the strict requirements of both controlled and captive lines connected with special Military programs.

Quality Assurance

Following 100% screening, the Military Products Division samples all products processed in conformance with MIL-STD-883 Class B to the following LTPD levels:

Test	LTPD
DC 25°C	a use to be no 2 mil
DC +125°C	2013 Maria no econo 3 de
DC -55° C	5
Functional at 25°C	2
Functional at Temperature E	xtremes 5
AC 25°C	2
AC +125°C	to bond san and 73
AC -55°C	5

The Military Products Division ensures outgoing product quality and integrity by performing inspection Lot Group A's and B's per Mil-Std-883 Method 5005, conducting self audits in all areas involved in screening tests per Method 5004 of Mil-Std-883, gating all shipments to our customers, and maintaining a calibration control system in accordance with Mil-Std-45662.

For products requiring programming prior to AC tests, testing is performed utilizing MIL-M-38510 Slash Sheet sample plans.

Product Qualification/ Quality Conformance Inspection (QCI)

The Military Products Division has a quality conformance testing program in accordance with Mil-Std-883, Method 5005.

Quality Conformance Testing provides necessary feedback and monitors several areas:

- Reliability of Product/Processes
- Vendor Qualification for Raw Materials
- Customer Quality Requirements
- Maintain Product Qualification
- Engineering Monitor on Products/Processes

Standard procedures for new product release specify that Monolithic Memories' Reliability Department, as a minimum, conduct full qualification testing per Method 5005 of Mil-Std-883. Once qualified, each package type (from each assembly line) and device (by technology group as delineated in Mil-M-38510) are incorporated into Monolithic Memories Quality Conformance Inspection program which utilizes the requirements of Mil-M-38510.

When Military Programs do not require that QCI data be run on the specific lot shipped, Monolithic Memories Quality Conformance program allows customers to obtain generic data on all product families manufactured by the Military Products Division. Generic Qualification Data enables customers to eliminate costly qualification and descruct unit charges, and also improves delivery time by a factor of eight to ten weeks. The following generic data is available:

Group B—Package related tests

- QCI is performed every 6 weeks of manufacture on each package type.
- Any device type in the same package type may be used regardless of the specific part number.
- Purpose: To monitor assembly integrity.

Group C-Product/Process related tests

- QCI is performed every 13 weeks of manufacture, on representative devices from the same microcircuit group.
- · Life test data may be used to qualify similar technologies.
- Purpose: To monitor the reliability of the process and parametric performance for each product technology.

2

Prices

All prices are in U.S. dollars and are subject to change without notice.

Minimum Order Requirements

For all orders placed in the factory there is a minimum order requirement of \$1000 (\$250 per line item) except for the following:

HAL* Circuits—The \$3-4K N.R.E. and mask charge can be amortized over the initial production commitment. The minimum initial production commitment is 5K units within one year; the minimum quantity per line item release is 2K.

ProPAL Circuits—When purchased, the initial phase of HAL Circuit, there is no additional N.R.E. and there is a nominal adder for programming and testing. The minimum quantity per release is 500 units. When purchased without a follow-on the \$1-2K N.R.E. can be amortized over a minimum initial production commitment of \$2500 units.

There will be a minimum of \$250 and \$50 per line item for drop-ship orders.

Terms

70%/30 days, 30%/45 days from date of invoice, FOB Sunnyvale, California.

Commercial Code

The letter code "C" is used to denote commercial device limits as follows:

Commercial—TA = 0° C to + 75°C VCC = 5 V $\pm 5\%$

General

Unless otherwise specified the standard packages are "J" or "N" packages. In some instances the "D" package is the only package available. Other non-standard packages may be available. Contact a sales representative of Monolithic Memories. Non-standard devices are considered nonreturnable by distribution to Monolithic Memories.

Package Codes

All devices ordered must include a package code as a suffix to the part number. The package code definitions are shown below.

PACKAGE

DESCRIPTION

J Ceramic dual-in-line*
JS Ceramic dual-in-line*
N Plastic dual-in-line*
NS Plastic dual-in-line*

NL Molded Leadless Chip Carrier

Dip Package Width Configuration

4	300 mil	600 mi
20 pin	N, J	-
24 pin	NS, JS	N, J

In-House PROM Programming Guidelines

1) Minimum Order Size:

1/4K-8K 5K pcs/yr/pattern 500 pcs/shipment 16K-32K 2.5K pcs/yr/pattern

250 pcs/shipment

2) Lead Time: Initial code acceptance—six weeks.

Standard lead time plus weeks after code acceptance.

3) Cancellations: 60 Days

4) Schedule Change: 30 Days

5) Price Adder:

Price includes ink marking with customer pattern number.

6) Inputs: Truth Tape

Paper Tape Disk Master

A combination of two inputs are required.

If only one input is supplied, a sample lot must be signed off by the customer.

Order Size

DENSITY	MIN-10K	10K-25K	25K +
1/4-2K	50¢	40¢	30¢
4K-8K	60¢	50¢	40¢
16K-32K REG/DIAG	85¢	70¢	55¢

Monolithic Memories Software

SYSTEM	PALASM 2 OBJECT	PALASM 2 SOURCE	
	\$200	\$500	
DEC VAC VMS MT	PAL2-VMSE-MT	PAL2-VMSS-MT	
IBM PC (DOS) 5D	PAL2-IPCE-5D	PAL2-IPCS-5D	
ASCII MT		PAL2-ASCS-NJ	

^{*}See "Part Numbering Systems" for complete part descriptions.



JAN Program

Monolithic Memories is certified by the Defense Electronics Supply Center to fabricate wafers in our 4-inch fab lines and to assemble and test MIL-M-38510 Class B PROMs and PAL circuits in our Sunnyvale facilities. Monolithic Memories has, in addition, been awarded full laboratory suitability to conduct all qualification and conformance testing in accordance with MIL-STD-883, Method 5005.

Selected devices will be further qualified in leadless chip carriers.

Long term QPL I plans include FIFO's Double-Density PLUS Interface, New PAL Families as they are introduced, and Registered/Standard PROMs.

Our goal in the Military Products Division is to support the JAN38510 Program with a continual flow of new high-performance, Advanced Technology Products.

Monolithic Memories Products for which slash sheet specifications currently exist are listed in the "M38510 Slash Sheet Cross Reference to Generic Part Number."

Listings are based on QPL-38510-65, dated October 1985 M38510 (Part I Qualified Devices) Slash Sheet Cross Reference to Generic Part Number

M38510	01	02	03	04	05	06	07	08	09	10
				with the line	90	ergial david	mmop ethi	uses to des	al 'O' she	o nollelium
206		53S441						15 200		
209	AGS-	10:	- MINI	THEMSO				53S841	6 = JOV	
503	10H8	12H6	14H4	- MZ-2/		10L8	12L6	14L4		
504	16L8A	16R8A	16R6A	16R4A						revenue

Near future QPL I plans include:

PAL16L8A-2

PAL16R8A-2

PAL16R6A-2

PAL16R4A-2

PAL20L8A

PAL20R8A

PAL20R6A

PAL20R4A



DESC Drawing Program

Monolithic Memories is an active participant in the DESC Drawing Program. For contracts invoking MIL-STD-454 we offer our full PAL product line to DESC Drawings 81035 and 81036. Monolithic Memories is also approved to supply the 32K PROM to DESC Drawing 82008. The idea behind the DESC Drawing Program is to standardize MIL-STD-883B microcircuits where fully qualified JAN product is not available. The advantage to the user is that DESC Drawings are a cost effective alternative to source control drawings and are offered as off-the-shelf stocking items by IC manufacturers participating in the program.

Since semiconductor demand is on the rise, and lead times will be a major concern, DESC Drawings should always be considered to improve availability over source control draw-

ings. It is standard practice at Monolithic Memories to convert our 883B processing to DESC Drawings for all products which we are approved to supply. Monolithic Memories Inc., then dual marks devices with both the DESC Drawing Number and the Generic Part Number. DESC approved products can then be procured to either part number as standard product through both OEM and distributor channels.

The following cross reference will allow you to determine the appropriate DESC Drawing part numbers for each PAL product and the 32K PROM. Future DESC print activity will include new PAL products and registered PROMs. Monolithic Memories will work with DESC to continually generate new drawings, which will provide a steady flow of advanced technology products to standardized specifications.

DESC Drawing/Generic Part Type Cross Reference

DESC DRAWING PART NO.: 81035	01 SEASEN	S-ACRECIAGE R S-ACRECIAGE	X*undore
DRAWING	DEVICE TYPE	CASE OUTLINE	LEAD FINISH

PAL DEVICES

DESC DRAWING	GENERIC PART NUMBER	REPLACEMENT JAN SPECIFICATION PART NUMBER	
8103501RA*	PAL10H8MJ883B	M38510/50301BRX	
81035012C	PAL10H8ML883B	M38510/50301B2X	
8103501YC	PAL10H8MF883B	M38510/50301BYX	
8103502RA	PAL12H6MJ883B	M38510/50302BRX	
81035022C	PAL12H6ML883B	M38510/50302B2X	
8103502YC	PAL12H6MF883B	M38510/50302BYX	
8103503RA	PAL14H4MJ883B	M38510/50303BRX	
81035032C	PAL14H4ML883B	M38510/50303B2X	
8103503YC	PAL14H4MF883B	M38510/50303BYX	
8103504RA	PAL16H2MJ883B	M38510/50304BRX	
81035042C	PAL16H2ML883B	M38510/50304B2X	
8103504YC	PAL16H2MF883B	M38510/50304BYX	
8103505RA	PAL16C1MJ883B	M38510/50305BRX	
81035052C	PAL16C1ML883B	M38510/50305B2C	
8103505YC	PAL16C1MF883B	M38510/50305BYX	
8103506RA	PAL10L8MJ883B	M38510/50306BRX	
81035062C	PAL10L8ML883B	M38510/50306B2X	
8103506YC	PAL10L8MF883B	M38510/50306BYX	
8103507RA	PAL12L6MJ883B	M38510/50307BRX	
81035072C	PAL12L6ML883B	M38510/50307B2X	
8103507YC	PAL12L6MF883B	M38510/50307BYX	
8103508RA	PAL14L4MJ883B	M38510/50308BRX	
81035082C	PAL14L4ML883B	M38510/50308B2X	
8103508YC	PAL14L4MF883B	M38510/50308BYX	
8103509RA	PAL16L2MJ883B	M38510/50309BRX	
81035092C	PAL16L2ML883B	M38510/50309B2X	
8103509YC	PAL16L2MF883B	M38510/50309BYX	

*Lead Finishes

A = Solder Dip C = Gold Plate



DESC Drawing Program

DESC Drawing/Generic Part Type Cross Reference continued

DESC DRAWING	Section and append about 100 and appendix of the Control of the Co	REPLACEMENT JAN SPECIFICATION PART NUMBER
8103607RA	PAL16L8AMJ883B1	M38510/50401BRX
81036072C	PAL16L8AML883B	M38510/50401B2X
8103607SA	PAL16L8AMW883B	M38510/50401BYX
8103608RA	PAL16R8AMJ883B1	M38510/50402BRX
81036082C	PAL16R8AML883B	M38510/50402B2X
8103608SA	PAL16R8AMW883B	M38510/50402BYX
8103609RA	PAL16R6AMJ883B1	M38510/50403BRX 6 Details
81036092C	PAI 16R6AMI 883R	M38510/50403B2X 11 010 118
8103609SA	PAL16R6AMW883B	M38510/50403BYX
8103610RA	PAL16R4AMJ883B1	M38510/50404BRX
81036102C	PAL16R4AML883B	M38510/50404B2X
	PAL16R4AMW883B	M38510/50404BYX
8103611RA	**PAL16L8A-2MJ883B	M38510/50407BRX
81036112C	**PAL16L8A-2ML883B	M38510/50407B2X
8103611SC	PAL16L8A-2MF883B	
8103612RA	**PAL16R8A-2MJ883B	M38510/50408BRX
81036122C	**PAL16R8A-2ML883B	M38510/50408B2X
8103612SC	PAL16R8A-2MF883B	
8103613RA	**PAL16R6A-2MJ883B	M38510/50409BRX
81036132C	**PAL16R6A-2ML883B	M38510/50409B2X
8103613SC	PAL16R6A-2MF883B	
8103614RA	**PAL16R4A-2MJ883B	M38510/50410BRX
81036142C	WD41 40D 44 044 000D	M38510/50410B2X
8103614SC	PAL16R4A-2MF883B	DESCORJENING
8412901LA	PAL20L8AMJS883B	M38510/50501BJX
84129013C	PAL20L8AML883B	M38510/50501B3X
8412901KA	PAL20L8AMW883B	010800ra
8412902LA	PAL20R8AMJS883B	M38510/50502BJX
84129023C	PAL20R8AML883B	M38510/50502B3X
8412902KA	PAL20R8AMW883B	\$25088018
8412903LA	PAL20R6AMJS883B	M38510/50503BJX
84129033C	PAL20R6AML883B	M38510/50503B3X
8412903KA	PAL20R6AMW883B	U62.030016
8412904LA	PAL20R4AMJS883B	M38510/50504BJX
84129043C	PAL20R4AML883B	M38510/50504B3X
8412904KA	PAL20R4AMW883B	1000 10,0000 1000 118
8412905LA	PAL20L10AMJS883B	\$103504 <u>Y</u> C
84129053C	PAL20L10AML883B	A22000017
8412906LA	PAL20X8AMJS883B	810350388
84129063C	PAL20X8AML883B	DY8088013
84129063C 8412907LA	PAL20X0AMIC663B	3103506BA
8412907LA 84129073C	PAL20X10AML883B	910350820

^{**}Converting from "A" to "B" PAL in third quarter 1986.

Inactive for new designes using R Case Outline only. Use applicable QPL 38510 device. The Case Outline only. Use applicable QPL 38510 device. The Case Outline only. Use applicable QPL 38510 device. The Case Outline only. Use applicable QPL 38510 device. The Case Outline only. Use applicable QPL 38510 device. The Case Outline only. Use applicable QPL 38510 device. The Case Outline only. Use applicable QPL 38510 device. The Case Outline only. Use applicable QPL 38510 device. The Case Outline only. Use applicable QPL 38510 device. The Case Outline only. Use applicable QPL 38510 device. The Case Outline only. Use applicable QPL 38510 device. The Case Outline only. Use applicable QPL 38510 device. The Case Outline only. Use applicable QPL 38510 device. The Case Outline only. The Case Outline o



DESC Drawing/Generic Part Type Cross Reference continued

DESC DRAWING	GENERIC PART NUMBER	REPLACEMENT JAN SPECIFICATION PART NUMBER
8412908LA	PAL20X4AMJ883B	Mit. M. 38:10 E not produte. Monothine Me
84129083C	PAL20X4AML883B	the right to ship record to based on 52 week o
8506501RA	**PAL16L8A-4MJ883B	C and/or 9 contrage cert Wit-M-883 Revisio
85065012C	**PAL16L8A-4ML883B	overseasons and the ablancation as some ablancation
8506501SC	**PAL16L8A-4MF883B	
8506502RA	**PAL16R8A-4MJ883B	I piesesel uns untuipeiumsik
85065022C	**PAL16R8A-4ML883B	IAM Products Type Tie Memories Med he
8506502SC	**PAL16R8A-4MF883B	sistemen orden. Vincin offi for U.S.A. asset
8506503RA	**PAL16R6A-4MJ883B	
85065032C bessessord stor	**PAL16R6A-4ML883B	in cort is cort in cort in cortined assembly in
8506503SC	**PAL16R6A-4MF883B	Saldonske.
8506504RA	**PAL16R4A-4MJ883B	Mil-Std-881 Chris F- codects, and orders to
85065042C	**PAL16R4A-4ML883B	drawings, whore see - ado-build is not requi
8506504SC	**PAL16R4A-4MF883B	ologist over Particular I Justile Incility Title Re
8515501RA1	PAL16L8BPJ883B	
85155012C1	PAL16L8BPL883B	early of our outstances to manufacture M
8515502RA1	PAL16R8BPJ883B	
85155022C1	PAL16R8BPL883B	propuet. Contomant to Mil-Std-893 remu
8515503RA1	PAL16R6BPJ883B	inely manifored in our needits at the Penan
85155032C1	PAL16R6BPL883B	is incoming inspections to Summyale. Mana
8515504RA1	PAL16R4BPJ883B	nilitas for each_\lane: ini_Memories fucility
85155042C1	PAL16R4BPL883B	 woled herip at three
8515505RA1	PAL16L8BM-2J883B	
85155052C1	PAL16L8BM-2L883B	auditification of the production of the
8515506RA1	PAL16R8BM-2J883B	Market and the Control of the Contro
85155062C1	PAL16R8BM-2L883B	10 2
8515507RA1	PAL16R6BM-2J883B	
85155072C1	PAL16R6BM-2L883B	Assembly yidhis sa'
8515508RA1	PAL16R4BM-2J883B	10,009 4800 01009
85155082C1	PAL16R4BM-2L883B	table of large and the second
PROM: 82008B1JA	53S3281MJ883B	M38510/21102BJX
82008B13C	53S3281ML883B	M38510/21102B3X
82008B2JA	53S3281AJ883B	Ecosar working
82008B23C	53S3281AL883B	Leidersteinsche in Trein Weisens Gunnen 2

^{**}Converting from "A" to "B" PAL in fourth quarter 1986.

1DESC Print 85155 to be released approx. 6/86



Group D-In-depth package related tests

- QCI is conducted every 26 weeks using devices which represent the same package construction and lead finish.
- Any device type in the same package type may be used regardless of the specific part number.
- Purpose: To monitor the reliability and integrity of various package materials and assembly processes.

Generic Data:

Monolithic Memories Generic Data Program is based on MIL-M-38510, which allows for shipments based on 26 weeks of coverage for Group C Testing and 36 weeks of coverage for Group D Testing.

Should circumstances arise where generic coverage to MIL-M-38510 is not possible, Monolithic Memories reserves the right to ship product based on 52 weeks of generic Group C and/or D coverage per MIL-M-883 Revision C.

Manufacturing and Screening Locations

JAN Products, Monolithic Memories Modified Level "S," and customer orders which call for U.S.A. assembly, are manufactured in our DESC certified assembly line in Sunnyvale, California.

Mil-Std-883 Class B products, and orders to source control drawings, where stateside build is not required, are assembled at our Penang, Malaysia facility. This facility is qualified by Monolithic Memories Quality Department, as well as by many of our customers, to manufacture Mil-Std-883 Class B product. Conformance to Mil-Std-883 requirements is routinely monitored through audits at the Penang facility, as well as incoming inspections in Sunnyvale. Manufacturing capabilities for each Monolithic Memories facility are highlighted on the chart below.

Manufacturing Capabilities

	Sunnyvale	Penang
Assembly	X	X
Precap Inspection	X	X
Environmental Testing	X	X
Electrical Pre-Test	X	X
Burn-In	X	X
Post Burn-In Electricals	X	X
Group A Testing	X	X
Mark	X	X
Factory Programming (when applicable)	X	
Qualification and Quality Conformance Testing	X	

To identify the assembly location of each military device, the Country of origin is marked on all products prior to shipment. Products assembled in our stateside facility in Sunnyvale, California, will have "USA" marked on the topside of the device. The exception to this is JAN 38510 product, which is marked to the Mil-M-38510 requirements only.

Offshore built product, which is manufactured in Penang, Malaysia, will have "Malaysia" or "Malay" marked on the bottom side of the device.

Marking Example:



Process Audits

Process Audits are performed in accordance with Mil-M-38510, Appendix A, paragraph 20.1.3.9, self audits by the Quality Assurance Department.

AC Testing

Although Monolithic Memories offers a large selection of programmable products, it must be pointed out that AC Testing cannot be performed on many of our product types without their being programmed. For those devices which must be programmed prior to AC Tests and are ordered unprogrammed, Monolithic Memories must "guarantee" their AC Performance.

Newer devices in the PROM/PLE and PAL families do allow preprogram AC testability at 25°C.

Since the **guaranteeing** of parameters can be a serious concern for the Military user, we have outlined several approaches to address the AC screening issue.

- Monolithic Memories can pull a Sample from a lot using our own Standard patterns (designed to blow in excess of 50 percent of the fuses) and perform AC testing.
 - a) PAL/PROM products processed to DESC prints include programmability samples and AC testing at 25°C.
 - b) PROM/PLE AC testing can be performed at 25°C, -55°C, 125°C temperatures.
- Monolithic Memories can program PROM/PLE's using custom patterns submitted by the customer. AC can then be done with the following options:
 - a) Sample AC at 25°C
 - b) Sample AC at 25°C, -55°C, 125°C
 - c) 100% AC at 25°C
 - d) 100% AC at 25°C, -55°C and 125°C

Note: For PALs contact the factory

On PAL products where custom programming is performed and AC testing is required, additional vector generation and fault coverage analysis is required, as well as AC program generation and checkout.

To give you an idea of delivery differences for the options discussed above, general lead times are as follows:

- · Unprogrammed:
- Cerdip, 4-6 weeks
- Cerpack/Flat pack, 8-12 weeks
- Leadless chip carrier, 6–12 weeks
- (consult monthly leadtime guide for individual part types).
- Unprogrammed product using our standard pattern to verify AC at room temperature on sample basis (option 1).
 Add 2 weeks to standard delivery.
- Programmed product using customer programs with sample AC (option 2a and b). Contact factory for delivery.
 Delivery quoted will be after receipt of customer design package
- 100% AC testing at 25°C—Standard Monolithic Memories pattern or customer pattern, (option c). Contact factory.

Remember, for ProPALs, customer must provide design package including Boolean Equations, "Seed" function test sequence, package stipulation and AC test vectors, when required. Delivery quotes for this type of product begin after receipt of this data from the customer.



VIL/VIH Parametric Information

 V_{IL} and V_{IH} parameters are, in effect, input conditions of D.C. and Functional output tests and are not directly tested. V_{IL} is specified at \leq 0.8 V, and V_{IH} is specified at \geq 2.0 V.

ElectroStatic Discharge

The Military Products Division of Monolithic Memories has fully implemented static control procedures throughout its facilities in Penang, Malayasia and Sunnyvale, California.

All manufacturing areas where product is processed or handled, including our Reliability Labs, Engineering Labs, etc., have full static control such as wrist straps, antistatic smocks, grounded stainless steel tables, conductive mats and ion generators wherever necessary.

All product is moved throughout our facilities and shipped to customers in static shielded containers.

In addition, MPD distributors must demonstrate that they meet the same stringent standards governing ESD handling and control procedures as the factory. Individual distributor locations are audited and approved annually by MPD's Quality Assurance Department.

An ESD identifier is marked on all products in front of the date code, and all shipping containers are labeled with an ESD Caution Message. These procedures have been implemented, and will continually be reviewed, to ensure that our customers receive only the highest quality product from the Military Products Division.

Package Information

Leadless Chip Carrier/Pin Grid Array

Monolithic Memories' Military Products Division offers, with few exceptions, our entire product line in square, ceramic leadless chip carriers.

8-BIT INTERFACE

• 20 square LCC

PROM CIRCUITS (Programmable Read Only Memories)

- 20 square LCC
- 28 square LCC

PLE CIRCUITS (Programmable Logic Elements)

- 20 square LCC
- 28 square LCC

PAL/HAL* CIRCUITS (Programmable Array Logic)

- · 20 square LCC
- 28 square LCC
- · 44 square LCC

HMSI CIRCUITS (High-Complexity

Medium Scale Integration)

28 square LCC

FIFO CIRCUITS (First-In-First-Out Memories)

20 square LCC

DOUBLE-DENSITY INTERFACE CIRCUITS

- 20 square LCC
- · 28 square LCC

MULTIPLIER CIRCUITS

44 square LCC

^{*}HALs are the mask-programmable versions of PAL

Military Ordering Information

PAL/PROM/PLE Programming Inputs:

- A. Two masters (programmed device) and checksum
- B. Master and truthtable (or product terms for PAL)
- C. Master and magnetic tape (VAX compatible)
- D. Master and floppy disk (VAX compatible)
- PALASM/PLEASM IBM compatible floppies, VAX compatible magnetic tape or floppies
- F. Master only (least preferred)

NOTES: Deput to the said of the service of the said of

If options A, B, C, D or E are submitted, Monolithic Memories may require customer approval of prototypes before proceeding with programming.

If option F is submitted, Monolithic Memories will require customer approval of factory generated prototypes before proceeding.

Military Ordering Information Minimum Order Guidelines:

- Standard (unprogrammed/non-programmable) product Mil-Std-883, Class B DESC Print Devices JAN Devices Requires a \$1000.00 (\$250 per line item) per order
- Source Control Drawings (unprogrammed/ non-programmable) product Requires a \$1000.00 (\$250 per line item) per order
- ProPAL32R16
 \$5K per pattern
 500 units min per pattern
 200 units min per request date per pattern
- HAL20RA10 & 24RS Family \$5K per pattern*
 2500 units min per pattern
 1000 units min per request date per pattern
- HAL20/24
 \$3K per combinatorial pattern
 \$4K per sequential pattern
 2500 units min per pattern
 1000 units min per request date per pattern

Military Ordering Information Cancellation Policy:

HAL (Mask Programmable Devices)

- · 60 days firm.
- 90 days uncancellable.
- 61-90 days can be rescheduled once up to 60 days out.
- Any line item shortage of less than 5% can be rescheduled for next delivery date (or cancelled).

ProPAL/ProPROM/ProPLE (Programmed Devices)

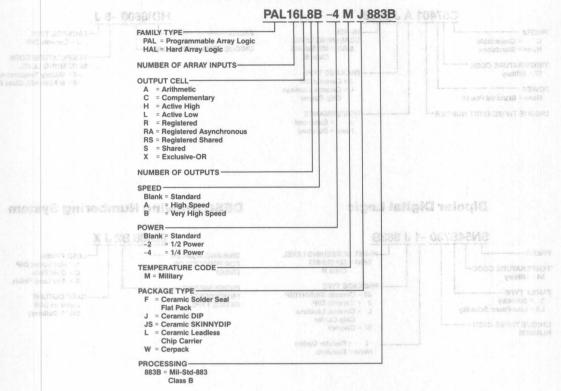
- · 30 days firm.
- 60 days uncancellable.
- 31-60 days can be rescheduled once up to 60 days out.
- Any line item shortage of less than 5% can be rescheduled for next delivery date (or cancelled).

Terms: place a a room one or against his bas, about end

70%/30 Days, 30%/45 Days from date of invoice, F.O.B. Sunnyvale, California.

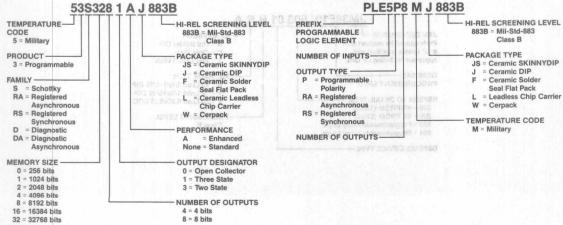
^{*}Applicable to 20RA10 only. Assumes customers provide a set of test vectors, verifiable to 90% fault grading for all HAL devices.



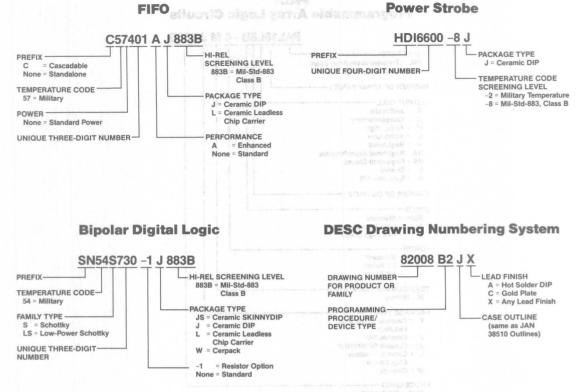


High Performance PROMs

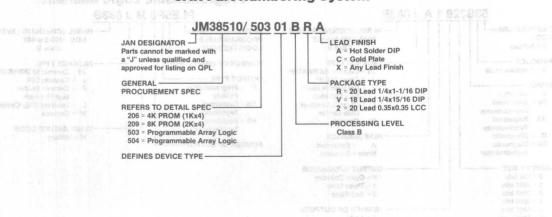
PLE™ Programmable Logic Element



Power Strobe



JAN Part Numbering System



A THE BASE OF THE PROPERTY OF

Introduction Military Products Division **PROM PLE™** Devices **PAL®** Devices HAL®/ZHAL™ Devices System Building Blocks/HMSI™ 8 FIFO **Memory Support Arithmetic Elements and Logic** Multipliers 8-Bit Interface **Double-Density PLUS™ Interface** ECL10KH 14 **Logic Cell Array General Information Advance Information Package Drawings** Representatives/Distributors

PROMs	Table	e of	Co	ntents		
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53/63S080 53/63S081	32x8 bit			53/63RS881A	1024x8 bit Registered	3-42
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53/63S140	256x4 bit			30/0011/11001	Enable	3-46
53/63S141	256x4 bit			53/63RA1681A	2048x8 bit Registered w/Asyn	0 10
53/63S141A	256x4 bit			35/05/14/100/14	Enable	3-46
53/63S240	512x4 bit			53/63RS1681	2048x8 bit Registered w/Sync	0 10
53/63S240 53/63S241	512x4 bit			33/03/13/100/	Enable	3-50
	512x4 bit			53/63RS1681A	2048x8 bit Registered w/Sync	0 00
53/63S241A	256x8 bit			33/03N31001A	Enable	3-50
53/63S280					Enable	3-30
53/63S281	256x8 bit					
53/63S281A	256x8 bit			Diagnostic Reg	istared PPOMs	
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Typical ICC vs	Temperature/TAA vs Temperature	3-31		53/63DA1643	4096x4 bit Diagnostic Registered	
Switching Test I	_oad	3-37			Output Initialization	3-79
Definition of Wa	veforms	3-37		Monolithic Memo	ories PROM Programmer Reference	
	gram			Chart		3-86

Monolithic IIII Memories

PROM Performance Analysis (Maximum Commercial Limits)

		MMI (7	TiW)		I (NiCr)	A	MD	FUJIT	SU	HA	RRIS	NAT	IONAL	SIGNETICS		ŢI	
Туре	Out- put	Part No.	TAA*/ICC		NCE ONLY) TAA/ICC	Part No.	TAA*/ICC	Part No.	TAA*/ICC	Part No.	TAA/ICC	Part No.	TAA*/ICC	Part No.	TAA/ICC	Part No.	TAA/IC
1/4K (32x8)	OC TS	63S080 63S081	25/125 25/125	6330-1 6331-1	50/125 50/125	27S18 27S18A 27S19	40/115 25/115 40/115	7111E 7111H 7112E	35/100 25/100 35/100	7602 7603	50/130	74S188 74S288	35/110 35/110	82S23 82S23A 82S123	50/96 25/96 50/96	18SA030 18S030	40/110 40/110
		63S081A	15/125			27S19A	25/115	7112H 7112Y	25/100 20/100					82S123A	25/96		
1K (256x4)	OC	63S140	45/130	6300-1	55/130	27S20 27S20A	45/130 30/130	7113	30/100	7610 7610A 7610B	60/130 45/110 35/110	74S387	50/130	82S126 82S126A	50/120 30/120	24SA10	65/100
JEST (MCM)	TS	63S141 63S141A	45/130 30/130	6301-1	55/130	27S21 27S21A	45/130 30/130	7114	30/100	7611 7611A 7611B	60/130 45/110 35/110	74S287	50/130	82S129 82S129A	50/120 27/120	24S10	55/100
2K (256x8)	OC TS	63S281 63S281A	45/140 45/140 28/140	6308-1 6309-1	70/155 70/155	SMRLOIV SMRSR)	S\$1.199 951.199	7117E 7117H 7118E 7118H	45/140 35/140 45/140 35/140	8-18161A 8-18161A	80/190 30/190	74LS471	60/100	82S135	45/155	28LA22 28L22	75/100 70/100
2K (256x8) 24-Pin DIP	TS	63S285	45/160	6336-2	70/155	51313G+ 514 134	32035	20-00W, 0.13914 0.1395	123,400 003,400	METOTAL METOTAL	081,180	SERIES I	68/173	521419 52151	PV (6/8 -)	580200	312
2K (512x4)	OC	63S240	45/130	6305-1	60/130	27S12 27S12A	50/130 30/130	7115E 7115H	45/120 35/120	7620 7620A 7620B	70/130 50/120 40/120	74S570 74S570A	55/130 45/130	82S130 82S130A	50/140 33/140		
	TS	63S241 63S241A	45/130 35/130	6306-1	60/130	27S13 27S13A	50/130 30/130	7116E 7116H 7116Y	45/120 35/120 30/120	7621 7621A 7621B	70/130 50/120 40/120	74S571 74S571A 74S571B	55/130 45/130 35/130	82S131 82S131A	50/140 30/140		35/110
4K (512x8)	OC TS	63S480 63S481	45/155 45/155	6348-1 6349-1	70/155 70/155	27S28 27S28A 27S29	55/160 35/160 55/160	7123E 7123H 7124E	45/170 35/170 45/170	7649	60/170	74S473 74S473A 74S472	60/155 45/155 60/155	000147	60/155	28SA42 28L42	65/135
	10	63S481A		6349-2	55/155	27S29A	35/160	7124H	35/170	7649A	45/170	74S472A 74S472B	45/155 35/155	82S147 82S147A	60/155 45/155	28542	95/85 60/135
4K (512x8) 24-Pin DIP	TS	63S485	45/160	6341-1 6341-2	70/155 55/155	27S31 27S31A	55/175 35/175	1,25N 1,25N	35/175 46/1775 35/175	7641 7641A	70/170 45/170	74S474 74S474A 74S474B	65/170 45/170 35/170	82S141	60/175	28S46	60/135
4K (512x8) Registered	TS	63RA481 63RA481A	20/180 15/180			27S25 27S25A	27/185 20/185	7226RA/RS-25 7226RA/RS-20	25/170 20/170			87SR25 87SR25B	27/185 20/185		to the		
4K (1Kx4)	OC	63\$440	45/140	6352-1	60/175	27S32 27S32A	55/140 35/140	7121E 7121H	45/150 35/150	7642 7642A 7642B	60/140 50/140 45/140	74S572 74S572A	60/140 45/140	Part (6)	1712/160 EUroti	24SA41	60/140
	TS	63S441 63S441A	45/140 35/140	6353-1 6353-2	60/175 50/140	27S33 27S33A	55/140 35/140	7122E 7122H 7122Y	45/150 35/150 30/150	7643 7643A 7643B	60/140 50/140 45/140	74S573 74S573A 74S573B	60/140 45/140 35/140	82S137 82S137A 82S137B	60/140 45/140 35/140	24S41	60/140

PROM Performance Analysis (Maximum Commercial Limits) 30 Tot 76400 45/140 [7485739 | 35/140 [8281378 | 55/140

	Out	MMI (T	MMI (TiW)		MMI (NICr) (REFERENCE ONLY)		AD	FUJIT	SU	HAI	RRIS	NAT	ONAL	SIGNETICS		TI	
Туре	put	Part No.	TAA*/ICC		TAA/ICC	Part No.	TAA*/ICC	Part No.	TAA*/ICO	Part No.	TAA/ICC	Part No.	TAA*/ICC	Part No.	TAA/ICC	Part No.	TAA/IC
4K (1Kx4) Diagnostic	TS	63DA441 63DA442	18/180 18/180			27S65 27S65A	15/185 12/185	72.00 A PE 25	25.170 20.070			9186991)	\$DV/82				
8K (1Kx8) 600-mil DIP	TS	63S881 63S881A		6381-1 6381-2	90/175 55/170	27S181 27S181A	60/185 35/185	7132E 7132H 7132Y	55/175 45/175 35/175	7681 7681A	70/170 50/170	87S181 87S181A	55/170 45/170		70/175 55/175 45/175	28S86A	65/165
8K (1Kx8) 300-mil DIP	TS	63S881NS 63S881ANS		6381-1NS 6381-2NS	90/175 55/170	27S281 27S281A	60/185 35/185	7132E-SK 7132H-SK 7132Y-SK	55/175 45/175 35/175	6-7681 6-7681A	70/170 50/170	87\$281	55/170	82S181N3 82S181AN3	70/175 55/175	322vs 387 4 5	em : 12 84 F0
8K (1Kx8) Registered	TS	63RS881 63RS881A	20/180 15/180	6.445-1	V0/1196	27S35/37 27S35/37A	25/185 20/185	7232RA/RS-25 7232RA/RS-20	25/185 20/185			87SR181	20/175			SRBANS	85/140
8K (2Kx4)	TS	63S841 63S841A		6389-1 6389-2	70/170 55/155	27S185 27S185A	50/150 35/150	7128E 7128H 7128Y	55/155 45/155 35/155	7685 7685A	70/170 50/170	87S185 87S185A 87S185B	55/140 45/140 35/140		100/120 50/155 45/155	24\$81	70/175
8K (2Kx4) Diagnostic	TS	63DA841	20/185	05/10-1	Les 36	27S75 27S75A	15/185 12/185	1108	38.126	5650# 6650#	36 (20)	243976A	45/130	5251204 5251204	30/140		
16K (2Kx8) 600-mil DIP	TS	63S1681 63S1681A	50/185 35/185	2-1016	107/00	27S191 27S191A	50/185 35/185	7138E 7138H 7138Y	55/180 45/180 35/180	76161 76161A	60/180 50/180	87S191 87S191A 87S191B	65/175 45/175 35/175	82S191 82S191A 82S191B	80/185 55/185 45/185	28S166	75/175
16K (2Kx8) 300-mil DIP	TS	63S1681NS 63S1681ANS	50/185 35/185	1910g-1	100 100 100 100	27S291 27S291A	50/185 35/185	7138E-SK 7138H-SK 7138Y-SK	55/180 45/180 35/180	6-76161 6-76161A	60/180 50/180	87S291	65/175	82S191BN3	45/185	28/ 478	18/199
16K (2Kx8) Registered	TS	63RA/RS1681 63RA/RS1681A	20/185 15/185			27S45/47 27S45/47A	25/185 20/185			19: R	g7 [10			850 I UM	511.70		
16K (4Kx4)	TS	63S1641 63S1641A	50/175 35/175	£30	ETE/80	27S41 27S41A	50/165 35/165	7152E 7152H 7152Y	55/170 45/170 35/170	76165	60/170	87S195A 87S195B	45/170 35/170	82HS195	45/155	24310	
16K (4Kx4) Diagnostic	TS 2S	63D1641 63DA1643	20/190			27S85 27S85A	15/185 12/185	(i	25/120				20114	808 (27V	12/13		
32K (4Kx8)	TS	63S3281 63S3281A	45/190 35/190	SCIA I	262 123	27S43 27S43A	55/185 40/185	7142E 7142H	65/185 55/185	76321	65/190	87\$321	55/185	82S321 82HS321	70/175 45/175	10/31/005	100.110
64K (8Kx8)	TS	63S6481** 63S6481A	55/190 45/190	58111977	PRAIDO	27S49 27S49A	55/190 40/190	7144E 7144H	65/190 55/190	76641	85/190	Fain	BAND	to the	IVARY	Page No.	Teach In

^{*}tCLK for Registered and Diagnostic PROMs
**Preliminary Information

High Performance 32x8 PROM TiW PROM Family

mance 53/63S080 53/63S081 Family 63S081A

Features/Benefits

- 15-ns maximum access time
- Reliable titanium-tungsten fuses (TiW) guarantee greater than 98% programming yields
- · Low-voltage generic programming
- PNP inputs for low input current
- · Open collector or three-state outputs.

Applications

- Programmable logic element (PLE™) 5 inputs, 8 outputs, 32 product terms
- Address decoder
- Priority encoder

Description

The 53/63S080, 53/63S081 and 63S081A feature low input current PNP inputs, full Schottky clamping and three-state and open collector outputs. The titanium-tungsten fuses store a logical low and are programmed to the high-state. Special on-chip circuitry and extra fuses provide preprogramming testing which assures high programming yields and high reliability.

The 63 series is specified for operation over the commercial temperature and voltage range. The 53 series is specified for the military ranges.

Programming

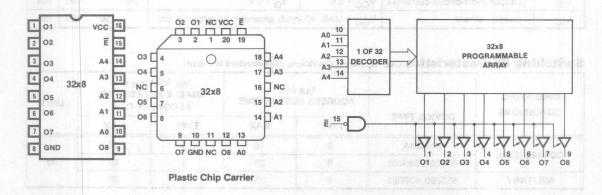
The 53/63S080, 53/63S081 and 63S081A are programmed with the same programming algorithm as all other Monolithic Memories' generic TiW PROMs. For details contact the factory.

Selection Guide

	MEMORY	PACKAGE		PEDEODMANICE	PART NUMBER		
SIZE	ORGANIZATION	OUTPUT	PINS	TYPE	PERFORMANCE	0°C to +75°C	-55°C to +125°C
	K2 -	TS	Hoth	N,J,W (NL),(L)	Enhanced	63S081A	erailer — pursik
1/4 K	32x8	TS	16 (20)			63S081	53S081
		OC	(20)	((4L),(L)	Standard	63\$080	53\$080

Pin Configurations

Block Diagram



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TWX: 910-338-2376 2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2374

Monolithic MM

53/63S080 53/63S081 63S081A

Absolute Maximum Ratings

Absolute maximum natings	Operating	Programming
Supply voltage VCC	0.5 V to 7 V	12 V
Input voltage	1.5 V to 7 V	7 V
Input current	30 mA to +5 mA	A STATE OF STATE OF
Off-state output voltage		
Storage temperature -6	55 °C to +150 °C	

Operating Conditions

SYMBOL	rent Periopolita, fulli schoolitic uterpling end free open content of the PARAMETER los pequipolitics of the content of the c	MILITARY MIN NOM MAX	COMMERCIAL MIN NOM MAX	UNIT
VCC	Supply voltage, see I sales has quifornic quito	4.5 5 5.5	4.75 5 5.25	V
TA	Operating free-air temperature	-55 125	0 75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	en e a desenhar i El	TEST CONDITION		MIN TYP†	MAX	UNIT
VILLIBRE	Low-level input voltage	boossasa seri				0.8	V
VIH	High-level input voltage	the same progra			2	graph se	V
VIC	Input clamp voltage	V _{CC} = MIN	100	V			
IIL	Low-level input current	V _{CC} = MAX	V _I = 0.4 V		-0.25	mA	
I _I H.	High-level input current	V _{CC} = MAX	V _I = V _{CC} MAX	s-bitti	40	μА	
V -	Low-level output voltage	V - AMINI	SICAMOAT	Com	PONEW	0.45	V
VOL	200-level output voltage	VCC = MIN	I _{OL} = 16 mA	Mil	TO TITIBLE	0.5	
V and	Ulab Javel 4 (400 A) also a *	SVERE CLEANING	Com I _{OH} = -3.2	2.4		V	
VOH	High-level output voltage*	V _{CC} = MIN	Mil I _{OH} = -2 mA	Y 27	2.4		DI NAT
lozL	Off state suitant surrent*	Standard	V _O = 0.4 V	55.5			
lozh	Off-state output current*	V _{CC} = MAX	V _O = 2.4 V	and the second second	A minor exercise (sedimino district	40	μΑ
1	Open collector output ourrent	V - MAY	V _O = 2.4 V		5.6	40	
CEX	Open collector output current	V _{CC} = MAX	V _O = 5.5 V	100		μΑ	
los	Output short-circuit current**	V _{CC} = 5 V	V _O = 0 V		-20	-90	mA
lcc	Supply current	VCC = MAX. AI	MAX. All inputs grounded. All outputs open.			125	mA

Switching Characteristics Over Operating Conditions (See standard test load)

OPERATING CONDITIONS	DEWOL TABE		(ns) CCESS TIME	t _{EA} AND ENABLE AC RECOVE	UNIT	
	DEVICE TYPE	TYP†	MAX	TYP†	MAX	
ALVA VA VAIV	63S081A	9	15	9	20	ns
COMMERCIAL	63S080, 63S081	9	25	9	20	
MILITARY	53S080, 53S081	9	35	Parelle Chie	30	

^{*} Three-state only

^{**} Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

[†] Typicals at 5.0 V V_{CC} and 25°C T_A.

High Performance 256x4 PROM TIW PROM Family

53/63\$140 53/63\$141 53/63\$141

Features/Benefits

- 30-ns maximum access time
- Reliable titanium-tungsten fuses (TiW) guarantee greater than 98% programming yields
- Low-voltage generic programming
- PNP inputs for low input current
- · Open collector or three-state outputs

Applications

- · Microprogram control store
- Microprocessor program store
- Look-up table
- Character generator
- Code converter
- Programmable Logic Element (PLE™) with 8 inputs, 4 outputs, and 256 product terms

Description

The 53/63S140 and 53/63S141/A are 256x4 bipolar PROMs featuring low input current PNP inputs, full Schottky clamping, and open collector or three-state outputs. The titanium-tungsten fuses store a logical low and are programmed to the high state. Special on-chip circuitry and extra fuses provide preprogramming testing which assures high programming yields and high reliability.

The 63 series is specified for operation over the commercial temperature and voltage range. The 53 series is specified for the military ranges.

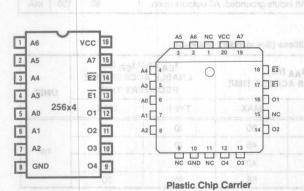
Programming

The 53/63S140 and 53/63S141/A PROMs are programmed with the same programming algorithm as all other Monolithic Memories' generic TiW PROMs. For details contact the factory.

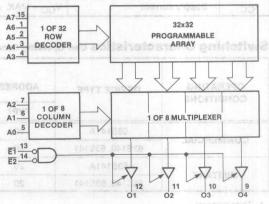
Selection Guide

	MEMORY	PACKAGE		MIM = ggV s	PART NUMBER		
SIZE	ORGANIZATION	OUTPUT	PINS	TYPE	PERFORMANCE	0°C to +75°C	-55°C to +125°C
Au		TS	VaCa		Enhanced	63S141A	53S141A
1 K	256x4	TS	16 (20)	N,J,W, (NL),(L)		63S141	53S141
		ОС	(20)	((4),()	Standard	63S140	53S140

Pin Configurations



Block Diagram



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TWX: 910-338-2376

3-7

Absolute Maximum Ratings

Absolute maximum hatings		[- (1) [[[[[[[[[[[[[[[[[[[
	Operating	Programming
Supply voltage V _{CC}	0.5 V to 7 V	12 V
Input voltage	1.5 V to 7 V	7 V
Input current	30 mA to +5 mA	
Off-state output voltage	0.5 V to 5.5 V	12 V
Storage temperature	65° to +150°C	

Operating Conditions

SYMBOL	PARAMETER PRODUCTION OF THE PA	MILITARY MIN NOM MAX		COMMERCIAL MIN NOM MAX			UNIT	
Vcc	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
TA	Operating free-air temperature	-55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	Scient Autors of Mil.	TEST CONDITION		MIN TYP†	MAX	UNIT
VIL	Low-level input voltage			530	ts ransome se	0.8	V
VIH	High-level input voltage				2	okoni qi	V
VIC	Input clamp voltage	V _{CC} = MIN	I _I = -18 mA		1172221191	-1.5	V
TIL BORRE	Low-level input current	V _{CC} = MAX	V _I = 0.4 V	series in the series	see 27 siese La	-0.25	mA
I _{IH}	High-level input current	V _{CC} = MAX	V _I = V _{CC} MAX	1 1944	Setona BES.	40	μΑ
V/	1 1 1 1 1	V - MINI	I _{OL} = 16 mA	Com		0.45	V
VOL	VOL Low-level output voltage	V _{CC} = MIN		Mil	s-hi-u/2	0.5	V
· · ·			Com I _{OH} = -3.2 mA		0.41		V
VOH	High-level output voltage*	V _{CC} = MIN	Mil I _{OH} = -2 mA		2.4		V
lozL	0"-1-1	V 144V	V _O = 0.4 V			-40	A
lozh	Off-state output current*	V _{CC} = MAX	V _O = 2.4 V	81		40	μΑ
187	0	burbates	V _O = 2.4 V	81	1-48-57	40	
CEX	Open collector output current	V _{CC} = MAX	V _O = 5.5 V		Property and the second second second	100	μΑ
los	Output short-circuit current**	V _{CC} = 5 V	V _O = 0 V		-20	-90	mA
¹ CC	Supply current	VCC = MAX. AI	AX. All inputs grounded. All outputs open.		80	130	mA

OPERATING CONDITIONS	DEVICE TYPE		A (ns)	tEA AND E	CESS TIME	UNIT
	1C. 1	TYP†	MAX	TYP†	MAX	2669
	63S141A	20	30	10	20 10	ns
COMMERCIAL	63S140, 63S141	20	45	10	25	
MILITARY	53S141A	20	40	m == 10	30	da
	53S140, 53S141	20	55	10	30	

^{*} Three-state only.

^{**} Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

[†] Typicals at 5.0 V VCC and 25°C TA.

High Performance 512x4 PROM Ti-W PROM Family

53/63\$240 53/63\$241 53/63S241A

Features/Benefits

- 35-ns maximum access time
- Reliable titanium-tungsten fuses (TiW) guarantee greater than 98% programming yields
- Low-voltage generic programming
- . PNP inputs for low input current
- . Open collector or three-state outputs

Applications

- Microprogram control store
- Microrocessor program store
- Look-up table
- · Character generator
- Code converter
- Programmable logic element (PLE™) with 9 inputs, 4 outputs. 512 product terms

Description

The 53/63S240 and 53/63S241/A are 512x4 bipolar PROMs featuring low input current PNP inputs, full Schottky clamping, and open collector or three-state outputs. The titaniumtungsten fuses store a logical low and are programmed to the high-state. Special on-chip circuitry and extra fuses provide preprogramming testing which assures high programming vields and high reliability.

The 63 series is specified for operation over the commercial temperature and voltage range. The 53 series is specified for the military ranges.

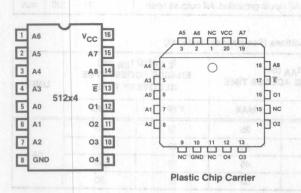
Programming

The 53/63S240 and 53/63S241/A PROMs are programmed with the same programming algorithm as all other Monolithic Memories generic Ti-W PROMs. For details contact the factory.

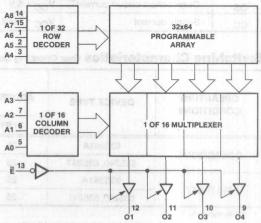
Selection Guide

	MEMORY		PAC	KAGE	DEDECRIMANCE	PART NUMBER		
SIZE	ORGANIZATION	OUTPUT	PINS	TYPE	PERFORMANCE	0°C to +75°C	-55°C to +125°C	
04		TS	V A.O = D.4	4 1 1	ok line	Enhanced	63S241A	53S241A
2 K	512x4	TS	16 (20)	N,J,W, (NL),(L)		63S241	53S241	
		ОС	(20)	(141),(1)	Standard	63S240	53S240	

Pin Configurations



Block Diagram



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TWX: 910-338-2376



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Absolute Maximum Ratings

	Operating	Programming
Supply voltage V _{CC}	0.5 V to 7 V	12 V
Input voltage	1.5 V to 7 V	7 V
Input current		
Off-state output voltage	-0.5 V to 5.5 V	12 V
Storage temperature	65° to +150°C	
621703230		

Operating Conditions

SYMBOL	PARAMETER 90 bns.	MILITARY MIN NOM MAX		COMMERCIAL MIN NOM MAX			UNIT	
Vcc	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
TA	Operating free-air temperature maid bits ablery	-55	100	125	0	di teo tea	75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TE	EST CONDITION		MIN TYP† MAX	UNIT
VIL	Low-level input voltage				0.8	V
VIH	High-level input voltage		w 1-1		2	V
V _{IC}	Input clamp voltage	V _{CC} = MIN I _I = -18 mA			-1.5	V
HEON 1	Low-level input current	V _{CC} = MAX V _I = 0.4 V _I			mA	
TIH	High-level input current	V _{CC} = MAX	VI = VCC MAX		lemmai iou 40	μΑ
\/	Law lavel autout values	N/ - MINI	10 1	Com	0.45	
VOL	Low-level output voltage	V _{CC} = MIN	I _{OL} = 16 mA	Mil	0.5	V
	SEARCH TELES	340000000	Com I _{OH} = -3.2 mA Mil I _{OH} = -2 mA		2.4 SMADRO	V
VOH	High-level output voltage*	V _{CC} = MIN				
lozL	ed sis241A B	positing	V _O = 0.4 V	ST.	-40	
lozh	Off-state output current*	V _{CC} = MAX	V _O = 2.4 V	BT .	AG18 40	μΑ
35240	838840	.,	V _O = 2.4 V	90	40	
CEX	Open collector output current	V _{CC} = MAX	V _O = 5.5 V		100	μΑ
los	Output short-circuit current**	V _{CC} = 5 V	V _O = 0 V	8	-20 -90	mA
^I CC	Supply current	V _{CC} = MAX. All inputs grounded. All outputs open.			80 130	mA

OPERATING CONDITIONS	DEVICE TYPE		ACCESS TIME	ENABLE AC	t _{ER} (ns) CCESS TIME RY TIME	UNIT
		TYP†	MAX	TYP†	MAX	CA
00111150111	63S241A	25	35	12	20	ns
COMMERCIAL	63S240, 63S241	25	45	12	25	
MILITARY	53S241A	25	45	12	30	
	53S240, 53S241	25	55	12	30	

^{*} Three-state only.

^{**} Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

† Typicals at 5.0 V V_{CC} and 25°C T_A.

High Performance 256x8 PROM TiW PROM Family

53/63\$280 53/63\$281 53/63\$281A

Features/Benefits

- 28-ns maximum access time
- Reliable titanium-tungsten fuses (TiW) guarantee greater than 98% programming yields
- Low-voltage generic programming
- PNP inputs for low input current
- . Open collector or three-state outputs

Applications

- Microprogram control store
- Microprocessor program store
- Look-up table
- Character generator
- Code converter
- Programmable Logic Element (PLE™) with 8 inputs, 8 outputs, and 256 product terms

Description

The 53/63S280 and 53/63S281/A are 256x8 bipolar PROMs featuring low input current PNP inputs, full Schottky clamping, and open collector or three-state outputs. The titanium-tungsten fuses store a logical low and are programmed to the high state. Special on-chip circuitry and extra fuses provide preprogramming testing which assures high programming yields and high reliability.

The 63 series is specified for operation over the commercial temperature and voltage range. The 53 series is specified for the military ranges.

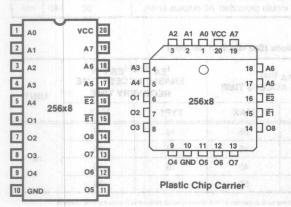
Programming

The 53/63S280 and 53/63S281/A PROMs are programmed with the same programming algorithm as all other Monolithic Memories' generic TiW PROMs. For details contact the factory.

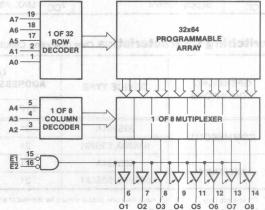
Selection Guide

	MEMORY	MEMORY PACKAGE		DEDECRIMANCE	PART NIMBER			
SIZE	ORGANIZATION	OUTPUT	PINS	TYPE	PERFORMANCE	0°C to +75°C	-55° C to +125° C	
	1 1	TS	N.IW	N,J,W	0 - 0 -	Enhanced	63S281A	53S281A
2 K	256x8	TS			C. I. I.	63S281	53S281	
	A .	ОС	VAS =	1	Standard	63S280	53S288	

Pin Configurations



Block Diagram



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Monolithic Memories



3

Absolute Maximum Ratings Operating Programming Supply voltage V_{CC}. -0.5 V to 7 V .12 V Input voltage Input current -1.5 V to 7 V .7 V Input current -30 mA to +5 mA .30 mA to +5 mA Off-state output voltage -0.5 V to 5.5 V .12 V Storage temperature -65° to +150°C

Operating Conditions

SYMBOL	PARAMETER PARAMETER	MILITARY COMMERCIAL MIN NOM MAX MIN NOM MAX	UNIT
VCC	Supply voltage	4.5 5 5.5 4.75 5 5.25	V
TA	Operating free-air temperature	-55 125 0 works 75	°C

DC Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	Т	EST CONDITION		MIN TYP† MAX	UNIT
VIL	Low-level input voltage				0.8	٧.
VIH	High-level input voltage	DATE OF THE PARTY			2 seignarian and	V
V _{IC}	Input clamp voltage	V _{CC} = MIN	I _I = -18 mA		1.5	V
» կլեում	Low-level input current	V _{CC} = MAX	V _I = 0.4 V and 8 charge quitting			mA
ЧН	High-level input current	V _{CC} = MAX	V _I = V _{CC} MAX	1.786	40	μΑ
.,	1 - 1 - 1 - 1 - 1		101	Com	0.45	
VOL	Low-level output voltage	V _{CC} = MIN	I _{OL} = 16 mA	Mil	0.5	V
	ASSESSED TALAS	8040F-76000	Com 1 _{OH} = -3.2 mA Mil 1 _{OH} = -2 mA		2.4 SMAGRO	V
VOH	High-level output voltage*	V _{CC} = MIN				
lozL	BB ATBORES :	Bahabu	V _O = 0.4 V	25	-40	
lozh	Off-state output current*	V _{CC} = MAX	V _O = 2.4 V	e T	40	μΑ
182138	839.280		V _O = 2.4 V	00-1	40	
CEX	Open collector output current	V _{CC} = MAX	V _O = 5.5 V		100	μΑ
los	Output short-circuit current**	V _{CC} = 5 V	V _O = 0 V		-20 -90	mA
lcc	Supply current	V _{CC} = MAX. All i	nputs grounded. All o	utputs open.	90 140	mA

OPERATING CONDITIONS	DEVICE TYPE		A (ns) ACCESS TIME	tEA AND ENABLE ACC	CESS TIME	UNIT
CONDITIONS		TYP†	MAX	TYP†	MAX	(25) FA
COMMEDOIAL	63S281A	21 54	28	18	25	8.6-
COMMERCIAL	63S280, 63S281	21	45	18	25	200
MILITARY	53S281A	21	40	18	30	ns
	53S280, 53S281	21	50	18	30	100

^{*} Three-state only.
** Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

[†] Typicals at 5.0 V VCC and 25° C TA.

High Performance 256x8 PROM TiW PROM Family

Features/Benefits

- Replaces 24-pin 256x8 NiCr PROM (6336)
- Upward pinout-compatible with higher density PROMs
- 45-ns maximum access time
- Reliable titanium-tungsten fuses (TiW) guarantee greater than 99% programming yields
- · Low voltage generic programming
- · PNP inputs for low input current
- . Three-state outputs with four enable pins

Applications

- Microprogram control store
- Microprocessor program store
- Look-up table
- · Character generator
- Code converter

Description

The 63S285 is a 256x8 bipolar PROM featuring low-current PNP inputs, full Schottky clamping, and three-state outputs. The titanium-tungsten fuses store a logical low and are programmed to the high state. Special on-chip circuitry and extra fuses provide preprogramming testing which assures high programming yields and high reliability.

The 63 series is specified for operation over the commercial temperature and voltage range.

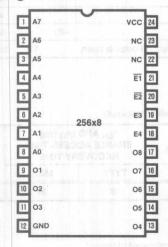
Programming

The 63S285 PROM is programmed with the same programming algorithm as all other Monolithic Memories generic TiW PROMs. For details contact the factory.

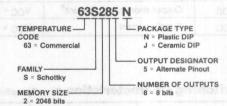
Selection Guide

	MEMORY	PA	CKAGE	OUTPUT	PERFORMANCE	PART NUMBER
SIZE	ORGANIZATION	PINS	TYPE	OUTPOT	PERFORMANCE	0°C to +75°C
2K	256x8	24	N,J	TS	Standard	63S285

Pin Configuration



Part Numbering System



Monolithic Memories TWX: 910-338-2376

Absolute Maximum Ratings Operating Programming Supply voltage V_{CC} -0.5 V to 7 V 12 V Input voltage -1.5 V to 7 V 7 V Input current -30 mA to +5 mA Off-state output voltage -0.5 V to 5.5 V 12 V

Storage temperature -65° to +150°C

Operating Conditions

SYMBOL	q Mg/m language starting grades print PARAMETER with page software useful to tred		MMER NOM		UNIT
VCC	e Supply voltage of an audiorus at settes 19 5/71	4.75	5	5.25	V
TA	Operating free-air temperature	0		75	°C

DC Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITION		MIN TYP† N	XAI	UNIT
VIL	Low-level input voltage	Guaranteed input logical low voltage for all inputs††		0.8		V
VIH	High-level input voltage	Guaranteed input logical high voltage for all inputs††		2		V
VIC	Input clamp voltage	V _{CC} = MIN	I _I = -18 mA	1 6756C3 64 TO	-1.5	V
ηL	Low-level input current	VCC = MAX	V _I = 0.4 V	-(0.25	mA
ΊΗ	High-level input current	VCC = MAX	VI = VCC MAX		40	μΑ
VOL	Low-level output voltage	VCC = MIN IOL = 16 mA		THE CATE OF	0.45	V
VOH	High-level output voltage	V _{CC} = MIN	I _{OH} = -3.2 mA	2.4		V
lozL	malayd onhea		V _O = 0.4 V	MARKET STEEL	-40	101
lozh	Off-state output current	V _{CC} = MAX	V _O = 2.4 V	ex re-initialization (fig.	40	μΑ
los	Output short-circuit current*	V _{CC} = 5 V	V _O = 0 V	-20 -90		mA
Icc	Supply current	V _{CC} = MAX. All inputs grounded. All outputs open.		115	160	mA

OPERATING CONDITIONS	DEVICE TYPE		(ns) CCESS TIME	ENABLE AC	ter (ns) CCESS TIME RY TIME	UNIT
		TYP†	MAX	TYP†	MAX	ONIT
COMMERCIAL	63S285	26	45	18	30	ns

^{*} Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

[†] Typicals at 5.0 V V_{CC}, and 25° C T_A.

^{††} VIL and VIH limits are absolute values with respect to the device ground pin(s) and include all overshoots due to test equipment noise.

High Performance 1024x4 PROM TiW PROM Family

53/63S440 53/63S441 53/63S441A

Features/Benefits

- 35-ns maximum access time
- Reliable titanium-tungsten fuses (TiW) guarantee greater than 98% programming yields
- Low-voltage generic programming
- . PNP inputs for low input current
- . Open collector or three-state outputs

Applications

- Microprogram control stores
- Microprocessor program store
- Look-up table
- Character generator
- Code converter
- Programmable logic element (PLE™) 10 inputs, 4 outputs, 1024 product terms

Description

The 53/63S440 and 53/63S441/A are 1024x4 bipolar PROMs featuring low input current PNP inputs, full Schottky clamping with open collector or three-state outputs. The titanium-tungsten fuses store a logical low and are programmed to the high-state. Special on-chip circuitry and extra fuses provide preprogramming testing which assures high programming yields and high reliability.

The 63 series is specified for operation over the commercial temperature and voltage range. The 53 series is specified for the military ranges.

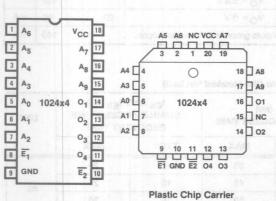
Programming

The 53/63S440 and 53/63S441/A PROMs are programmed with the same programming algorithm as all other Monolithic Memories' generic TiW PROMs. For details contact the factory.

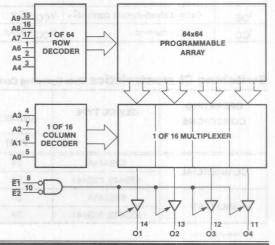
Selection Guide

	MEMORY		PACKAGE		PERFORMANCE SO	PART NUMBER			
SIZE	ORGANIZATION	OUTPUT	PINS	TYPE	PERFORMANCE	0°C to +75°C	-55°C to +125°C		
V	1000	TS	- Falcill		Enhanced	63S441A	53S441A		
4 K	1024x4	I S	18				0	63S441	53S441
		ОС	(20)	((42),(2)	Standard	63S440	53\$440		

Pin Configuration



Block Diagram



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Monolithic | Memories



3

Absolute Maximum Ratings

	Operating	Programming
Supply voltage V _{CC}	0.5 V to 7 V	12 V
Input voltage	1.5 V to 7 V	7 V
Input current	30 mA to +5 mA	
Off-state output voltage	0.5 V to 5.5 V	
Storage temperature	65° to +150°C	

Operating Conditions the two total and profused

SYMBOL	ingorgens bris wer ladge PARAMETER bisgnid Laure bris wer ladge PARAMETER bisgnid	MILITARY COMMERCIAL MIN NOM MAX MIN NOM MAX	UNIT
Vcc	Supply voltage anim prifer parameter animal policing	4.5 5 5.5 4.75 5 5.25	V
TA	Operating free-air temperature	-55 125 0 10 75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITION		MIN TYP† MA	K UNIT
VIL	Low-level input voltage	navero e e e e e e e e e e e e e e e e e e			0.	8 V
VIH	High-level input voltage	The 53 63 544			2	V
VIC	Input clamp voltage	V _{CC} = MIN	I _I = -18 mA	10 01 (E. 19) In	wint is raipot eta 7.	5 V
I _{IL}	Low-level input current	V _{CC} = MAX	V _I = 0.4 V		-0.2	5 mA
IH	High-level input current	V _{CC} = MAX	V _I = V _{CC} MAX		4	0 μΑ
	er and the second services of the second second second second	N/ MINI	10-1	Com	0.4	5 V
VOL	Low-level output voltage	V _{CC} = MIN	I _{OL} = 16 mA	Mil	0.	5
1 80 5 35	3 86-1 3 875-1 3 0	Com I _{OH} = -3.2 mA		LITANBADEO	3516	
VOH	High-level output voltage*	V _{CC} = MIN	Mil I _{OH} = -2 mA	(et i	2.4	V
lozL	828 44	West May	V _O = 0.4 V	31	io#S01 -4	
lozh	Off-state output current*	V _{CC} = MAX	V _O = 2.4 V	DC	4	0 μΑ
	0	V FAAV	V _O = 2.4 V		4	0
CEX	Open collector output current	V _{CC} = MAX	V _O = 5.5 V		10	0 μΑ
los	Output short-circuit current**	V _{CC} = 5 V	V _O = 0 V		-20 -9	0 mA
lcc	Supply current	VCC = MAX. AI	I inputs grounded. All of	outputs open.	95 14	0 mA

OPERATING CONDITIONS	DEVICE TYPE		(ns) CCESS TIME	ENABLE A	D t _{ER} (ns) CCESS TIME ERY TIME	UNIT
	I I I I I I I I I I I I I I I I I I I	TYP†	MAX	TYP†	MAX	
COMMEDCIAL	63S441A	24	35	16	25	mie
COMMERCIAL	63S440, 63S441	24	45	16	25	ns
MILITARY	53S441A	24	50	16	30	
	53S440, 53S441	24	55	16	30	

[·] Three-state only.

^{**} Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

[†] Typicals at 5.0 V VCC and 25°C TA.

High Performance 512x8 PROM TiW PROM Family

53/63S480 53/63S481 53/63S481A

Features/Benefits

- 30 ns maximum access time
- Reliable titanium-tungsten fuses (TiW) guarantee greater than 98% programming yields
- Low voltage generic programming
- . PNP inputs for low input current
- · Open collector or three-state outputs

Applications

- Microprogram control store
- · Microprocessor program store
- · Look-up table
- Character generator
- Code converter
- Programmable Logic Element (PLE™) with 9 inputs, 8 outputs, and 512 product terms

Description

The 53/63S480 and 53/63S481/A are 512x8 bipolar PROMs featuring low input current PNP inputs, full Schottky clamping, and open collector or three-state outputs. The titanium-tungsten fuses store a logical low and are programmed to the high state. Special on-chip circuitry and extra fuses provide preprograming testing which assures high programming yields and high reliability.

The 63 series is specified for operation over the commercial temperature and voltage range. The 53 series is specified for the military ranges.

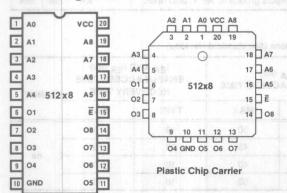
Programming

The 53/63S480 and 53/63S481/A PROMs are programmed with the same programming algorithm as all other Monolithic Memories' generic TiW PROMs. For details contact the factory.

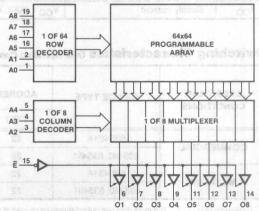
Selection Guide

	MEMORY		PAC	KAGE	PEDECONANIOS	PART NUMBER	
SIZE	ORGANIZATION	OUTPUT	PINS	TYPE	PERFORMANCE	0°C to +75°C	-55°C to +125°C
as F		TS	La b		Enhanced	63S481A	53S481A
4 K	512x8	TS	20	N,J,F, NL,L	0	63S481	53S481
		ОС	The C	INL,L	Standard	63S480	53S480

Pin Configurations



Block Diagram



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Monolithic Memories

3-17

3

Absolute Maximum Ratings	Operating	Programming
Supply voltage V _{CC}	0.5 V to 7 V	, 12 V
Input voltage	1.5 V to 7 V	
Input current	30 mA to +5 mA	
Off-state output voltage	0.5 V to 5.5 V	12 V
Storage temperature	65° to +150°C	Company and the company of the

Operating Conditions

SYMBOL	escuring low input content PulP inputs, full Schools and content a	2009 1 19 12 14 14	ILITARY NOM MAX	COMMER MIN NOM		UNIT
Vcc	Supply voltage on a volume of the supply voltage	4.5	5 5.5	4.75 5	5.25	y V.
TA DIE SE	Operating free-air temperature	-55	125	Organ wolls	75	°C

DC Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITION		MIN TYP† MAX	UNIT
VIL	Low-level input voltage				0.8	3 V
VIH	High-level input voltage			240	2	V
VIC	Input clamp voltage	V _{CC} = MIN	I _I = -18 mA		noternous -1.	200
IIL.	Low-level input current	V _{CC} = MAX	V ₁ = 0.4 V		-0.25	
JiHi ali	High-level input current	V _{CC} = MAX	VI = VCC MAX	V _I = V _{CC} MAX		μΑ
1/	Leveleval autout valtage	V - MINI	1 - 10 1	Com	6.msf kut 0.4	5 V
VOL	Low-level output voltage	V _{CC} = MIN	I _{OL} = 16 mA	Mil	chian no.	
v 5	25/41057/2AS*	V _{CC} = MIN		Com I _{OH} = -3.2 mA		
VOH	High-level output voltage*			2.4	V	
lozL		V MAY	V _O = 0.4 V	And the second	-4(
lozh		V _{CC} = MAX	V _O = 2.4 V	67	40	μΑ
Total	Once collector output oursel	ebriata J	V _O = 2.4 V	(3)	40	
CEX	Open collector output current	V _{CC} = MAX	V _O = 5.5 V		100	μΑ
los	Output short-circuit current**	V _{CC} = 5 V	V _O = 0 V	V _O = 0 V) mA
Icc	Supply current	V _{CC} = MAX. All	inputs grounded. All o	outputs open.	104 155	mA

OPERATING CONDITIONS	DEVICE TYPE		(ns)	ENABLE A	O t _{ER} (ns) CCESS TIME ERY TIME	UNIT
TEXT POT A SES	to L MAN	TYP†	MAX	TYP†	MAX	10
COMMERCIAL	63S481A	22	30 cr st	18	25	ns
COMMERCIAL	63S480, 63S481	22	45.0 10	18	25	
MUITARY	53S481A	22	40	18	30	
MILITARY	53S480, 53S481	22	50	18	35	

[†] Typicals at 5.0 V V_{CC} and 25° C T_A.

High Performance 512x8 PROM TiW PROM Family

53/63\$485

Features/Benefits

- . Upward pinout-compatible with higher density PROMs
- 45-ns maximum access time
- Reliable titanium-tungsten fuses (TiW) guarantee greater than 99% programming yields
- Low-voltage generic programming
- . PNP inputs for low input current
- Three-state outputs with four ANDed enable pins
- Saves space with 24-pin SKINNYDIP® package

Description

The 53S485 and 63S485 are 512x8 bipolar PROMs featuring low current PNP inputs, full Schottky clamping, and three-state outputs. The titanium-tungsten fuses store a logical low and are programmed to the high state. Special on-chip circuitry and extra fuses provide preprogramming testing which assures high programming yields and high reliability.

The 63 series is specified for operation over the commercial temperature and voltage range. The 53 series is specified for the military ranges.

Applications

- Microprogram control store
- Microprocessor program store
- Look-up table

• Character generator The 53S485 and 63S48

The 53S485 and 63S485 PROMs are programmed with the same programming algorithm as all other Monolithic Memories generic TiW PROMs. For details contact the factory.

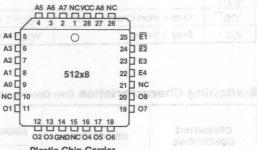
Selection Guide

err 20	MEMORY	OUTPUT	F	PACKAGE	DEDECRMANCE	PART	NUMBER
SIZE	ORGANIZATION	OUTPUT	PINS	TYPE	PERFORMANCE	0°C to +75°C	-55°C to +125°C
4K	512x8	muo TS	24 (28)	NS,JS,N,J,W, (NL),(L)	Standard	63S485	53\$485

Pin Configurations



Code converter



Plastic Chip Carrier

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Monolithic Memories



3

Absolute Maximum Ratings

Absolute Maximum natings	Operating	Programming
Supply voltage VCC	0.5 V to 7 V	12 V
Input voltage	1.5 V to 7 V	7 V
Input current	-30 mA to +5 mA	
Off-state output voltage	0.5 V to 5.5 V	12 V
Storage temperature	-65° C to +150° C	

Operating Conditions and ESPERA Land REPERATOR AND ARREST AND REPORT OF THE PROPERTY OF THE PR

SYMBOL	PARAMETER STORE OF THE		MILITARY MIN NOM I		COMMERCIAL MIN NOM MAX			UNIT
Vcc	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
TA	Operating free-air temperature	-55		125	0		75	°C

DC Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	Time 535485 an	EST CONDITION		MIN TYP†	MAX	UNIT
VIL	Low-level input voltage	Guaranteed input	it logical low voltage	* 25012	era gosaj viso	0.8	V
VIH	High-level input voltage	Guaranteed inputer for all inputs	t logical high voltage		2		V
VIC	Input clamp voltage	V _{CC} = MIN	I _I = -18 mA	ments in policy of		-1.5	V
IIL II	Low-level input current	V _{CC} = MAX	V _I = 0.4 V	mar	7.295,2.483	-0.25	mA
High of D	High-level input current	V _{CC} = MAX	VI = VCC MAX		H LASIMAKINI	40	μΑ
VOL	Low-level output voltage	VCC = MIN	M.21.2M RG	Com	512942	0.45	XAV
VOL	Low-level output voltage	ACC - MIN	IOL = 16 mA	Mil	Lipter v. ottadav, tieje x jeze ======	0.5	V
Vон	High-level output voltage	VCC = MIN	Com IOH = -3.2 mA	1	0.4		1
VOH	r light-level output voltage	ACC - MIIA	Mil I _{OH} = -2 mA		2.4		V
lozL	Off-state output current	V	V _O = 0.4 V	NT IN		-40	
IOZH	On-state output current	V _{CC} = MAX	V _O = 2.4 V			40	μΑ
los**	Output short-circuit current**	V _C C = 5 V	VO = 0 V		-20	-90	mA
Icc	Supply current	VCC = MAX. All i	nputs grounded. All o	utputs open.	115	160	mA

OPERATING CONDITIONS	DEVICE TYPE		(ns) CCESS TIME	tEA AND ENABLE AC RECOVE	UNI		
	ells, Clap Cerrier	TYP†	MAX	TYP†	MAX	Olviii	
COMMERCIAL	63S485	26	45	18	30		
MILITARY	53S485	26	55	18	35	ns	

^{**} Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

[†] Typical at 5.0 V VCC, and 25° C TA.

High Performance 2048x4 PROM TiW PROM Family

53/63\$841 53/63\$841A

Features/Benefits

- 35-ns maximum access time
- Reliable titanium-tungsten fuses (TiW) guarantee greater than 98% programming yields
- Low-voltage generic programming
- . PNP inputs for low input current

Applications

- · Microprogram control store
- · Microprocessor program store
- · Look-up table
- Character generator
- Code converter
- Programmable Logic Element (PLE") with 11 inputs,
 4 outputs and 2048 product terms per output

Description

The 53/63S841 and 53/63S841A are 2048x4 bipolar PROMs featuring low input current PNP inputs, full Schottky clamping, and three-state outputs. The titanium-tungsten fuses store a logical low and are programmed to the high state. Special on-chip circuitry and extra fuses provide preprogramming testing which assures high programming yields and high reliability.

The 63 series is specified for operation over the commercial temperature and voltage range. The 53 series is specified for the military ranges.

Programming

The 53/63S841 and 53/63S841A PROMs are programmed with the same programming algorithm as all other Monolithic Memories generic TiW PROMs. For details contact the factory.

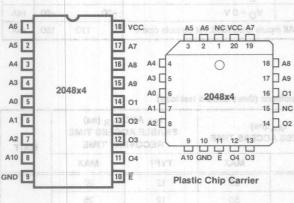
Electrical Ci srectoristics over operand Conditions

Selection Guide

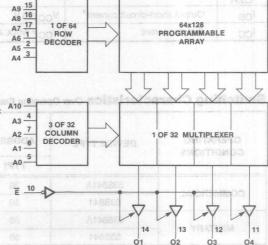
	MEMORY	Visi	PACKAGE		PEDEODIMANOE	PART	NUMBER
SIZE	ORGANIZATION	OUTPUT	PINS	TYPE	PERFORMANCE	0°C to +75°C	-55°C to +125°C
V	0040.4	An An	18	N,J,W,	Enhanced	63S841A	53S841A
8 K	2048x4	TS	(20)*	(NL),(L)	Standard	63S841	53S841

^{*} Available in either a 20 or 28 terminal ceramic Leadless Chip Carrier.

Pin Configurations



Block Diagram



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Absolute Maximum Ratings	Operating	Programming
Supply voltage V _{CC}	0.5 V to 7 V	12 V
Input voltage	1.5 V to 7 V	7 V
Input current	–30 mA to +5 mA	
Off-state output voltage	0.5 V to 5.5 V	
Storage temperature	65° to +150°C	

Operating Conditions

SYMBOL	t resepred-mensal ent a PARAMETER et bas		MILITARY MIN NOM MAX		COMMERCIAL MIN NOM MAX			UNIT	
Vcc	Supply voltage and sales but valuations side		4.5	5	5.5	4.75	5	5.25	V
TA	Operating free-air temperature		-55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	unstyors.	TEST CONDITION		MIN TYP†	MAX	UNIT
V _{IL}	Low-level input voltage	r persone anno The same aroun	.ebicani Fr dhi	w ("B.F9) Insu	the Logic Ste	0.8	V
VIH	High-level input voltage	ig Will pheneg		o tesp system for	0		No V
VIC	Input clamp voltage	V _{CC} = MIN	V _{CC} = MIN I _I = -18 mA			-1.5	V
1/L	Low-level input current	V _{CC} = MAX	V _I = 0.4 V	LOS NORTH	-0.25	mA	
lн	High-level input current	V _{CC} = MAX	V _I = V _{CC} MAX		trans a chromina in a ch	40	μΑ
V SATE OF	Law level extent velters	V - MINI	- 10 - 1	Com	THE PROPERTY OF THE	0.45	V
VOL	Low-level output voltage	V _{CC} = MIN	I _{OL} = 16 mA	Mil	2048-4	0.5	N 8
149.8	(88/2) b	BDM418	Com I _{OH} = -3.2 r	Com I _{OH} = -3.2 mA			
VOH	High-level output voltage	V _{CC} = MIN	Mil I _{OH} = -2 mA	sa, pine o scho	2.4		V
lozL	niste.	Hook Di	V _O = 0.4 V	1	nelizne	-40	D esse
lozh	Off-state output current	V _{CC} = MAX	MAX V _O = 2.4 V			40	μΑ
los	Output short-circuit current*	V _{CC} = 5 V	V _O = 0 V		-20	-90	mA
I _{CC}	Supply current	V _{CC} = MAX. All inputs grounded. All outputs open.			110	150	mA

OPERATING CONDITIONS	DEVICE TYPE		(ns)	ENABLE A	O t _{ER} (ns) CCESS TIME ERY TIME	TINU
	language of the second	TYP†	MAX	TYP†	MAX	[8] on
	63S841A	30	35	12	25	ns
COMMERCIAL	63S841	30	50	12	25	
MILITARY	53S841A	30	50	12	30	
	53S841	30	55	12	30	

^{*} Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

[†] Typicals at 5.0 V VCC and 25° C TA.

High Performance 1024x8 PROM TiW PROM Family

53/63\$881 53/63\$881

Features / Benefits

- · 30-ns maximum access time
- · Reliable titanium-tungsten fuses (TiW) guarantee greater than 99% programming yields
- Low-voltage generic programming
- . PNP inputs for low input current
- Three-state outputs
- 24-pin SKINNYDIP® or 600-mil DIP package

Applications

- Microprogram control stores
- Microprocessor program store
- Look-up table
- Character generator
- Code converter
- Programmable Logic Element (PLE™) with 10 inputs, 8 outputs and 1024 product terms

Selection Guide

Description

The 53/63S881 and 53/63S881A are 1024x8 bipolar PROMs featuring low input current PNP inputs, full Schottky clamping. and three-state outputs. The titanium-tungsten fuses store a logical low and are programmed to the high state. Special on-chip circuitry and extra fuses provide preprogramming testing which assures high programming yields and high reliability.

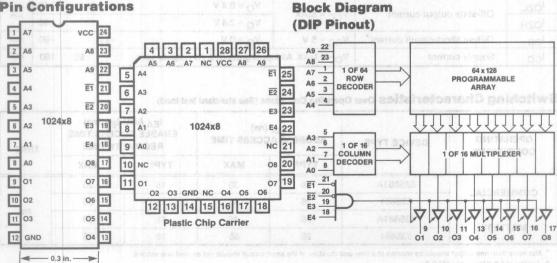
The 63 series is specified for operation over the commercial temperature and voltage range. The 53 series is specified for the military ranges. DC Electrical Characteristics over operat

Programming

The 53/63S881 and 53/63S881A PROMs are programmed with the same programming algorithm as all other Monolithic Memories generic TiW PROMs. For details contact the factory.

MEMORY		OLITRUT	PACKAGE		DEDECRIMANOE	PART NUMBER	
SIZE	ORGANIZATION	OUTPUT	PINS	TYPE	PERFORMANCE	0°C to +75°C	-55°C to +125°C
OV	1004-0	TO 1 S. 8	24	NS,JS,N,J,W,	Enhanced	63S881A	53S881A
8K	1024x8	TS	(28)	(NL),(L)	Standard	63S881	53\$881

Pin Configurations



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ARRAY

Absolute Maximum Ratings Operating Operating Programming Supply voltage V_{CC}. -0.5 V to 7 V 12 V Input voltage Input current -1.5 V to 7 V 7 V Input current -30 mA to +5 mA -0.5 V to 5.5 V 12 V Storage temperature -65° C to +150° C -65° C to +150° C

Operating Conditions

SYMBOL	and three state outputs, the transmit sungeren in logical ImaRAMETER og animed to the high st	MILITARY MIN NOM MAX	COMMERCIAL MIN NOM MAX	UNIT
Vcc	Supply voltage and assume that pulled	4.5 5 5.5	4.75 5 5.25	e V
TA	Operating free-air temperature	-55 125	0 alugho a 75	°C

DC Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	Presention .	TEST CONDITION		MIN TYP†	MAX	UNIT
VIL	Low-level input voltage	Guaranteed input logical low voltage for all inputs			10 Tolerans	0.8	Joseph Character
VIH	High-level input voltage	Guaranteed input logical high voltage for all inputs		2	iavnos	ab V	
VIC	Input clamp voltage	V _{CC} = MIN	I _I = -18 mA		d 1828 produc		V
IIL	Low-level input current	V _{CC} = MAX	V _I = 0.4 V			-0.25	mA
1 _{IH}	High-level input current	V _{CC} = MAX	V _I = V _{CC} MAX		William Committee Co	40	μΑ
- 1	Low-level output voltage V _{CC} = MIN	HAROBRE -	10-1	Com	A CONTRACTOR OF THE CONTRACTOR	0.45	V
VOL		I _{OL} = 16 mA	Mil	ALTERNATION OF THE PROPERTY OF	0.5	V	
A) 988		W, crinanci	Com I _{OH} = -3.2	mA	2.4	Ţ	V
VOH	High-level output voltage	V _{CC} = MIN	Mil I _{OH} = -2 m	A	7 2.4		V
lozL	Office of the second		V _O = 0.4 V	18	a of terrup	-40	μΑ
lozh	Off-state output current	V _{CC} = MAX	V _O = 2.4 V		40		μΑ
los	Output short-circuit current*	V _{CC} = 5 V	V _O = 0 V		-20	-90	mA
lcc	Supply current	V _{CC} = MAX. All inputs grounded. All outputs open.			92	160	mA

OPERATING CONDITIONS	DEVICE TYPE		(ns) CCESS TIME	t _{EA} AND ENABLE ACC RECOVER	CESS TIME	UNIT
		TYP† 35 at	MAX	TYP†	MAX	
	63S881A	26	30	18	25	101.6
COMMERCIAL	63S881	26	45	18	30	50 (1)
MILITARY	53S881A	26	45	18	30	ns
	53\$881	26	55	18	35	

^{*} Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

[†] Typical at 5.0 V VCC, and 25°C TA.

High Performance 4096x4 PROM TiW PROM Family

53/63\$1641A

Features/Benefits

- 35-ns maximum access time
- · Reliable titanium-tungsten fuses (TiW)
- Low-voltage generic programming
- . PNP inputs for low input current

Applications

- Microprogram control stores
- Microprocessor program store
- Look-up table
- Character generator
- Code converter
- Programmable Logic Element (PLE™) 12 inputs, 4 outputs, 4096 product terms

Description

The 53/63S1641 features low input current PNP inputs, full Schottky clamping and three-state outputs. The titanium-tungsten fuses store a logical low and are programmed to the high state. Special on-chip circuitry and extra fuses provide pre-programming testing which assures high programming yields and high reliability.

The 63 series is specified for operation over the commercial temperature and voltage range. The 53 series is specified for the military ranges.

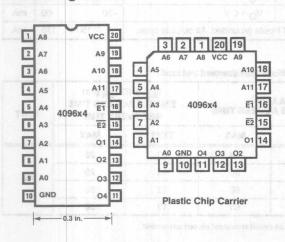
Programming

The 53/63S1641 PROM is programmed with the same programming algorithm as all other Monolithic Memories' generic TiW PROMs. For details contact the factory.

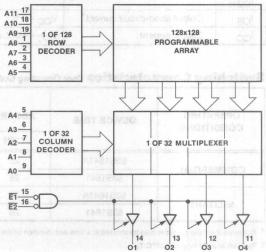
Selection Guide

	MEMORY	MEMORY			PART NUMBER		
SIZE	ORGANIZATION	OUTPUT	PACKAGE	PERFORMANCE	0°C to +75°C	-55°C to +125°C	
		Am S S + mg.	Por Ton	N,J,	Enhanced	63S1641A	53S1641A
16 K	4Kx4	TS	HO NL	Standard	63S1641	53S1641	

Pin Configuration



Block Diagram



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Monolithic M. Memories

Absolute Maximum Ratings Operating Operating Programming Programming Supply voltage V_{CC} -0.5V to 7V 12V Input voltage -1.5V to 7V 7V Input current -30mA to +5mA

 Off-state output voltage
 .-0.5V to 5.5V
 12V

 Storage temperature
 -65°C to +150°C

Operating Conditions

SYMBOL	COO MA DATA A DE LACIONE PARAMETER TRANSPER	MILITARY MIN NOM MAX			1000000	NOM	UNIT	
Vcc	Supply voltage	4.5	5	5.5	4.75	5	5.25	٧
TA	Operating free-air temperature	-55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITION		MIN TYP† MAX	UNIT
VIL	Low-level input voltage	anton pure	0.8	V		
V _{IH}	High-level input voltage	The 15/80516		2 197997003	٧	
Vic	Input clamp voltage	V _{CC} = MIN I _I = -18 mA		-1.5	V	
Ι _Ι L	Low-level input current	V _{CC} = MAX	MAX V _I = 0.4 V		-0.25	mA
ЧН	High-level input current	V _{CC} = MAX	V _I = V _{CC} MAX		40	μА
	DENGE TEAN	NA PAIN	343334	Com	0.45	V
VOL	L Low-level output voltage VCC	V _{CC} = MIN	I _{OL} = 16 mA	Mil	0.741mA080 0.5	BELZE
Atteta	d statelly to	sonedes.	Com I _{OH} = -3.2 mA		0.4	
VOH	High-level output voltage	V _{CC} = MIN	Mil I _{OH} = -2 mA	T	2.4	N aV
lozL	Off and the second seco	100 00000000000000000000000000000000000	V _O = 0.4 V	re region of the first and	-40	
lozh	Off-state output current	V _{CC} = MAX	V _O = 2.4 V		40	μΑ
los	Output short-circuit current*	V _{CC} = 5 V	V _O = 0 V		-20 -90	mA
lcc	Supply current	V _{CC} = MAX. All inputs grounded. All outputs open.		130 175	mA	

OPERATING CONDITIONS	DEVICE TIME		(ns) CCESS TIME	ENABLE A	D t _{ER} (ns) CCESS TIME ERY TIME	TINU
		TYP†	MAX	TYP†	MAX	-71
THE UNIT	63S1641A	28	35	12	25	ns
COMMERCIAL	63S1641	28	50	12	25	
MILITARY	53S1641A	28	50	12	30	
	53S1641	28	65	12	30	

^{*} Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

 $[\]dagger$ Typicals at 5.0 V VCC and 25° C TA.

53/63S1681A

High Performance 2048x8 PROM **TIW PROM Family**

Features/Benefits

- 35-ns maximum access time
- 16384-bit memory
- · Reliable titanium-tungsten fuses (TiW)
- Available in space saving SKINNYDIP® package

Applications

- Microprogram control stores
- Microprocessor program store
- Look-up table
- Character generator
- Code converter
- Programmable Logic Element (PLE™) 11 inputs, 8 outputs, 2048 product terms

Description

The 53/63S1681 is a high-speed 2Kx8 PROM which uses industry standard package and pin out. In addition, the device is available in the 24-pin (0.3 in.) SKINNYDIP®.

53/63\$1681

The family features low current PNP inputs, full Schottky clamping and three-state outputs. The Titanium-Tungsten fuses store a logical low and are programmed to the high state. Special on-chip circuitry and extra fuses provide preprogramming tests which assure high programming yields and high

The 63 series is specified for operation over the commercial temperature and voltage range. The 53 series is specified for the military ranges.

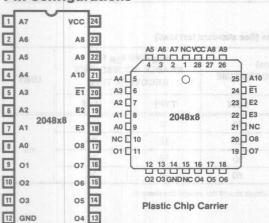
Programming

The 53/63S1681 PROM is programmed with the same programming algorithm as all other Monolithic Memories' generic TiW PROMs. For details contact the factory.

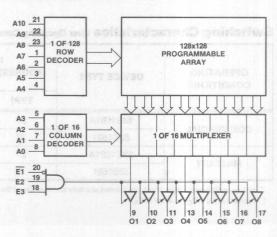
Selection Guide

	MEMORY			PACKAGE	PEDEODMANOE	PART NUMBER		
SIZE	ORGANIZATION	OUTPUT	PINS	TYPE	PERFORMANCE	0°C to +75°C	-55°C to +125°C	
4014	0040.0	TO	24 N,NS,J,	24	N.NS,J,JS,W,	Enhanced	63S1681A	53S1681A
16K	2048x8	TS	(28)	(NL),(L)	Standard	63S1681	53S1681	

Pin Configurations



Block Diagram



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53/63S1681 53/63S1681A

Absolute Maximum Ratings	Operating	Programming
Supply voltage V _{CC}	0.5 V to 7 V	12 V
Input voltage	1.5 V to 7 V	7 V
Input current	30 mA to +5 mA	
Off-state output voltage	0.5 V to 5.5 V	12 V
Storage temperature	65°C to +150°C	

Operating Conditions

SYMBOL	PARAMETER	MILITARY COMMERCIAL MIN NOM MAX MIN NOM MAX	UNIT
Vcc	Supply voltage	4.5 5 5.5 4.75 5 5.25	٧
TA	Operating free air temperature	-55 125 0 75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	yffidslar -	TEST CONDITION		MIN TYP† MAX	UNIT
V _{IL}	Low-level input voltage	M SSRES GO SM		830.	0.8	V
VIH	High-level input voltage	gres yazilen, ani			2	V
VIC	Input clamp voltage	V _{CC} = MIN	I _I = -18 mA	-1.5	V	
Legoa	Low-level input current	V _{CC} = MAX	V _I = 0.4 V	-0.25	mA	
TIH O	High-level input current	V _{CC} = MAX	V _I = V _{CC} MAX	40	μΑ	
V	Law level extrust valters	V = MINI	I _{OL} = 16 mA	Com	0.45	V
VOL	V _{OL} Low-level output voltage V _C	V _{CC} = MIN		Mil	0.5	24 NE Z
V/	Ulah landa da d	V - MINI	Com I _{OH} = -3.2	24 YROYTH	V	
VOH	High-level output voltage	VCC = MIIN	V _{CC} = MIN Mil I _{OH} = -2 mA			2.4
lozL	Off state output oursel	V - 144V	V _O = 0.4 V		-40	Δ.
lozh	Off-state output current	V _{CC} = MAX	V _O = 2.4 V		102503 40	μΑ
los	Output short-circuit current*	V _{CC} = 5 V	V _O = 0 V		-20 -90	mA
Icc	Supply current	V _{CC} = MAX. All	inputs grounded. All o	135 185	mA	

Switching Characteristics Over Operating Conditions (See standard test load)

OPERATING CONDITIONS	DEVICE TYPE		t _{AA} (ns) ADDRESS ACCESS TIME		t _{EA} AND t _{ER} (ns) ENABLE ACCESS TIME RECOVERY TIME		
		TYP†	MAX	TYP†	MAX	100	
COMMEDOIAL	63S1681A	27	35	18	25	alati.	
COMMERCIAL	63S1681	27	50	18	30		
eleje din je kyalo	53S1681A	27	50	18	30	ns	
MILITARY	53S1681	27	60	18	35		

^{*} Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

† Typicals at 5.0 V VCC and 25° C TA.

High Performance 4096x8 PROM **TiW PROM Family**

53/63**S**3281 53/63**S**3281**A**

Features/Benefits

- 35-ns maximum access time
- 32768-bit memory
- Reliable titanium-tungsten fuses (TiW)
- . PNP inputs for low input current

Applications

- Microprogram control stores
- Microprocessor program store
- · Look-up table
- Character generator
- Code converter
- Programmable Logic Element (PLE™) with 12 inputs, 8 outputs and 4096 product terms

Description

The 53/63S3281 is a high-speed 4Kx8 PROM which uses industry standard pin out.

The family features low-current PNP inputs, full Schottky clamping and three-state outputs. The Titanium-Tungsten fuses store a logical low and are programmed to the high state. Special on-chip circuitry and extra fuses provide preprogramming testing which assure high programming yields and high reliability.

The 63 series is specified for operation over the commercial temperature and voltage range. The 53 series is specified for the military ranges.

Programming

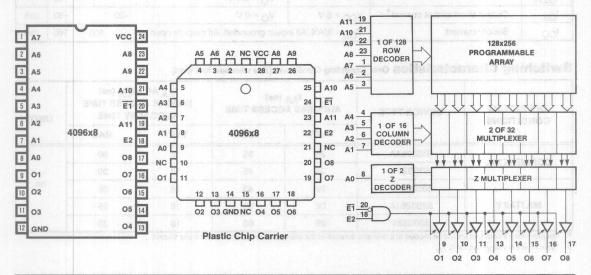
The 53/63S3281 PROM is programmed with the same programming algorithm as all other Monolithic Memories' generic TiW PROMs. For details contact the factory.

Selection Guide

	MEMORY			KAGE	DEDECRIANCE	PART NUMBER					
SIZE	ORGANIZATION	OUTPUT	PINS	TYPE	PERFORMANCE	0°C to +75°C	-55°C to +125°C				
00.14	1000 0	46 2 1	24	N,J,W,	Enhanced	63S3281A	53S3281A				
32 K	4096x8	TS	(28)*	(28)*	(28)*	(28)*	(NL),(L)	(NL),(L)	Standard	63S3281	53S3281

Pin Configurations

Block Diagram



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Absolute Maximum Ratings	Operating	Programming
Supply voltage V _{CC}	0.5 V to 7 V	12 V
Input voltage	1.5 V to 7 V	7 V
Input current	30 mA to +5 mA	
Off-state output voltage	0.5 V to 5.5 V	12 V
Storage temperature	65°C to +150°C	

Operating Conditions the at 1890288480 and

SYMBOL	The faugated are three-state and the Therman	MILITARY MIN NOM MAX			COMMERCIAL MIN NOM MAX			UNIT
Vcc	Supply voltage making woll ablig of a mote assuff	4.5	5	5.5	4.75	5	5.25	V
TA	Operating free-air temperature	-55		125	0	8690	75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	us yasana sa	TEST CONDITION		MIN TYP† MAX	UNIT
VIL	Low-level input voltage	seedengsen W			0.8	ob oV
V _{IH}	High-level input voltage	The 53/63832	etion 12 insuts	(13) In their	2 algo il aldamos	Vog.
V _{IC}	Input clamp voltage is as motion	V _{CC} = MIN	I _I = -18 mA	ec max to	abortq 8000 brir-1.5	V
I _{IL}	Low-level input current	V _{CC} = MAX	V _I = 0.4 V		-0.25	mA
-I _{IH}	High-level input current	V _{CC} = MAX	V _I = V _{CC} MAX	with the second second	40	μΑ
	20%	LMROTRES	TORNA STORY	Com	0.45	
VOL+ of	Low-level output voltage	V _{CC} = MIN	I _{OL} = 16 mA	Mil	0.5	as V
A #8588		unerlu3 .V	Com I _{OH} = -3.2 m.	A	2.4	V
VOH	High-level output voltage	V _{CC} = MIN	Mil I _{OH} = -2 mA		2.4	
lozL	64		V _O = 0.4 V		-40	
lozh	Off-state output current	V _{CC} = MAX	V _O = 2.4 V		40	μΑ
los	Output short-circuit current*	V _{CC} = 5 V	V _O = 0 V	V _O = 0 V		mA
lcc	Supply current	V _{CC} = MAX. All inputs grounded. All outputs open.			150 190	mA

Switching Characteristics Over Operating Conditions (See standard test load)

OPERATING CONDITIONS	DEVICE TYPE	t _{AA}	(ns)	tEA AN ENABLE	UNI	
	8 COLUMN	TYP†	MAX	TYP†	MAX	1.6
COMMERCIAL	63S3281A	26	35	18	80 30	0.4
	63S3281	26	45	18	30	100
	53S3281B	26	40	18	35	ns
MILITARY	53S3281A	26	50	18	35	50
	53S3281	26	60	18	35	Coherry

^{*} Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

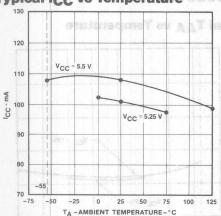
E SP Stantal Albertan or Self.

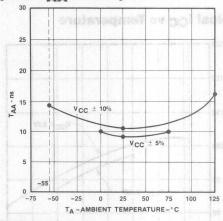
⁺ Typicals at 5.0 V VCC and 25°C TA.

53/63S080 53/63S081 63S081A

Typical Icc vs Temperature Typical TAA vs Temperature



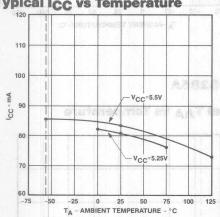


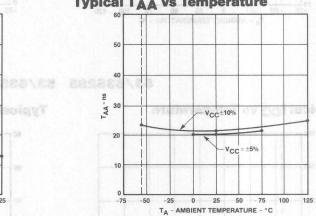


53/63S140 53/63S141/A

Typical ICC vs Temperature



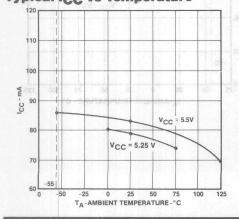


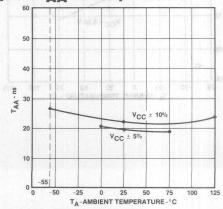


53/63\$240 53/63\$241/A

Typical Icc vs Temperature

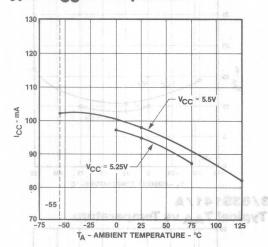
Typical TAA vs Temperature



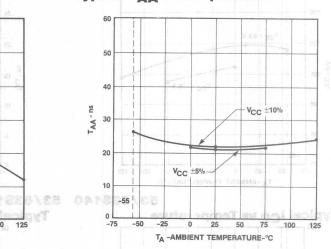


Araces recent as 53/63\$280 53/63\$281/Assegment as 53/63\$280

Typical I_{CC} vs Temperature

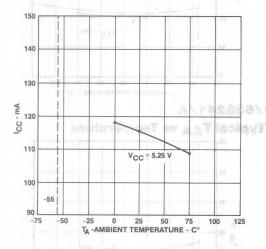


Typical TAA vs Temperature

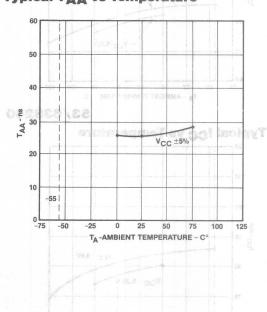


53/63S285 53/63S285A

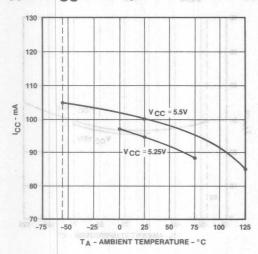
Typical Icc vs Temperature



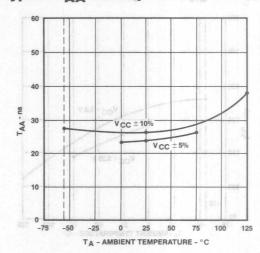
Typical TAA vs Temperature



53/63S440 53/63S441A

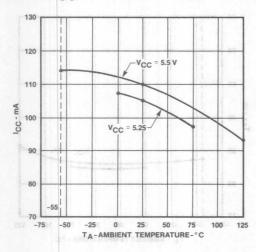


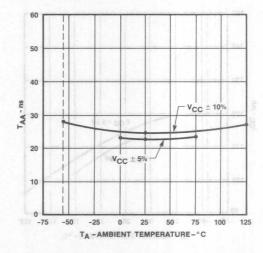
Typical I_{CC} vs Temperature Typical T_{AA} vs Temperature



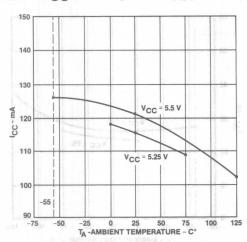
53/63\$480 53/63\$481A

Typical I_{CC} vs Temperature Typical T_{AA} vs Temperature

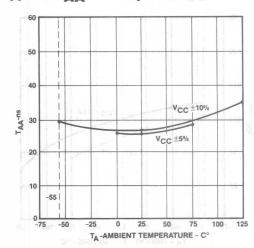




53/63S485 53/63S485A

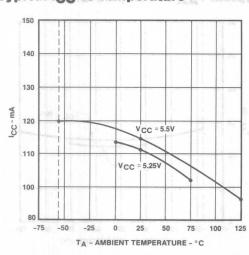


Typical I_{CC} vs Temperature Typical T_{AA} vs Temperature

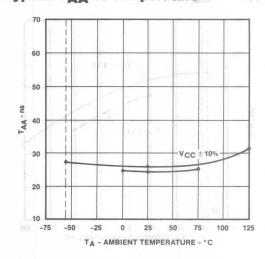


53/63\$841 53/63\$841A

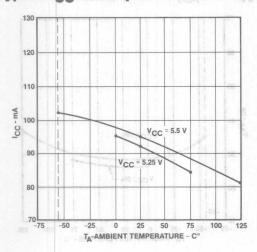
Typical I_{CC} vs Temperature



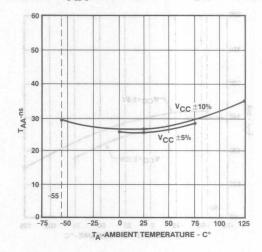
Typical TAA vs Temperature



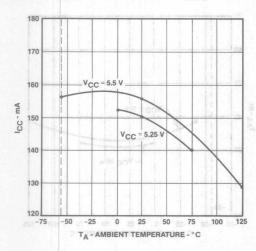
53/63S881 53/63S881A



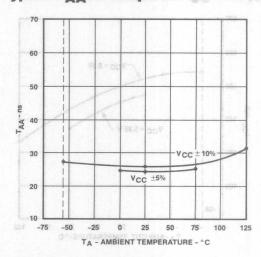
Typical I_{CC} vs Temperature Typical T_{AA} vs Temperature 1 legique



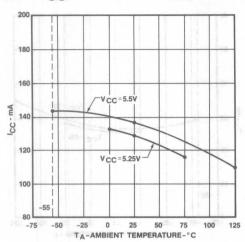
53/63S1641 53/63S1641A



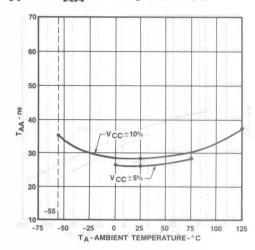
Typical I_{CC} vs Temperature Typical T_{AA} vs Temperature



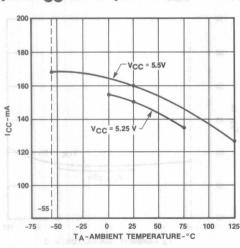
53/63S1681 53/63S1681A



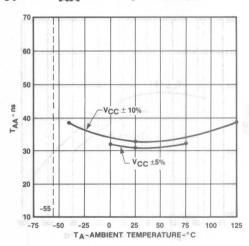
Typical I_{CC} vs Temperature Typical T_{AA} vs Temperature



53/63S3281 53/63S3281A

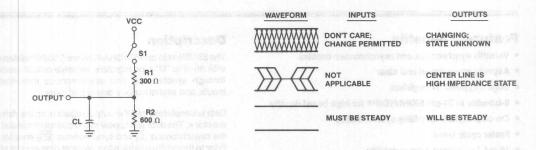


Typical I_{CC} vs Temperature Typical T_{AA} vs Temperature

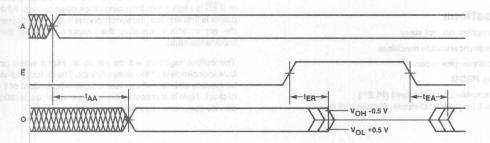


Switching Test Load

Definition of Timing Diagram



Definition of Waveforms



- 1. Input pulse amplitude 0 V to 3.0 V.
- 2. Input rise and fall times 2-5 ns from 0.8 V to 2.0 V.
- 3. Input access measured at the 1.5 V level.
- 4. t_{AA} is tested with switch S₁ closed. C_L = 30 pF and measured at 1.5 V output level.
- 5. For open collector devices, tEA and tER are measured at the 1.5 V output level with S1 closed and CL = 30 pF. S1 is open for high impedence to "1" test, and closed for high impedance to "0" test. ter is tested with CL = 5 pF. S1 is open for "1" to high impedance test, measured at VOH -0.5 V output level; S1 is closed for "0" to high impedance test measured at VOL +0.5 V output level.

High Performance 512x8 Registered PROM

53/63RA481 53/63RA481A

Features/Benefits

- Versatile synchronous and asynchronous enables
- Asynchronous preset and clear
- Edge-triggered "D" registers
- 8-bit-wide in 24-pin SKINNYDIP® for high board density
- On-chip register simplifies system timing
- Faster cycle times
- 16 mA I_{OL} output drive capability
- Reliable titanium-tungsten fuses (Ti W), with programming yields typically greater than 98%

Applications

- Microprogram control store
- State sequencers/state machines
- Next address generation
- Mapping PROM
- Programmable Logic Element (PLE™)
 9 Inputs, 8 Registered Outputs, 512 product terms

Description

The 53/63RA481 and 53/63RA481A are 512x8 Registered PROMs with on-chip "D" type registers, versatile output enable control through synchronous and asynchronous three-state enable inputs, and asynchronous preset and clear.

Data is transferred into the output registers on the rising edge of the clock. The data will appear at the outputs provided that both the asynchronous (E) and synchronous (ES) enables are Low. Prior to the positive clock edge, register data are not affected by changes in addressing or synchronous enable inputs.

Memory expansion and data control is made more flexible with synchronous and asynchronous enable inputs. Outputs may be set to the high-impedance state at any time by setting $\overline{\mathbb{E}}$ to a High or if $\overline{\mathbb{ES}}$ is High when the rising clock edge occurs. When V_{CC} power is first applied, the synchronous enable flip-flop will be in the set condition causing the outputs to be in the high-impedance state.

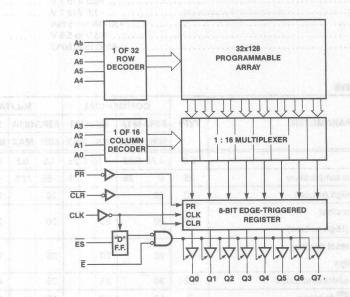
The output registers will be set to all Highs when preset is Low independent of the state of clock. The output registers will be reset to all Lows when clear is Low independent of the state of clock. Note that preset and clear are exclusive operations and cannot occur simultaneously.

Selection Guide

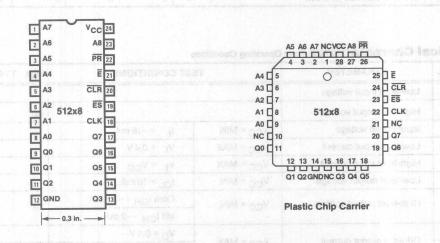
	MEMORY		KAGE	PERFORMANCE	PART	NUMBER
SIZE	ORGANIZATION	PINS			0°C to +75°C	-55°C to +125°C
416	540.0	24	NS,JS,	Enhanced	63RA481A	53RA481A
4 K	512x8	(28)	W, (NL),(L)	Standard	63RA481	53RA481

3

Block Diagram



Pin Configurations



53/63RA481 53/63RA481A

Absolute Maximum Ratings		mangaid speld
Absolute maximum natings	Operating	Programming
Supply voltage V _{CC}	0.5 V to 7 V	12 V
Input voltage	1.5 V to 7 V	
Input current	30 mA to +5 mA	
Off-state output voltage	0.5 V to 5.5 V	12 V
Storage temperature	65°C to +150°C	

Operating Conditions

			C	ОММ	ERCIA	AL.	MILITARY				
SYMBOL	PARAMETER	TYP†	63RA481A		63RA481		53RA481A		53RA481		UNIT
	SESTIMATION SESTI	1 K	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
VCC	Supply voltage	5.0	4.75	5.25	4.75	5.25	4.5	5.5	4.5	5.5	V
TA	Operating free-air temperature	25	0	75	0	75	-55	125	-55	125	°C
t _w	Width of clock (High or Low)	10	20		20	g.7.	20		20		ns
tprw	Width of preset or clear	10	20		20	- 1,5	20		20		ns
tclrw	(Low) to Output (High or Low)	10	20		20		20		20		115
tprr	Recovery from preset or clear	11	20		20		25		25		ns
tclrr	(Low) to clock High	111	20		20		25		25		115
t _s (A)	Setup time from address to clock	22	30		35		35		45		ns
t _S (ES)	Setup time from ES to clock	7	10		10		15		15		ns
t _h (A)	Hold time from address to clock	-5	0		0		0	10/19	0	Ano	ns
th (ES)	Hold time from ES to clock	-3	5		5		5		5		ns

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	The same	TEST CONDITIONS	MIN T	YP† MAX	UNIT
VIL	Low-level input voltage	a Clar	- <u>Will</u> US	4/37	0.8	V
VIH	High-level input voltage	a II sa	English College	2.0		V
VIC	Input clamp voltage	V _{CC} = MIN	I _I = -18 mA		-1.2	V
I _{IL}	Low-level input current	V _{CC} = MAX	V _I = 0.4 V	J.Fi	-0.25	mA
Iн	High-level input current	V _{CC} = MAX	V _I = V _{CC}	offi	40	μΑ
VOL	Low-level output voltage	V _{CC} = MIN	I _{OL} = 16 mA	010	0.5	V
VOH	High-level output voltage	V _{CC} = MIN	Com I _{OH} = -3.2 mA	2.4		V
OH	and the same of the same of	.00	Mil I _{OH} = -2 mA	2.4		, v
lozL	Off-state output current	V NAAV	V _O = 0.4 V		-40	
lozh	On-state output current	V _{CC} = MAX	V _O = 2.4 V	40		μΑ
los	Output short-circuit current*	V _{CC} = 5 V	V _O = 0 V	-20	-90	mA
lcc	Supply current	V _{CC} = MAX.	All inputs TTL. All outputs open.		130 180	mA

^{*} Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

 $[\]dagger$ Typicals at 5.0 V $\rm V_{CC}$ and 25°C $\rm T_A$

Switching Characteristics Over Operating Conditions and using Standard Test Load

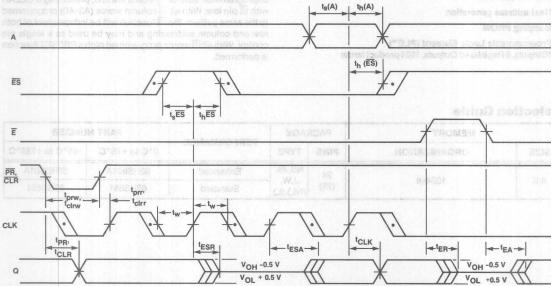
	PARAMETER	TYP†	СОММ	ERCIAL	MILI		
SYMBOL			63RA481A	63RA481	53RA481A	53RA481	UNIT
			MIN MAX	MIN MAX	MIN MAX	MIN MAX	
tCLK	Clock to output Delay	11	15	20	20	25	ns
t _{ESA}	Clock to output access time (ES)	14	25	30	30	35	ns
tESR	Clock to output recovery time (ES)	14	25	30	30	35	ns
t _{EA}	Enable to output access time (E)	10	20	30	25	s tares 64.035	ns
tER	Disable to output recovery time (E)	10	20	30	25	35	ns
tPR	Preset to output delay (PR)	15	25	25	25	30	ns
tCLR	Clear to output delay (CLR)	18	25	30	35	40	ns

[†] Typicals at 5.0 V V_{CC} and 25°C T_A.

Function Table at tourned to the new assets your total

E E	ES	CLK	PR	CLR	A8-A0	Q7-Q0	Operation	
HOU	X	X	X	X	X	Z	High-Impedance	
X	Н	1	X	X	X	Z	High-Impedance	
L	L. Carrier	X	ndv nForst 6	Н	X	Н	Preset	
nao fileo pi	Mr Gr Littele	X	H H	ini edixen	X	L	Clear	
eu oFerber	Para Torre	X	uso Ferri	nsw 19 Figuren	X	Illegal Operation		
mol Frei vou	Far Carle	CONT.	Н	Н	Α	Data	Memory Access	

Definition of Waveforms



- Notes: 1. Input pulse amplitute 0 V to 3.0 V.
 - 2. Input rise and fall times 2-5 ns from 0.8 V to 2.0 V.
 - 3. Input access measured at the 1.5 V level.
 - 4. Switch S₁ is closed, C_L = 30 pF and outputs measured at 1.5 V output level for all tests except t_{ESA} and t_{ESR}.
 - 5. t_{EA} and t_{ESA} are measured at the 1.5 V output level with C_L = 30 pF. S₁ is open for high impedance to "1" test, and closed for high impedance to "0" test.

 t_{ER} and t_{ESR} are tested with C_L = 5 pF. S₁ is open for "1" to high impedance test, measured at V_{OH} =0.5 V output level; S₁ is closed for "0" to high impedance test measured at V_{OL} +0.5 V output level.

High Performance 1024x8 Registered PROM

53/63RS881 53/63RS881A

Features/Benefits

- · Edge triggered "D" registers
- Synchronous and asynchronous enables
- Versatile 1:16 initialization words
- 8-Bit-wide in 24-pin SKINNYDIP® package for high board density
- · Simplifies system timing
- Faster cycle times
- 16 mA IOI output drive capability
- · Reliable titanium-tungsten fuses (TiW), with programming yields typically greater than 98%

Applications

- Microprogram control store
- State sequencers
- Next address generation
- Mapping PROM
- Programmable Logic Element (PLE™). 10 Inputs, 8 Registered Outputs, 1024 product terms

Description with assume fugition of Joseph

The 53/63RS881 and 53/63RS881A are 1Kx8 PROMs with onchip "D" type registers, versatile output enable control through synchronous and asynchronous enable inputs, and flexible start up sequencing through programmable initialization.

Data is transferred into the output registers on the rising edge of the clock. Provided that the asynchronous (E) and synchronous (ES) enables are low, the data will appear at the outputs. Prior to the positive clock edge, register data are not affected by changes in addressing or synchronous enable inputs.

Memory expansion and data control is made flexible with synchronous and asynchronous enable inputs. Outputs may be set to the high impedance state at any time by setting E to a high or if ES is high when the rising clock edge occurs. When VCC power is first applied the synchronous enable flip-flop will be in the set condition causing the outputs to be in the high impedance state.

The flexible initialization feature allows start up and time out sequencing with 1:16 programmable words to be loaded into the output registers. With the synchronous INITIALIZE (IS) pin low, one of the 16 column words (A3-A0) will be set in the output registers independent of the row addresses (A9-A4). The unprogrammed state of IS words are low, presenting a CLEAR with IS pin low. With all IS column words (A3-A0) programmed to the same pattern, the IS function will be independent of both row and column addressing and may be used as a single pin control. With all IS words programmed high a PRESET function is performed.

Selection Guide

MEMORY		PACKAGE			PART NUMBER	
SIZE	ORGANIZATION	PINS	TYPE	PERFORMANCE	0°C to +75°C	-55°C to +125°C
8 K	1024x8	24 (28)	NS,JS, J,W, (NL),(L)	Enhanced	63RS881A	53RS881A
				Standard	63RS881	53RS881

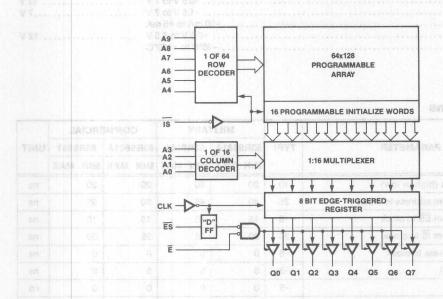
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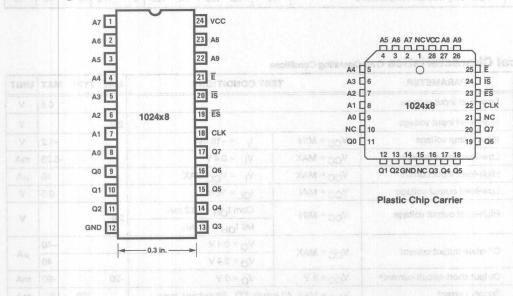
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TWX: 910-338-2376 2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2374

Block Diagram



Pin Configurations



53/63RS881 53/63RS881A

Absolute Maximum Ratings		Block Diagram
Appointe maximum matings	Operating	Programming
Supply voltage V _{CC}	0.5 V to 7 V	12 V
Input voltage	1.5 V to 7 V	7 V
Input current	30 mA to +5 mA	
Off-state output voltage	0.5 V to 5.5 V	12 V
Storage temperature		

Operating Conditions SCHOW EXLIATING BLUMMINASSONS SE

			MILI	TARY	COMM	ERCIAL	
SYMBOL	PARAMETER	TYP†	53RS881A	53RS881	63RS881A	63RS881	UNIT
	HEXELPHIT INVESTIGATION		MIN MAX	MIN MAX	MIN MAX	MIN MAX	
t _w	Width of clock (high or low)	10	20	20	20	20	ns
ts(A)	Setup time from address to clock	25	40	45	30	35	ns
ts(ES)	Setup time from ES to clock	8	15	15	15	15	ns
ts(IS)	Setup time from IS to clock	20	30	35	25	30	ns
th(A)	Hold time address to clock	-5	0	0	0	0	ns
th(ES)	Hold time (ES)	-3	5	5	5	5	ns
th(IS)	Hold time (IS)	-5	0	0	0	0	ns
VCC	Supply voltage	5	4.5 5.5	4.5 5.5	4.75 5.25	4.75 5.25	V
TA	Operating free-air temperature	25	-55 125	-55 125	0 75	0 75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	EA T	EST CONDITIONS	MIN TYP†	MAX	UNIT
VIL	Low-level input voltage	l ra	To your and the second	was the	0.8	V
V _{IH}	High-level input voltage	1 0A	22 Tal. 8 No. 21 A	2.0		٧
V _{IC}	Input clamp voltage	V _{CC} = MIN	I _I = -18 mA	The state of the s	-1.2	V
IL	Low-level input current	V _{CC} = MAX	V ₁ = 0.4 V	E.J. UA.	-0.25	mA
lн	High-level input current	V _{CC} = MAX V _I = V _{CC} MAX		E 00	40	μΑ
VOL	Low-level output voltage	V _{CC} = MIN	I _{OL} = 16 mA	10 10	0.5	V
VOH	High-level output voltage	V _{CC} = MIN Com I _{OH} = -3.2 mA		2.4		V
·OH			Mil $I_{OH} = -2 \text{ mA}$	and dep		V
lozL	Off-state output current	V MAY	V _O = 0.4 V		-40	
lozh	On-state output current	ACC - INIMA	$V_{CC} = MAX$ $V_O = 2.4 V$		40	μΑ
los	Output short-circuit current*	V _{CC} = 5 V	V _O = 0 V	-20	-90	mA
lcc	Supply current	V _{CC} = MAX. All	130	180	mA	

^{*} Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

 $[\]ensuremath{^{\dagger}}$ Typicals at 5.0 V V_CC and 25°C T_A.

 16 mA IoL output dove capability
 Reliable fittentum-lungston fuses (TW), with programming yields typically greater than 98%

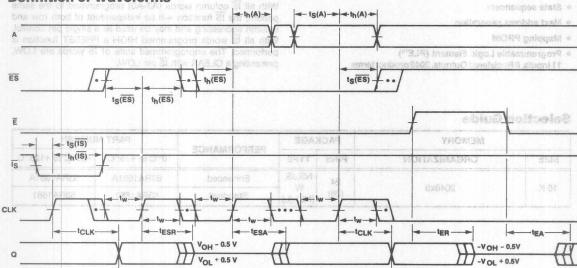
Applications

* Microprogram control diere

Switching Characteristics Over Operating Conditions and using Standard Test Load

		ТҮР	MILI	TARY	COMM	ERCIAL	UNIT
SYMBOL	PARAMETER		53RS881A	53RS881	63RS881A	63RS881	
			MIN MAX	MIN MAX	MIN MAX	MIN MAX	
^t CLK	Clock to output Delay	10	20	25	15	20	ns
tESA	Clock to output access time (ES)	ea 18 T	30	35	25,	ugillo sil 30on	ns
t _{ESR}	Clock to output recovery time (ES)	17	30	35	25	"O" hane30ht	ns
t _{EA}	Enable to output access time (E)	18	30	35	25	u 19au 81 30 alii	ns
t _{ER}	Disable to output recovery time (E)	17	30	35	25	30	ns

Definition of Waveforms



- NOTES: 1. Input pulse amplitude 0 V to 3.0 V.
 - 2. Input rise and fall times 2-5 ns from 0.8 V to 2.0 V.
 - 3. Input access measured at the 1.5 V level.
 - 4. t_{AA} is tested with switch S₁ closed. C_L = 30 pF and measured at 1.5 V output level.
 - 5. t_{EA} and t_{ESA} are measured at the 1.5 V output level with C_L = 30 pF. S₁ is open for high impedance to "1" test and closed for high impedance to "0" test.

 t_{ER} and t_{EA} are measured. C_L = 5 pF. S_1 is open for "1" to high impedance test, measured at V_{OH} -0.5 V output level; S_1 is closed for "0" to high impedance test measured at V_{OL} + 0.5 V output level.

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JJ/DJKA1081

Asynchronous Enable

1882968 A1952 P/05

Features/Benefits

- · Synchronous output enable
- Edge-triggered "D" registers
- Versatile 1:16 user programmable initialization words
- 8-bit-wide in 24-pin SKINNYDIP® for high board density
- . Simplifies system timing
- Faster cycle times
- 16 mA I_{OL} output drive capability
- · Reliable titanium-tungsten fuses (TiW), with programming yields typically greater than 98%

Applications

- Microprogram control store
- State sequencers
- Next address generation
- Mapping PROM
- Programmable Logic Element (PLE™) 11 Inputs, 8 Registered Outputs, 2048 product terms

Description

The 53/63RA1681 and 53/63RA1681A are 2Kx8 PROMs with on-chip "D"-type registers. Output enable control through an asynchronous enable input and flexible start up sequencing through programmable initialization words.

Data is transferred into the output registers on the rising edge of the clock. Provided that the asynchronous enable (E) is low, the data will appear at the outputs. Prior to the positive clock edge, register data are not affected by changes in addressing.

Memory expansion and data control is made flexible with asynchronous enable inputs. Outputs may be set to the high impedance state at any time by setting E to a HIGH.

The flexible initialization feature allows start up and time out sequencing with 1:16 programmable words to be loaded into the output registers. With the synchronous INITIALIZE (IS) pin LOW, one of the 16 column words (A3-A0) will be set in the output registers independent of the row addresses (A9-A4). With all IS column words (A3-A0) programmed to the same pattern, the IS function will be independent of both row and column addressing and may be used as a single pin control. With all IS words programmed HIGH a PRESET function is performed. The unprogrammed state of IS words are LOW, presenting a CLEAR with IS pin LOW.

Selection Guide

WELD P HELD

	MEMORY	PAC	KAGE	PEDEODMANOE	PART	NUMBER
SIZE	ORGANIZATION	PINS	TYPE	PERFORMANCE	0°C to +75°C	-55°C to +125°C
4016	2010.0	24	NS,JS,	Enhanced	63RA1681A	53RA1681A
16 K	2048x8	(28)	W, (NL),(L)	Standard	63RA1681	53RA1681

Est and rest measured at the 1,5 V output level with C = 30 of S , is open for high impactures to 11 test and circuit for migh

4- (A) 1 - - - (A) 2 - -

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TWX: 910-338-2376

 $V\otimes B = {}_{\textstyle {\rm HO}} V$

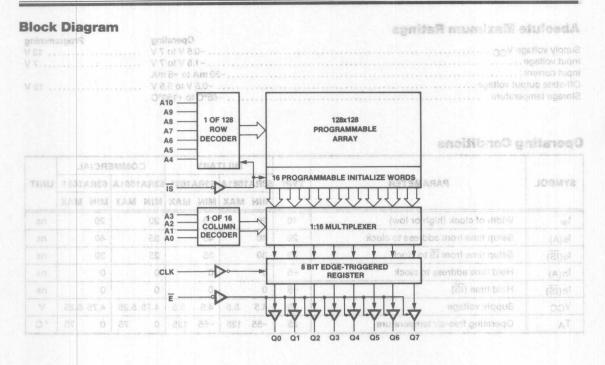
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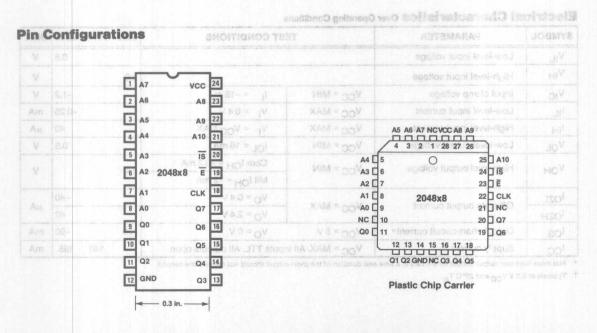
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3-46





53/63RA1681 53/63RA1681A

Absolute Maximum Ratings	
Operatin	g Programming
Supply voltage V _{CC}	V 12 V
Input voltage1.5 V to 7	V7 V
Input current	A
Off-state output voltage0.5 V to 5.5	V 12 V
Storage temperature	

Operating Conditions

		TYP†	MIL	ITARY	COMMI		
SYMBOL	PARAMETER		53RA1681	A 53RA1681	63RA1681A	63RA1681	UNIT
	<u> </u>		MIN MA	MIN MAX	MIN MAX	MIN MAX	
t _W	Width of clock (high or low)	10	20	20	20	20	ns
ts(A)	Setup time from address to clock	28	40	45	35	40	ns
ts(IS)	Setup time from IS to clock	20	30	35	25	30	ns
^t h(A)	Hold time address to clock	-5	0	0	0	0	ns
th(IS)	Hold time (IS)	-5	0	0	0	0	ns
VCC	Supply voltage	5	4.5 5.5	4.5 5.5	4.75 5.25	4.75 5.25	V
TA	Operating free-air temperature	25	-55 125	-55 125	0 75	0 75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	T	EST CONDITIONS	MIN	TYP†	MAX	UNIT
V _{IL}	Low-level input voltage				Ì	0.8	٧
V _{IH}	High-level input voltage		Section of the sectio	2.0			V
VIC	Input clamp voltage	V _{CC} = MIN	I _I = -18 mA	Sales Sales		-1.2	V
IIL	Low-level input current	V _{CC} = MAX	V _I = 0.4 V			-0.25	mA
Iн	High-level input current	V _{CC} = MAX	V _I = V _{CC} MAX			40	μΑ
VOL	Low-level output voltage	V _{CC} = MIN	I _{OL} = 16 mA	Secret Secret	788	0.5	V
VOH	High-level output voltage	V _{CC} = MIN	Com I _{OH} = -3.2 mA				V
·OH	a fles		Mil I _{OH} = -2 mA	2.4			
lozL	Off state output surrent	14 - MAY	V _O = 0.4 V	1 Intel		-40	
IOZH	Off-state output current	V _{CC} = MAX	V _O = 2.4 V			40	μΑ
los	Output short-circuit current*	V _{CC} = 5 V	V _O = 0 V	-20		-90	mA
lcc	Supply current	V _{CC} = MAX. All	inputs TTL. All outputs open.	TO SEL	140	185	mA

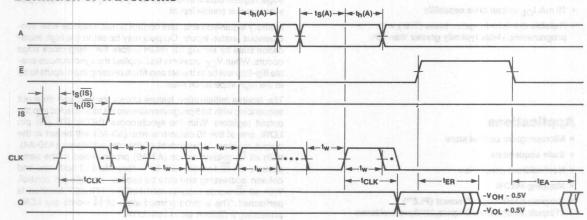
^{*} Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. Typicals at 5.0 V V_{CC} and 25°C T_A.

Switching Characteristics Over Operating Conditions and using Standard Test Load

			MILI	TARY	COMM	1219	
SYMBOL PARAMETER	PARAMETER	TYP	53RA1681A	53RA1681	63RA1681A	63RA1681	UNIT
		- Description	MIN MAX	MIN MAX	MIN MAX	MIN MAX	
tCLK	Clock to output Delay	10	20	25	15	20	ns
t _{EA}	Enable to output access time (E)	15	30	35	25	30	ns
tER	Disable to output recovery time (E)	15	30	35	25	30	ns

[†] Typicals at 5.0 V V_{CC} and 25°C T_A.

Definition of Waveforms



Notes: 1. Input pulse amplitute 0 V to 3.0 V.

- 2. Input rise and fall times 2-5 ns from 0.8 V to 2.0 V.
- 3. Input access measured at the 1.5 V level.
- 4. Switch S₁ is closed. C_L = 30 pF and outputs measured at 1.5 V output level for all tests except t_{ESA} and t_{ESR}.
- 5. t_{EA} and t_{ESA} are measured at the 1.5 V output level with C_L = 30 pF. S₁ is open for high impedance to "1" test, and closed for high impedance to "0" test.

teR and teSR are tested with CL = 5 pF. S₁ is open for "1" to high impedance test, measured at V_{OH} -0.5 V output level; S₁ is closed for "0" to high impedance test measured at V_{OL} +0.5 V output level.

2048x8 **Registered PROM** with Synchronous Enable

53/63RS1681 53/63RS1681A

Features/Benefits

- · Synchronous output enable
- Edge-triggered "D" registers
- Versatile 1:16 user programmable initialization words
- · 8-bit-wide in 24-pin SKINNYDIP® for high board density
- · Simplifies system timing
- Faster cycle times
- 16 mA I_{OL} output drive capability
- · Reliable titanium-tungsten fuses (TiW), with programming yields typically greater than 98%

Applications

- Microprogram control store
- State sequencers
- Next address generation
- Mapping PROM
- Programmable Logic Element (PLE™) 11 Inputs, 8 Registered Outputs, 2048 product terms

Description

The 53/63RS1681 and 53/63RS1681A are 2Kx8 PROMs with on-chip "D" type registers, versatile output enable control through synchronous enable inputs and flexible start up sequencing through programmable initialization words.

Data is transferred into the output registers on the rising edge of the clock. Provided that the synchronous (ES) enable is LOW, the data will appear at the outputs. Prior to the positive clock edge, register data are not affected by changes in addressing or synchronous enable inputs.

Memory expansion and data control is made flexible with synchronous enable inputs. Outputs may be set to the high impedance state by setting ES HIGH before the rising clock edge occurs. When V_{CC} power is first applied the synchronous enable flip-flop will be in the set condition causing the outputs to be in the high impedance state.

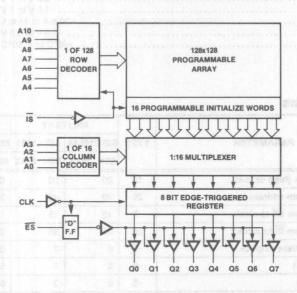
The flexible initialization feature allows start up and time out sequencing with 1:16 programmable words to be loaded into the output registers. With the synchronous INITIALIZE (IS) pin LOW, one of the 16 column words (A3-A0) will be set in the output registers independent of the row addresses (A10-A4). With all IS column words (A3-A0) programmed to the same pattern, the IS function will be independent of both row and column addressing and may be used as a single pin control. With all IS words programmed HIGH a PRESET function is performed. The unprogrammed state of IS words are LOW, presenting a CLEAR with IS pin LOW.

Selection Guide

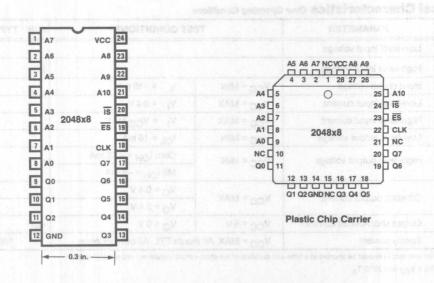
	MEMORY		KAGE	DEDECRIMANCE	PART	NUMBER
SIZE	ORGANIZATION	PINS	TYPE	PERFORMANCE	0°C to +75°C	-55°C to +125°C
1016	0040.0	24	24 NS,JS,	Enhanced	63RS1681A	53RS1681A
16 K	K 2048x8 (28) W, (NL),(L)	Standard	63RS1681	53RS1681		

3

Block Diagram



Pin Configurations



53/63RS1681 53/63RS1681A

Absolute Maximum Ratings		
	Operating	Programming
Supply voltage V _{CC}	0.5 V to 7 V	12 V
Input voltage	1.5 V to 7 V	7 V
Input current	30 mA to +5 mA	
Off-state output voltage	0.5 V to 5.5 V	12 V
Storage temperature	65°C to +150°C	

Operating Conditions

		MI	MILITARY				COMMERCIAL				
SYMBOL	PARAMETER	TYP†	53RS1681A		53RS1681		63RS1681A		63RS1681		UNIT
	TOTAL AREA: YESTLESSESS		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _W	Width of clock (high or low)	10	20	- ylavia	20		20		20		ns
ts(A)	Setup time from address to clock	28	40		45	- 11-	35		40		ns
ts(ES)	Setup time from ES to clock	7	15		15		15		15		ns
ts(IS)	Setup time from IS to clock	20	30		35	- 08	25		30		ns
^t h(A)	Hold time address to clock	-5	0		0		0		0		ns
th(ES)	Hold time (ES)	-3	5		5		5		5		ns
th(IS)	Hold time (IS)	-5	0		0		0		0		ns
Vcc	Supply voltage	5	4.5	5.5	4.5	5.5	4.75	5.25	4.75	5.25	V
TA	Operating free-air temperature	25	-55	125	-55	125	0	75	0	75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	Т	EST CONDITIONS	MIN 1	TYP† MAX	UNIT
VIL	Low-level input voltage			1.154	0.8	V
VIH	High-level input voltage		£537	2.0		V
VIC	Input clamp voltage	V _{CC} = MIN	I _I = -18 mA	11 1-1	-1.2	V
IIL	Low-level input current	V _{CC} = MAX	V _I = 0.4 V	I in	-0.25	mA
Iн	High-level input current	V _{CC} = MAX	VI = VCC MAX	4	40	μΑ
VOL	Low-level output voltage	V _{CC} = MIN	I _{OL} = 16 mA	Jacob L.	0.5	V
V _{OH}	High-level output voltage	V _{CC} = MIN	Com I _{OH} = -3.2 mA	2.4		V
OH	and the same at the same		Mil I _{OH} = -2 mA	2.4		
lozL	Off-state output current	V MAY	V _O = 0.4 V	les era	-40	^
IOZH	On-state output current	V _{CC} = MAX	V _O = 2.4 V	CONTRACT CON	40	μΑ
los	Output short-circuit current*	V _{CC} = 5 V	V _O = 0 V	-20	-90	mA
lcc	Supply current	V _{CC} = MAX. All inputs TTL. All outputs open.			140 185	mA

^{*} Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

 $[\]dagger$ Typicals at 5.0 V V_{CC} and 25°C T_A.

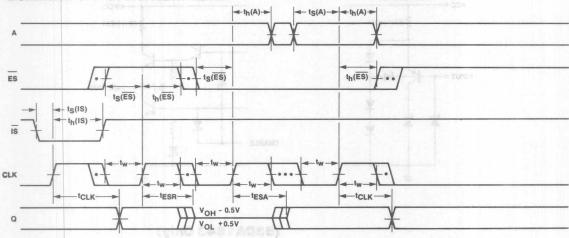
3

Switching Characteristics Over Operating Conditions and using Standard Test Load

SYMBOL			MILI	TARY	СОММ		
	PARAMETER	TYP† 53RS1681A 53RS1681		63RS1681A	63RS1681	UNIT	
	GENERAL SERVICE (TETT	O CONTO	MIN MAX	MIN MAX	MIN MAX	MIN MAX	ns
tCLK	Clock to output Delay	10	20	25	15	20	ns
tesa and	Clock to output access time (ES)	15	30	35	25	30	ns
tESR	Clock to output recovery time (ES)	15	30	35	25	30	ns

[†] Typicals at 5.0 V V_{CC} and 25°C T_A.

Definition of Waveforms

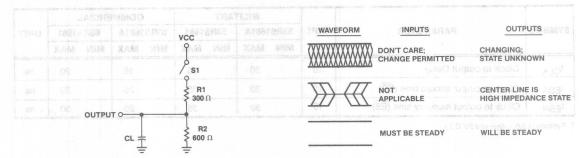


- Notes: 1. Input pulse amplitute 0 V to 3.0 V.
 - 2. Input rise and fall times 2-5 ns from 0.8 V to 2.0 V.
 - 3. Input access measured at the 1.5 V level.
 - 4. Switch S₁ is closed. C_L = 30 pF and outputs measured at 1.5 V output level for all tests except t_{ESA} and t_{ESR}.
 - 5. t_{EA} and t_{ESA} are measured at the 1.5 V output level with C_L = 30 pF. S₁ is open for high impedance to "1" test, and closed for high impedance to "0" test.

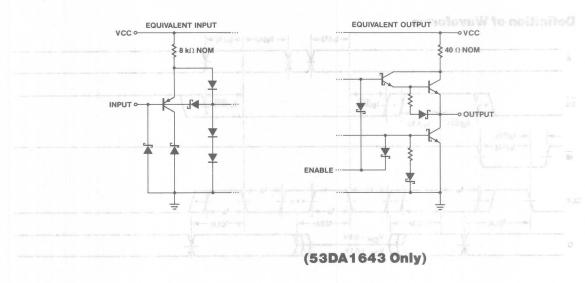
 t_{ER} and t_{ESR} are tested with C_L = 5 pF. S_1 is open for "1" to high impedance test, measured at V_{OH} =0.5 V output level; S_1 is closed for "0" to high impedance test measured at V_{OL} +0.5 V output level.

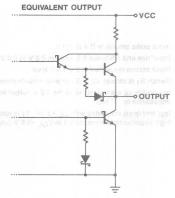
Switching Test Load

Definition of Timing Diagrams



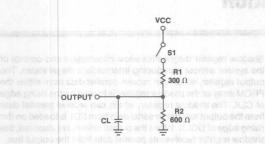
Schematic of Inputs and Outputs

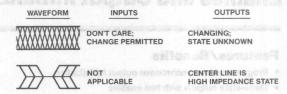




Switching Test Load

Definition of Timing Diagrams

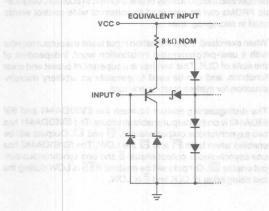


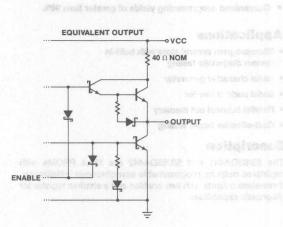


MUST BE STEADY WILL BE STEADY

e 24-514 BICHAPURE * package awas space

Schematic of Inputs and Outputs





| NEWORN | PACKAGE | PART NUMBER NUMBER | PART NUMBER NUMBER | PART NUMBER NUMBER NUMBER NUMBER | PA

2

1024x4 Diagnostic Registered PROM

53/63DA441 53/63DA442

Enables and Output Initialization

Features/Benefits

- Programmable asynchronous output initialization
- . Three-state outputs with two enables
- · Provides system diagnostic testing with system controllability and observability
- · Shadow register eliminates shifting hazards
- · Edge-triggered "D" registers simplifies system timing
- · Cascadable for wide control words used in microprogramming
- 24-pin SKINNYDIP® package saves space
- 24-mA output drive capability
- · Replaces embedded diagnostic code
- . Guaranteed programming yields of greater than 98%

Applications

- Microprogram control store with built-in system diagnostic testing
- Serial character generator
- Serial code converter
- Parallel in/serial out memory
- Cost-effective board testing

Description

The 53/63DA441 and 53/63DA442 are 1Kx4 PROMs with registered outputs, programmable asynchronous initialization, three-state outputs with two enables and a shadow register for diagnostic capabilities.

Shadow register diagnostics allow observation and control of the system without introducing intermediate illegal states. The output register, which can receive parallel data from either the PROM array or the shadow register is loaded on the rising edge of CLK. The shadow register, which can receive parallel data from the output register or serial data from SDI, is loaded on the rising edge of DCLK. When the output drivers are disabled, the shadow register receives its parallel data from the output bus.

During diagnostics, data loaded into the output register from the PROM array can be parallel-loaded into the shadow register and serially shifted out through SDO, allowing observation of the system. Similarly, diagnostic data can be serially shifted into the shadow register through SDI, and parallel-loaded into the output register, allowing control and test scanning to be imposed on the system. Since the output register and the shadow register are loaded by different input signals, they can be operated independently of one another. In addition, diagnostic PROMs can be cascaded to construct wide control words used in microprogramming.

When exercised, the initialization input loads the output register with a user-programmable initialization word, independent of the state of CLK. This features is a superset of preset and clear functions, and can be used to generate an arbitrary microinstruction for system reset or interrupt.

The distinguishing feature between the 53/63DA441 and 53/ 63DA442 is on the output enable structure. The 53/63DA441 has two asynchronous output enables, $\overline{E1}$ and $\overline{E2}.$ Outputs will be enabled when both E1 and E2 are LOW. The 53/63DA442 has one asynchronous output enable E and one synchronous output enable ES. Outputs will be enabled if ES is LOW during the last rising edge of CLK and E is LOW.

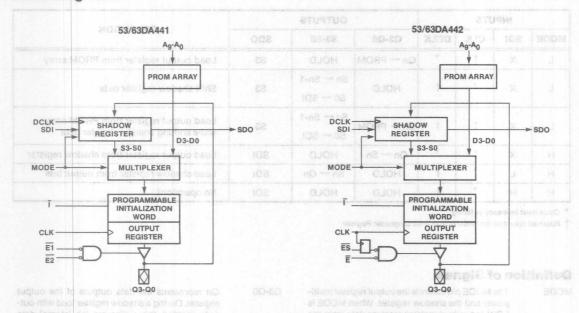
Selection Guide

MEMORY			PAC	KAGE	PART NUMBER		
SIZE	ORGANIZATION	OPTIONS	PINS	TYPE	MILITARY	COMMERCIAL	
	Two asynchronous enables		10.10.14	53DA441	63DA441		
4 K	1024x4	One synchronous enable, one asynchronous enable	(28)	NS,JS,W, (NL),(L)	53DA442	63DA442	

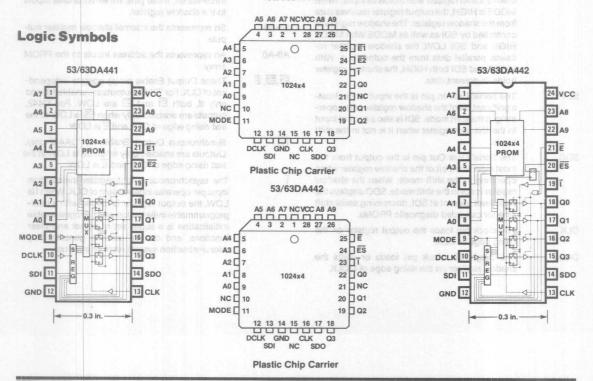


3

Block Diagrams



53/63DA441



INPUTS					OUTPUTS		OPERATION
MODE	SDI	CLK	DCLK	Q3-Q0	S3-S0	SDO	OPERATION
L	Х	1	*	Qn ← PROM	HOLD	S3	Load output register from PROM array
L	X	*	†	HOLD	Sn ← Sn-1 S0 ← SDI	S3	Shift shadow register data
Lygs	X	†	1 1	Qn ← PROM	Sn ← Sn-1 S0 ← SDI	S3	Load output register from PROM array while shifting shadow register data
Н	X	1	*	Qn ← Sn	HOLD	SDI	Load output register from shadow register
Н	L	*	1	HOLD	Sn ← Qn	SDI	Load shadow register from output bus
Н	Н	*	1	HOLD	HOLD	SDI	No operation†

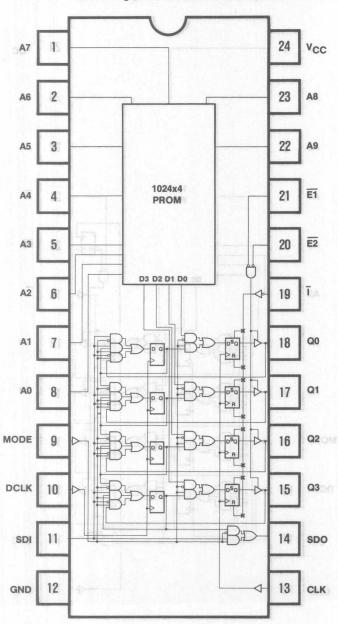
^{*} Clock must be steady or falling.

Defin	ition of Signals		
MODE	The MODE pin controls the output register multi- plexer and the shadow register. When MODE is LOW, the output register receives data from the PROM array and the shadow register is config- ured as a shift register with SDI as its input. When MODE is HIGH, the output register receives data	Q3-Q0	On represents the data outputs of the output register. During a shadow register load with outputs enabled, these pins are the internal data inputs to the shadow register. With the outputs three-stated, these pins are external data inputs to the shadow register.
	from the shadow register. The shadow register is controlled by SDI as well as MODE With MODE HIGH and SDI LOW, the shadow register re-	S3-S0	Sn represents the internal shadow register outputs.
	ceives parallel data from the output bus. With MODE and SDI both HIGH, the shadow register	A9-A0	An represents the address inputs to the PROM array.
	holds its present data.	Ē1,Ē2, Ē	These Output Enable pin(s) operate independ-
SDI	The Serial Data In pin is the input to the least- significant bit of the shadow register when oper- ating in the shift mode. SDI is also a control input to the shadow register when it is not in the shift		ent of CLK. For 'D441, outputs are enabled if, and only if, both $\overline{E1}$ and $\overline{E2}$ are LOW. For 'D442, outputs are enabled only when $\overline{E5}$ is LOW at the last rising edge of CLK and \overline{E} is LOW.
	mode.	ES	Synchronous Output Enable for 'DA442 only.
SDO	The Serial Data Out pin is the output from the most significant bit of the shadow register when		Outputs are enabled only when \overline{ES} is LOW at the last rising edge of CLK and \overline{E} is LOW.
	operating in the shift mode. When the shadow register is not in the shift mode, SDO displays the logic level present at SDI, decreasing serial shift time for cascaded diagnostic PROMs.	ACESIGE VINTA SA PA	The asynchronous output register initialization input pin operates independent of CLK. When I is LOW, the output register is loaded with a user-programmable initialization word. Programmable
CLK	The clock pin loads the output register on the rising edge of CLK.		initialization is a super set of preset and clear functions, and can be used to generate any
DCLK	The diagnostic clock pin loads or shifts the shadow register on the rising edge of DCLK.		microinstruction system reset or interrupt.

[†] Reserved operation for SN54/74S818 8-Bit Diagnostic Register.

Logic Diagram

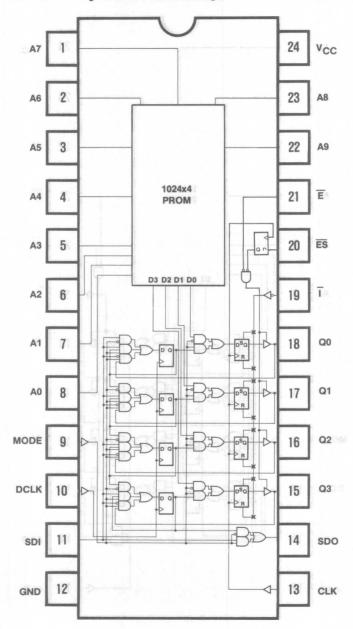
53/63DA441
1024x4 Diagnostic PROM
with Asynchronous Initialization
and Asynchronous Enables



3

Logic Diagram

53/63DA442
1024x4 Diagnostic PROM
with Asynchronous Initialization
and Both Asynchronous and Synchronous Enables



Absolute Maximum Ratings		
	Operating	Programming
Supply voltage V _{CC}	0.5 V to 7 V	12 V
Input voltage	1.5 V to 7 V	7 V
Input current	30 mA to +5 mA	
Off-state output voltage		
Storage temperature	65° to +150° C	

Operating Conditions

SYMBOL	PARAMETER	MIN	TYP	RY MAX	COMMER MIN TYP		CIAL	UNIT	
Vcc	Supply voltage	4.5	5	5.5	4.75	5	5.25	V	
T _A	Operating free-air temperature	-55	25	125	0	25	75	°C	
tw sc	Width of CLK (HIGH or LOW)	25	10	disalb b	20	10	, 1	ns	
t _{su}	Setup time from address to CLK	45	25	Idane I	35	25		ns	
th	Hold time for CLK	0	-15		0	-15	n Calana	ns	
twd	Width of DCLK (HIGH or LOW)	35	15		25	15		ns	
tsud	Setup time from control inputs (SDI, MODE) to CLK, DCLK	50	20		40	20		ns	
thd	Hold time for DCLK	0	-5		0	-5		ns	
$t_S(\overline{ES})$	Setup time from ES to CLK ('DA442 only)	20	10	to let	15	10	relat	ns	
t _h (ES)	Hold time (ES) ('DA442 only)	5	0		5	0		ns	
tiw	Initialization pulse width (LOW)	25	10	Apple .	20	10	AAAAA	ns	
tir	Initialization recovery time	45	30	2-	40	30	AND NO.	ns	

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	T	EST CONDITIONS	MIN T	YP† MAX	UNIT
VIL	Low-level input voltage				0.8	V
VIH	High-level input voltage			2.0		V
V _{IC}	Input clamp voltage	V _{CC} = MIN	I _I = -18 mA	SLATE	-1.2	V
IIL	Low-level input current	V _{CC} = MAX V _I = 0.4 V			-0.25	mA
IH	High-level input current	V _{CC} = MAX	V _I = V _{CC} MAX		40	μΑ
V _{OL}	Low-level output voltage	VCC = MIN	Com I _{OL} = 24 mA		0.5	V
	zon iovor output voltage	(ROJ = gloubil) dalls	Mil I _{OL} = 16 mA		0.0	
Vон	High-level output voltage	V _{CC} = MIN	Com I _{OH} = -3.2 mA			V
TOH	riigir lever output voitage	·CC ·······	Mil I _{OH} = -2 mA	2.4		V
IOZL	Off state output surrent	V - MAN	V _O = 0.4 V		-100	
lozh	Off-state output current	V _{CC} = MAX	V _O = 2.4 V		40	μΑ
los	Output short-circuit current*	V _{CC} = MAX	V _O = 0 V	-20	-90	mA
¹cc	Supply current	V _{CC} = MAX. All inputs TTL. All outputs open.			130 180	mA

^{*} Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

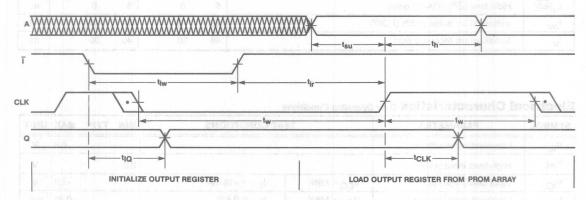
[†] Typicals at 5.0 V V_{CC} and 25°C T_A.

Switching Characteristics Over Operating Conditions and Using Standard Test Load

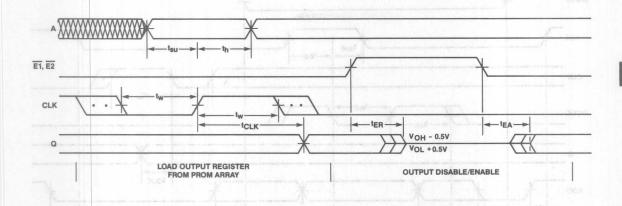
SYMBOL	PARAMETER	MIN .	LITAF TYP†			MMER TYP†	10000	UNIT
tCLK	CLK to output		11	25		11	18	ns
t _{ER}	Disable time		14	30		14	25	ns
^t EA	Enable time		16	30		16	25	ns
†MAXD	Maximum diagnostic clock frequency	7	20	pero	10	20	antis	MHz
tDS	DCLK to SDO delay (MODE = LOW)	MAAAAA	17	35		17	30	ns
tss	SDI to SDO delay (MODE = HIGH)		16	30		16	25	ns
tMS	MODE to SDO delay		14	30	milite)	14	25	ns
t _{IQ}	Initialization to output delay	87011	22	35	nd Bury	22	30	ns
t _{ESR}	CLK to output disable time ('DA442 only)	(3)10	22	35	13.8	22	30	ns
t _{ESA}	CLK to output enable time ('DA442 only)	-NUS	15	35	ini enti	15	30	ns

[†] Typicals at 5.0 V VCC and 25° C TA.

Definition of Waveforms

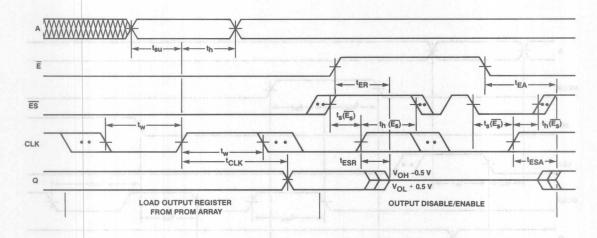


Normal PROM Operation (Mode = LOW)
(for both 53/63DA441 and 53/63DA442 with outputs enabled)

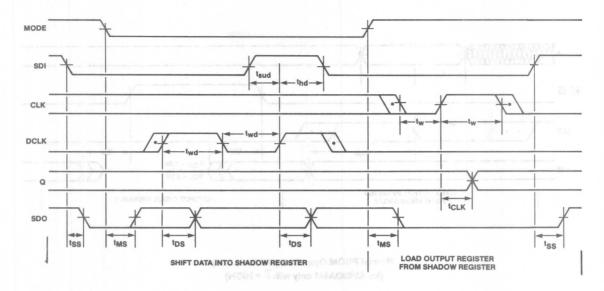


Normal PROM Operation (Mode = LOW)

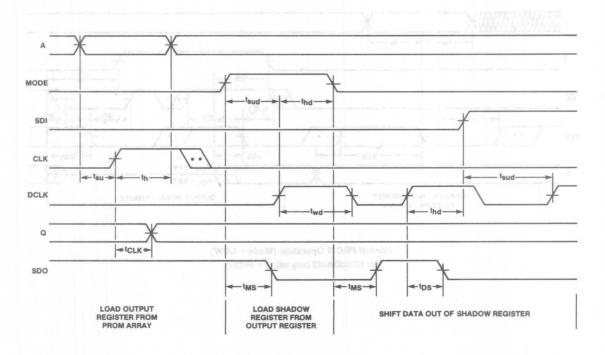
(for 53/63DA441 only with I = HIGH)



Normal PROM Operation (Mode = LOW) (for 53/63DA442 only with \overline{I} = HIGH)



SYSTEM CONTROL



SYSTEM OBSERVATION

2048x4 Diagnostic **Registered PROM**

53DA841 63DA841

with Asynchronous Enable and Output Initialization

Features/Benefits

- Asynchronous output enable
- Programmable asynchronous output initialization
- · Provides system diagnostic testing with system controllability and observability
- · Shadow register eliminates shifting hazards
- . Edge-triggered "D" registers simplifies system timing
- · Cascadable for wide control words used in microprogramming
- 24-pin SKINNYDIP® saves space
- · Reliable titanium-tungsten fuses (TiW), with programming yields typically greater than 98%
- 24-mA output drive capability
- Replaces embedded diagnostic code

Applications

- · Microprogram control store with built-in system diagnostic testing
- Serial character generator
- Serial code converter
- Parallel in/serial out memory
- · Cost-effective board testing

Description

The 53/63DA841 is a 2Kx4 PROM with registered three-state outputs, programmable asynchronous initialization and a shadow register for diagnostic capabilities. Shadow register diagnostics allow observation and control of the system without introducing intermediate illegal states. The output register, which can receive parallel data from either the PROM array or the shadow register is loaded on the rising edge of CLK. The shadow register, which can receive parallel data from the output register or serial data from SDI, is loaded on the rising edge of DCLK. When the output drivers are disabled, the shadow register receives its parallel data from the output bus. During diagnostics, data loaded into the output register from the PROM array can be parallel-loaded into the shadow register and serially shifted out through SDO, allowing observation of the system. Similarly, diagnostic data can be serially shifted into the shadow register through SDI, and parallel-loaded into the output register, allowing control and test scanning to be imposed on the system. Since the output register and the shadow register are loaded by different input signals, they can be operated independently of one another. In addition, diagnostic PROMs can be cascaded to construct wide control words used in microprogramming. When exercised, the Initialization input loads the register with a userprogrammable initialization word, independent of the state of CLK. This feature is a superset of preset and clear functions, and can be used to generate an arbitrary microinstruction for system reset or interrupt.

Selection Guide

	MEMORY	PAC	KAGE	PART NUMBER		
SIZE	ORGANIZATION	PINS	TYPE	0°C to +75°C	-55°C to +125°C	
8 K	2048x4	24 (28)	NS,JS, W, (NL),(L)	63DA841	53DA841	

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TWX: 910-338-2376 2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2374





Block Diagram

assets. The autout register, which can

GND 12

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e or good register from the PROMerray can be per-

er is loaded on the naing edge of CLIC. The shall we regis-men can reclaive parallel data from the output register or

different input signals, they can be operated independently of one another, in addition, diagnostic PROMs can be cascaded to Pin Configurations

can be used to generate an arbitrary microinstruction for system

Registered PROM with Asynchronous Enth, and Output Initialization PROM ARRAY Description AJJO ZKx4 PROM with registered three-state SHADOW

REGISTER

MODE-

S3-S0

MULTIPLEXER

PROGRAMMABLE INITIALIZATION WORD

OUTPUT

REGISTER

- Programmable asystemonous below initiality
- Provides system diagnostic testing with syste

→ SDO

- Shadow register eliminates ontifing hazards
- · Cascadalyle for wide control words used in
 - > 24-oin SKINN (DIPP saves space
- yleids typically graster from 36%

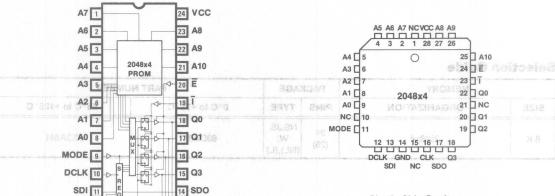
 - · Repisces embedded diagnostic code

allel-loaded into the shadow register and sensity at iffed out Q3-Q0 ing control and test scanning to be imposed on the system

D3-D0

Plastic Chip Carrier

- - · Cost-effective beard testing



13 CLK

mergalQ siged

	INPUTS				OUTPUTS		OPERATION
MODE	SDI	SDI CLK DCLK Q3-Q0 S3-S0 SD		SDO	OPERATION		
L	X	1	*	Qn ← PROM	HOLD	S3	Load output register from PROM array
	X	*		HOLD	Sn ← Sn-1	00	Objet abada was istandata
_	^			HOLD	S0 ← SDI	-S3	Shift shadow register data
L	х	t	29v	Qn ← PROM	Sn ← Sn-1 S0 ← SDI	S3	Load output register from PROM array while shifting shadow register data
Н	X	1	*	Qn - Sn	HOLD	SDI	Load output register from shadow register
Н	L	*	7	HOLD	Sn ← Qn	SDI	Load shadow register from output bus
Н	Н	*	t	HOLD	HOLD	SDI	No operation †

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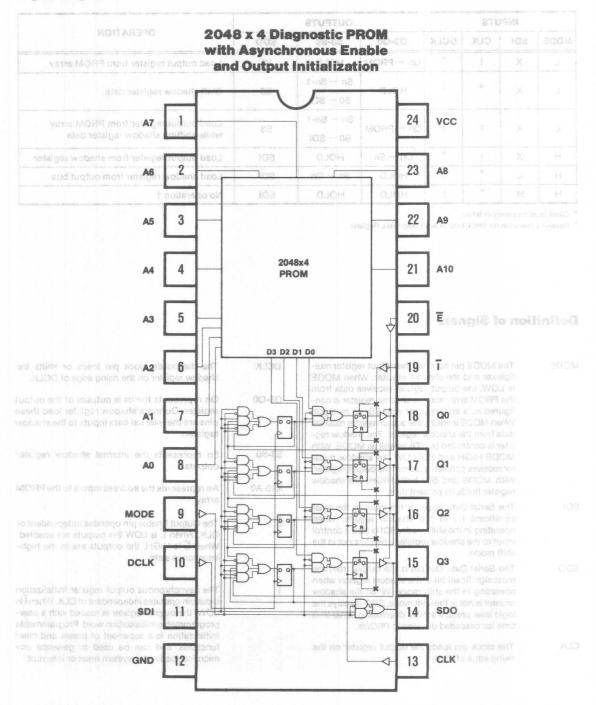
Definition of Signals

	DD (messes of	FO SO 60	The communication of the commu
MODE	The MODE pin controls the output register mul- tiplexer and the shadow register. When MODE is LOW, the output register receives data from	DCLK	The diagnostic clock pin loads or shifts the shadow register on the rising edge of DCLK.
	the PROM array and the shadow register is configured as a shift register with SDI as its input. When MODE is HIGH, the output register receives data from the shadow register. The shadow register is controlled by SDI as well as MODE. With	Q3-Q0 [] CE	On represents the data outputs of the output register. During a shadow register load these pins are the internal data inputs to the shadow register.
	MODE HIGH and SDI LOW, the shadow register receives parallel data from the output register. With MODE and SDI both HIGH, the shadow	\$3-\$0 3-\$0	Sn represents the internal shadow register outputs.
	register holds its present data.	A10-A0	An represents the address inputs to the PROM array.
SDI	The Serial Data In pin is the input to the least significant bit of the shadow register when operating in the shift mode. SDI is also a control input to the shadow register when it is not in the shift mode.		The Output Enable pin operates independent of CLK. When E is LOW the outputs are enabled. When E is HIGH, the outputs are in the high-impedance state.
SDO	The Serial Data Out pin is the output from the most significant bit of the shadow register when operating in the shift mode. When the shadow register is not in the shift mode, SDO displays the logic level present at SDI, decreasing serial shift time for cascaded diagnostic PROMs.		The asynchronous output register initialization input pin operates independent of CLK. When I is LOW, the output register is loaded with a user-programmable initialization word. Programmable initialization is a super-set of preset and clear
CLK	The clock pin loads the output register on the rising edge of CLK.		functions, and can be used to generate any microinstruction for system reset or interrupt.
			Education and control and T

 ^{*} Clock must be steady or falling.
 * Reserved operation for SN54/74S818 8-Bit Diagnostic Register.

Function Table

Logic Diagram





Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN TYP [†] MAX	COMMERCIAL MIN TYP† MAX	UNIT
Vcc	Supply voltage	4.5 5 5.5	4.75 5 5.25	V
TA	Operating free-air temperature	-55 25 125	0 25 75	°C
t _w	Width of CLK (HIGH or LOW)	25 10	20 10	ns
t _{su}	Set up time from address to CLK	45 27	40 27	ns
th	Hold time for CLK	0 -15	0 -15	ns
twd	Width of DCLK (HIGH or LOW)	45 15	40 15	ns
t _{sud}	Set up time from control inputs (SDI, MODE) to CLK, DCLK	50 20	45 20	ns
^t hd	Hold time for DCLK	0 -5	0 -5	ns
tiw	Initialization pulse width (LOW)	25 10	20 10	ns
t _{ir}	Initialization recovery time	45 30	40 30	ns

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TES	T CONDITIONS	MIN TYP†	MAX	UNIT
VIL	Low-level input voltage				0.8	V
V _{IH}	High-level input voltage			2.0		V
VIC	Input clamp voltage	V _{CC} = MIN	I _I = -18 mA		-1.2	V
IL	Low-level input current	V _{CC} = MAX	V _I = 0.4 V	and the same of the same	-0.25	mA
<u>Ч</u> н	High-level input current	V _{CC} = MAX	V _I = V _{CC} MAX		40	μΑ
VOL	Low-level output voltage	V _{CC} = MIN	Com I _{OL} = 24 mA	La Jane	0.5	V
·OL	NA vennov/77		Mil I _{OL} = 16 mA		0.5	·
VOH	High-level output voltage	V _{CC} = MIN	Com I _{OH} = -3.2 mA	2.4		V
*OH	alasama.eema casam	Navana a	Mil I _{OH} = -2 mA	OMILIAT W		V
lozL	0"	V 144V	V _O = 0.4 V		-100	^
lozh	Off-state output current	V _{CC} = MAX	V _O = 2.4 V		40	μΑ
los	Output short-circuit current*	V _{CC} = 5 V	V _O = 0 V	-20	-90	mA
lcc	Supply current	V _{CC} = MAX. All inp	outs TTL. All outputs open.	140	185	mA

^{*} Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

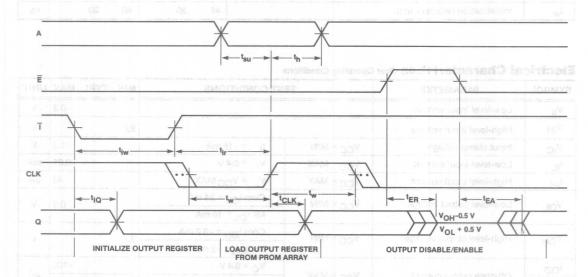
[†] Typicals at 5.0 V V_{CC} and 25°C T_A.

Switching Characteristics Over Operating Conditions and Using Standard Test Load

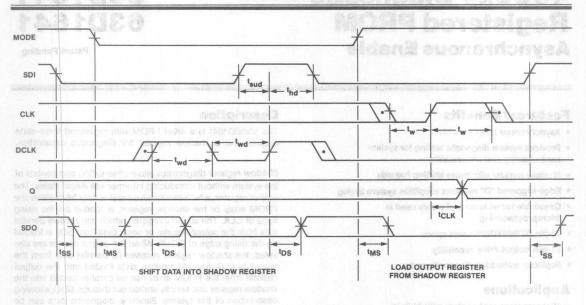
SYMBOL	PARAMETER	MILITAI MIN TYP†		COMM MIN T			דואט
tCLK	CLK to output	13	25	60	13	20	ns
t _{ER}	Enable time	16	30		16	25	ns
^t EA	Disable time	16	30		16	25	ns
^t IQ	Initialization to output delay	23	40	Calak Second	23	35	ns
f _{MAXD}	Maximum diagnostic clock frequency	7 18	AND STORY	10	18	Range of	MHz
t _{DS}	DCLK to SDO delay (MODE = LOW)	BMARA19	35		19	30	ns
tss a	SDI to SDO delay (MODE = HIGH)	16	30	- parameter	16	25	ns
^t MS	MODE to SDO delay	14	30		14	25	ns

[†] Typicals at 5.0 V VCC and 25°C TA.

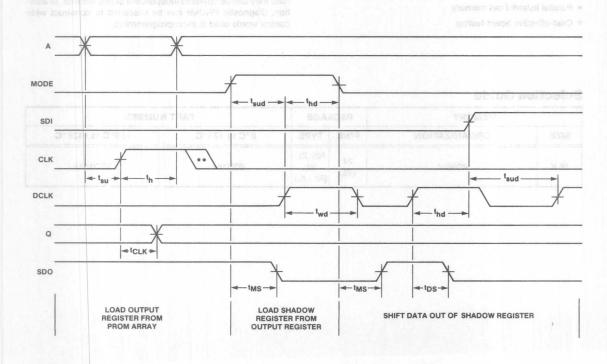
Definition of Waveforms



NORMAL PROM OPERATION (MODE = LOW)



SYSTEM CONTROL



SYSTEM OBSERVATION

Features/Benefits

- Asynchronous output enable
- Provides system diagnostic testing for system controllability and observability
- Shadow register eliminates shifting hazards
- Edge-triggered "D" registers simplifies system timing
- · Casadable for wide control words used in microprogramming
- 24-pin SKINNYDIP® saves space
- 24-mA output drive capability
- · Replaces embedded diagnostic code

Applications

- · Microprogram control store with built-in system diagnostic testing
- Serial character generator
- Serial code converter
- Parallel in/serial out memory
- Cost-effective board testing

Description

The 53/63D1641 is a 4Kx4 PROM with registered three-state outputs and a shadow register for diagnostic capabilities.

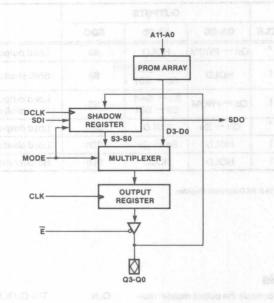
Shadow register diagnostics allow observation and control of the system without introducing intermediate illegal states. The output register, which can receive parallel data from either the PROM array or the shadow register, is loaded on the rising edge of CLK. The shadow register, which can receive parallel data from the output register or serial data from SDI, is loaded on the rising edge of DCLK. When the output drivers are disabled, the shadow register receives its parallel data from the output bus. During diagnostics, data loaded into the output register from the PROM array can be parallel-loaded into the shadow register and serially shifted out through SDO, allowing observation of the system. Similarly, diagnostic data can be serially shifted into the shadow register through SDI, and parallel-loaded into the output register, allowing control and test scanning to be imposed on the system. Since the output register and the shadow register are loaded by different input signals, they can be operated independent of one another. In addition, diagnostic PROMs can be cascaded to construct wide control words used in microprogramming.

Selection Guide

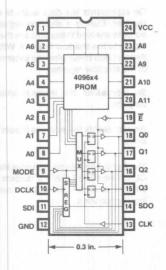
MEMORY		PACKAGE		PART NUMBER	
SIZE	ORGANIZATION	PINS	TYPE	0°C to +75°C	-55°C to +125°C
16 K	4096x4	24 (28)	NS,JS, W, (NL),(L)	63D1641	53D1641

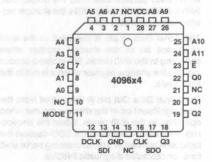
3

Block Diagram



Pin Configurations





Plastic Chip Carrier

Function Table

INPUTS				OUTPUTS			OPERATION
MODE	SDI	CLK	DCLK	Q3-Q0	S3-S0	SDO	OPERATION
L	X	1	*	Qn ← PROM	HOLD	S3	Load output register from PROM array
L	X	*	†	HOLD	Sn ← Sn-1 S0 ← SDI	S3	Shift shadow register data
L	X	†	1	Qn ←PROM	Sn ← Sn-1 S0 ← SDI	S3	Load output register from PROM array while shifting shadow register data
Н	Χ	1	*	Qn ← Sn	HOLD	SDI	Load output register from shadow register
Н	L	*	1	HOLD	Sn ← Qn	SDI	Load shadow register from output bus
Н	Н	*	1	HOLD	HOLD	SDI	No operation†

^{*} Clock must be steady or falling.

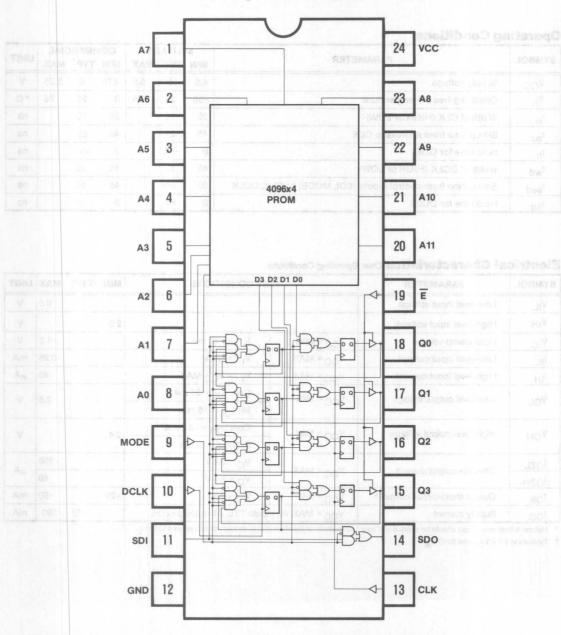
Definition of Signals

Dell	nition of Signals		
MODE	The MODE pin controls the output register mul- tiplexer and the shadow register. When MODE is LOW, the output register receives data from	CLK	The CLOCK pin loads the output register on the rising edge of CLK.
	the PROM array and the shadow register is con- figured as a shift register with SDI as its input. When MODE is HIGH, the output register receives	DCLK	The diagnostic clock pin loads or shifts the shadow register on the rising edge of DCLK.
	data from the shadow register. The shadow register is controlled by SDI as well as MODE. With MODE HIGH and SDI LOW, the shadow register receives parallel data from the output bus. With MODE and SDI both HIGH, the shadow register holds its present data.	Q3-Q0	On represents the data outputs of the output register. During a shadow register load with outputs enabled these pins are the internal data inputs to the shadow register. With the outputs three-stated these pins are external data inputs to the shadow register.
SDI	The Serial Data In pin is the input to the least significant bit of the shadow register when operating in the shift mode. SDI is also a control input to the shadow register when it is not in the shift mode.	S3-S0 A11-A0	Sn represents the internal shadow register outputs. An represents the address inputs to the PROM
SDO	The Serial Data Out pin is the output from the most significant bit of the shadow register when	ATT-AU	array.
	operating in the shift mode. When the shadow register is not in the shift mode, SDO displays the logic level present at SDI, decreasing serial shift time for cascaded diagnostic PROMs.	Ē	The Output Enable pin operates independent of CLK. When E is LOW the outputs are enabled. When E is HIGH, the outputs are in the high impedance state.

[†] Reserved operation for SN54/74S818 8-Bit Diagnostic Register.

Logic Diagram

4096x4 Diagnostic PROM
with Asynchronous Enable



	Operating	rrogramming
Supply voltage V _{CC}	0.5 V to 7 V	12 V
Input voltage		
Input Current	30 mA to +5 mA	
Off-state output voltage	0.5 V to 5.5 V	12 V
Storage temperature		

Operating Conditions

SYMBOL	PARAMETER		TYP [†]			MMER TYP [†]		UNIT
VCC	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
TA	Operating free air temperature	-55	25	125	0	25	75	°C
t _w	Width of CLK (HIGH or LOW)	25	10		20	10		ns
t _{su}	Set up time from address to CLK	45	25	1	40	25		ns
th	Hold time for CLK	0	-15	3 7.14	0	-15		ns
twd	Width of DCLK (HIGH or LOW)	45	15		40	15		ns
^t sud	Set up time from control inputs (SDI, MODE) to CLK, DCLK	50	20	1	45	20		ns
^t hd	Hold time for DCLK	0	-5	12A	0	-5		ns

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	on rot	EST CONDITIONS	MIN TYP†	MAX	UNIT
VIL	Low-level input voltage				0.8	V
VIH	High-level input voltage		J. J.	2.0		V
V _{IC}	Input clamp voltage	V _{CC} = MIN	I _I = -18 mA		-1.2	V
I _I L	Low-level input current	V _{CC} = MAX	V _I = 0.4 V		-0.25	mA
I _{IH}	High-level input current	V _{CC} = MAX	V _I = V _{CC} MAX		40	μΑ
VOL	Low-level output voltage	V _{CC} = MIN	Com I _{OL} = 24 mA		0.5	V
· OL	8452 3495 S24		Mil I _{OL} = 16 mA		0.5	V
V _{OH}	High-level output voltage	V _{CC} = MIN	Com I _{OH} = -3.2 mA	2.4		V
·OH	r ngir lover output voltage		Mil I _{OH} = -2 mA	2.4		V
lozL	Off state subsut surrent	V - MAY	V _O = 0.4 V		-100	
IOZH	Off-state output current	V _{CC} = MAX	V _O = 2.4 V		40	μΑ
los	Output short-circuit current*	V _{CC} = 5.V	V _O = 0 V	-20	-90	mA
Icc	Supply current	V _{CC} = MAX. All	inputs TTL. All outputs open.	140	190	mA

^{*} Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

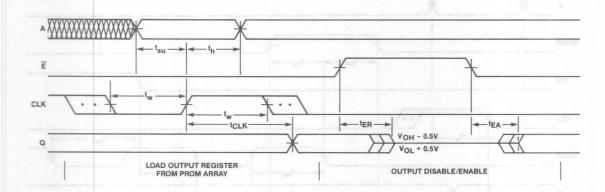
 $[\]dagger$ Typicals at 5.0 V $\rm V_{CC}$ and 25° C $\rm T_A$

Switching Characteristics Over Operating Conditions and Using Standard Test Load

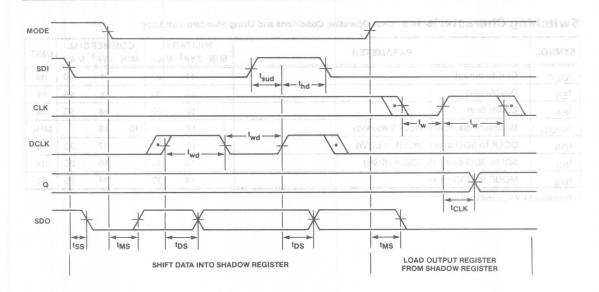
SYMBOL	PARAMETER	MILIT MIN TY	TARY P [†] MAX		MERCIAL TYP [†] MA)	UNIT
tCLK	CLK to output	1	1 25	de comment	11 20	ns
tER	Disable time	1	30		16 2	ns
t _{EA}	Enable time	10	30		16 2	5 ns
fMAXD	Maximum diagnostic clock frequency	7 18	3	10	18	MHz
t _{DS}	DCLK to SDO delay (MODE = LOW)	1	7 35		17 30	ns
tss	SDI to SDO delay (MODE = HIGH)	1	6 30		16 25	ns
^t MS	MODE to SDO delay	1	4 30		14 25	ns

[†] Typicals at 5.0 V VCC and 25°C TA.

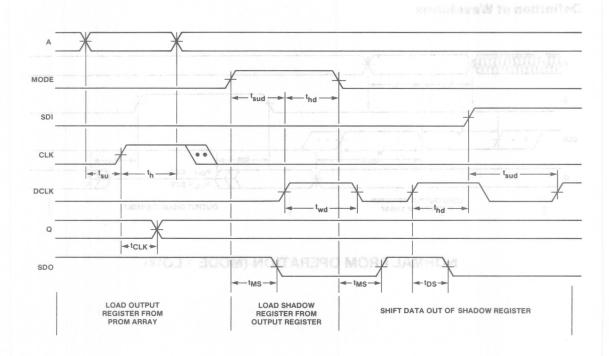
Definition of Waveforms



NORMAL PROM OPERATION (MODE = LOW)



SYSTEM CONTROL



SYSTEM OBSERVATION

4096x4 Diagnostic **Registered PROM**

53DA1643 63DA1643

Output Initialization

Features/Benefits

- Programmable asynchronous output initialization
- Provides system diagnostic testing with system controllability and observability
- . Shadow register eliminates shifting hazards
- Edge-triggered "D" registers simplifies system timing
- · Cascadable for wide control words used in microprogramming
- 24-pin SKINNYDIP® saves space
- 24-mA output drive capability
- · Replaces embedded diagnostic code

Applications

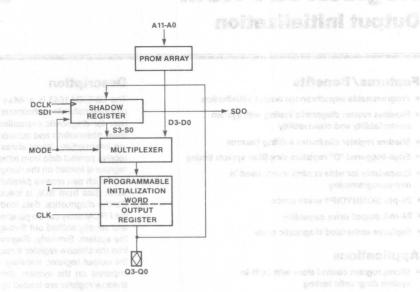
- . Microprogram control store with built-in system diagnostic testing
- Serial character generator
- · Serial code converter
- · Parallel in/serial out memory
- · Cost-effective board testing

Description

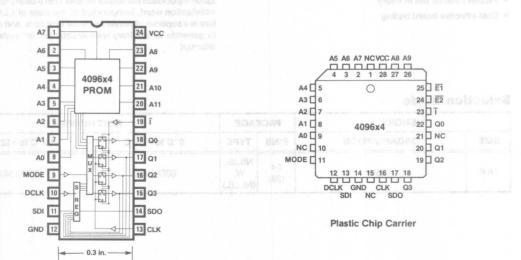
The 53/63DA1643 is a 4Kx4 PROM with registered outputs. programmable asynchronous initialization, and a shadow reqister for diagnostic capabilities. Shadow register diagnostics allow observation and control of the system without introducing intermediate illegal states. The output register, which can receive parallel data from either the PROM array or the shadow register is loaded on the rising edge of CLK. The shadow register, which can receive parallel data from the output register or serial data from SDI, is loaded on the rising edge of DCLK. During diagnostics, data loaded into the output register from the PROM array can be parallel-loaded into the shadow register and serially shifted out through SDO, allowing observation of the system. Similarly, diagnostic data can be serially shifted into the shadow register through SDI, and parallel-loaded into the output register, allowing control and test scanning to be imposed on the system. Since the output register and the shadow register are loaded by different input signals, they can be operated independently of one another. In addition, diagnostic PROMs can be cascaded to construct wide control words used in microprogramming. When exercised, the Initialization input loads the output register with a user-programmable initialization word, independent of the state of CLK. This feature is a superset of preset and clear functions, and can be used to generate an arbitrary microinstruction for system reset or interrupt

Selection Guide

MEMORY MEMORY			KAGE	PART NUMBER		
SIZE	ORGANIZATION	PINS	TYPE	0°C to +75°C	-55°C to +125°C	
16 K	4096x4	24 (28)	NS,JS, W, (NL),(L)	63DA1643	53DA1643	



Pin Configurations



Function Table

INPUTS			OUTPUTS			OPERATION	
MODE	SDI	CLK	DCLK	Q3-Q0	S3-S0	SDO	OPERATION
L	X	1	*	Qn ← PROM	HOLD	S3	Load output register from PROM array
L	X	*	1	HOLD	Sn ← Sn-1 S0 ← SDI	S3	Shift shadow register data
L	Х	1	dov	Qn ← PROM	Sn ← Sn-1 S0 ← SDI	S3	Load output register from PROM array while shifting shadow register data
Н	X	1	*	Qn ← Sn	HOLD	SDI	Load output register from shadow register
Н	L	*	1	HOLD	Sn ← Qn	SDI	Load shadow register from output bus
Н	Н	*	1SA	HOLD	HOLD	SDI	No operation†

^{*} Clock must be steady or falling.

Definition of Signals

The MODE pin controls the output register mul- tiplexer and the shadow register. When MODE is LOW, the output register receives data from	CLK	The clock pin loads the output register on the rising edge of CLK.
the PROM array and the shadow register is configured as a shift register with SDI as its input.	DCLK	The diagnostic clock pin loads or shifts the shadow register on the rising edge of DCLK.
data from the shadow register. The shadow reg- ister is controlled by SDI as well as MODE. With MODE HIGH and SDI LOW, the shadow regis- ter receives parallel data from the output register.	Q3-Q0	On represents the data outputs of the output register. During a shadow register load these pins are the internal data inputs to the shadow register.
register holds its present data.	S3-S0	Sn represents the internal shadow register outputs.
	444.40	
operating in the shift mode. SDI is also a control input to the shadow register when it is not in the	A11-A0	An represents the address inputs to the PROM array.
shift mode.	I JC	The asynchronous output register initialization
The Serial Data Out pin is the output from the most significant bit of the shadow register when operating in the shift mode. When the shadow register is not in the shift mode, SDO displays the logic level present at SDI, decreasing serial shift time for cascaded diagnostic PROMs.		input pin operates independent of CLK. When is LOW, the output register is loaded with a user programmable initialization word. Programmable initialization is a super set of preset and clear functions, and can be used to generate any microinstruction for system reset or interrupt.
	tiplexer and the shadow register. When MODE is LOW, the output register receives data from the PROM array and the shadow register is configured as a shift register with SDI as its input. When MODE is HIGH, the output register receives data from the shadow register. The shadow register is controlled by SDI as well as MODE. With MODE HIGH and SDI LOW, the shadow register receives parallel data from the output register. With MODE and SDI both HIGH, the shadow register holds its present data. The Serial Data In pin is the input to the least significant bit of the shadow register when operating in the shift mode. SDI is also a control input to the shadow register when it is not in the shift mode. The Serial Data Out pin is the output from the most significant bit of the shadow register when operating in the shift mode. When the shadow register is not in the shift mode, SDO displays the logic level present at SDI, decreasing serial shift	tiplexer and the shadow register. When MODE is LOW, the output register receives data from the PROM array and the shadow register is configured as a shift register with SDI as its input. When MODE is HIGH, the output register receives data from the shadow register. The shadow register is controlled by SDI as well as MODE. With MODE HIGH and SDI LOW, the shadow register receives parallel data from the output register. With MODE and SDI both HIGH, the shadow register holds its present data. The Serial Data In pin is the input to the least significant bit of the shadow register when operating in the shift mode. SDI is also a control input to the shadow register when operating in the shift mode when it is not in the shift mode. The Serial Data Out pin is the output from the most significant bit of the shadow register when operating in the shift mode. When the shadow register is not in the shift mode, SDO displays the logic level present at SDI, decreasing serial shift

[†] Reserved operation for SN54/74S818 8-Bit Diagnostic Register.

Logic Diagram 4096x4 Diagnostic PROM with Asynchronous Initialization VCC 24 s ab revision web A7 2 23 A8 A6 A9 A5 3 22 4096x4 PROM 5 20 D3 D2 D1 D0 19 -0-18 OA rel outs include to the stradow MODE 16 15 SDO isn't bou formed to iss inquiSDI 12 13 CLK GND

Absolute Maximum Ratings	Operating	s. O peristative
THE REAL PROPERTY OF THE PARTY	Operating	Programming
Supply voltage V _{CC}	0.5 V to 7 V	12 V
Input voltage	1.5 V to 7 V	7 V
Supply voltage V _{CC}	30 mA to +5 mA	
Off-state output voltage		
Storage temperature	65° to +150° C	

Operating Conditions

SYMBOL	PARAMETER	41 34 3	ILITARY TYP [†] MAX	10- CT 1550	MERCIA TYP† M		UNIT
Vcc	Supply voltage	4.5	5 5.5	4.75	5 5	.25	V
TA	Operating free-air temperature	-55	25 125	0	25	75	°C
t _w	Width of CLK (HIGH or LOW)	25	10	20	10		ns
t _{su}	Set up time from address to CLK	45	25	40	25		ns
th	Hold time for CLK	0	-15	0	-15		ns
twd	Width of DCLK (HIGH or LOW)	45	15	40	15		ns
tsud	Set up time from control inputs (SDI, MODE) to CLK, DCLK	50	20	45	20		ns
t _{hd}	Hold time for DCLK	0	-5	0	-5	. 0.40	ns
tiw	Initialization pulse width (LOW)	25	10	20	10	40.476.0	ns
tir	Initialization recovery time	45	25	40	25		ns

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	Т	EST CONDITIONS	MIN TYP	MAX	UNIT
V _{IL}	Low-level input voltage			<i>j</i>	0.8	V
VIH	High-level input voltage			2.0		V
VIC	Input clamp voltage	V _{CC} = MIN	I _I = -18 mA		-1.2	V
_I _I L	Low-level input current	V _{CC} = MAX	V _I = 0.4 V	www.	-0.25	mA
I _{IH}	High-level input current	V _{CC} = MAX	V _I = V _{CC} MAX	- 01'	40	μΑ
VOL	Low-level output voltage	V _{CC} = MIN	Com I _{OL} = 24 mA		0.5	V
·OL	(1)(0) 1 - 0.0	TO BELL LEGIST A	Mil I _{OL} = 16 mA	a .	0.5	V
Vон	High-level output voltage	V _{CC} = MIN	Com I _{OH} = -3.2 mA	2.4		V
ЮН	ng. ioro, output rollago		Mil I _{OH} = -2 mA	2.4		V
los	Output short-circuit current*	V _{CC} = MAX	V _O = 0 V	-20	-90	mA
lcc	Supply current	V _{CC} = MAX. All	inputs TTL. All outputs open.	140	190	mA

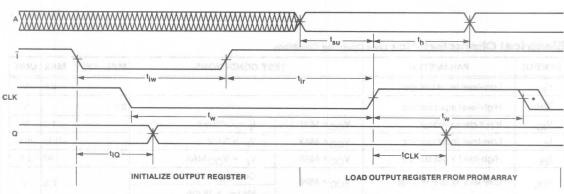
^{*} Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

[†] Typicals at 5.0 V V_{CC} and 25°C T_A.

SYMBOL	PARAMETER	MILITA MIN TYP [†]		COMMER MIN TYP		UNIT
tCLK	CLK to output	11	25	- 9191	20	ns
t IQ	Initialization to output delay	23	40	23	35	ns
fMAXD	Maximum diagnostic clock frequency	7 18		10 18		MHz
t _{DS}	DCLK to SDO delay (MODE = LOW)	17	35	17	30	ns
tss	SDI to SDO delay (MODE = HIGH)	16	30	16	25	ns
t _{MS}	MODE to SDO delay	14	30	14	25	ns

[†] Typicals at 5.0 V VCC and 25°C TA.

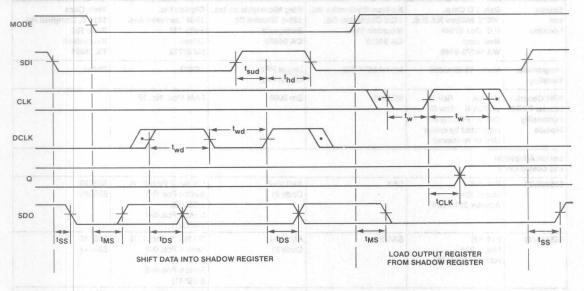
Definition of Waveforms



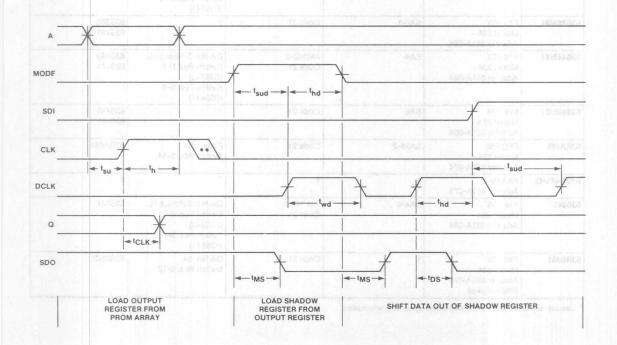
NORMAL PROM OPERATION (MODE = LOW)







SYSTEM CONTROL



SYSTEM OBSERVATION

Monolithic Memories PROM Programmer Reference Chart

Monolithic Memories PROM Programmer Reference Chart

Source	Data I/O Corp.	Kontron Electronics Inc.	Stag Microsystems Inc.	Digelec Inc.	Varix Corp.
and Location	10525 Willows Rd. N.E. P.O. Box 97046 Redmond WA 98073-9746	1230 Charleston Rd. Mountain View CA 94039	528-5 Weddell Dr. Sunnyvale CA 94089	1602 Lawrence Ave. Suite 113 Ocean NJ 07712	1210 E. Campbell Rd. Suite 100 Richardson TX 75081
Programmer Model(s)	Model 19/29A/29B	Model MPP-80S	Model PPX Model PPZ	UP803	OMNI
MMI Generic Bipolar PROM Personality Module	UniPak Rev 10 UniPak II Rev 07 (Not all PROMs are supported by earlier UniPak revisions)	MOD16	Zm 2000	FAM Mod. No. 12	A.
Socket Adapter and Device Cod					
63\$080/81	F18 P02 Model 22A - Adapter 351A-064	SA3	AM110-2 Code 21	DA No. 2 Pinout 1A Switch Pos. 0-7 (63S080) Switch Pos. 0-6 (63S081)	63S080 63S081
63\$140/41	F18 P01 Model 22A - Adapter 351A-064	SA4-2 and	AM130-2 Code 21	DA No. 1 Pinout 1B Switch Pos. 0-7 (63S140) Switch Pos. 0-6 (63S141)	63S140 63S141
63S240/41	F18 P03 Model 22A - Adapter 351A-064	SA4-1	AM130-3 Code 21	DA No. 1 Pinout 1D Switch Pos. 2-15 (63S240) Switch Pos. 2-14 (63S241)	63S240 63S241
63S280/81	F18 P08 Model 22A - Adapter 351A-064	SA6-1	Code 21	†	63S280 63S281
63S440/41	F18 P05 Model 22A - Adapter 351A-064	SA4	AM140-2 Code 21	DA No. 3 Pinout 1E Switch Pos. 0-7 (63S440) Switch Pos. 0-6 (63S441)	63S440 63S441
63\$480/81	F18 P09 Model 22A - Adapter 351A-064	SA6	Code 21	†	63S480 63S481
63RA481	FEC P65 Model 22A - Adapter 351A-074	SA31-2	Code 21	Pinout 1H Switch Pos. 5-14	63RA481
63DA441/42	FAA PAC Adapter 351A-073	†	*	†	† 830
63S841	F18 P06 Model 22A - Adapter 351A-064	SA4-4	AM 140-3 Code 21	DA No. 3 Pinout 1L Switch Pos. 5-15 (63S840) Switch Pos. 5-14 (63S841)	63S841
63RS881	F18 P86 Model 22A - Adapter 351A-074 (300 mil pkg)	1 - 201-2	Code 21	DA No. 64 Switch Pos. 0-12	63RS881

[†] Contact manufacturer for availability and programming information.

SYSTEM OBSERVATION

3

Monolithic Memories PROM Programmer Reference Chart

Source and Location	Data I/O Corp. 10525 Willows Rd. N.E. P.O. Box 97046 Redmond WA 98073-9746	Kontron Electronics Inc. 1230 Charleston Rd. Mountain View CA 94039	Stag Microsystems Inc. 528-5 Weddell Dr. Sunnyvale CA 94089	Digelec Inc. 1602 Lawrence Ave. Suite 113 Ocean NJ 07712	Varix Corp. 1210 E. Campbell Rd. Suite 100 Richardson TX 75081
Programmer Model(s)	Model 19/29A/29B	Model MPP-80S	Model PPX Model PPZ	UP803	OMNI
MMI Generic Bipolar PROM Personality Module	UniPak Rev 10 UniPak II Rev 07 (Not all PROMs are supported by earlier UniPak revisions)	MOD16	Zm 2000	FAM Mod. No. 12	
Socket Adapter and Device Co					
63DA841	FAA PAD Adapter 351A-073	†	†	†	†
63S1641	F18 P53 Model 22A - Adapter 351A-064	SA20	AM 120-6 Code 21	DA No. 70 Switch Pos. 4-12	63S1641
63S1681	F18 P21	SA5-4	AM 100-5 Code 21	DA No. 7	63S1681
63RA1681 63RS1681	F18 PA3	†	Code 21	DA No. 64	63RA1681 63RS1681
63D1641	FB2 P80 Adapter 351A-073	†	Code 21	†	63D1641
63DA1643	FAA P87 Adapter 351A-073	†	†	†	†
63S3281	F18 P63	†	Code 21	DA No. 64 Pinout 47 Switch Pos. 0-4	63S3281

[†] Contact manufacturer for availability and programming information.



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PLE to PROM Cross Reference

TEMP. RANGE	PLE NUMBER	INPUTS	OUTPUTS	OUTPUT TYPE	MEMORY SIZE	PROM NUMBER	PACKAGE
	PLE5P8C	5	8	Three-State	32 x 8	63S081	16N,J,(20),(NL)
	PLE5P8AC	5	8	Three-State	32 x 8	63S081A	16N,J,(20),(NL)
	PLE8P4C	8	4	Three-State	256 x 4	63S141A	16N,J,(20),(NL)
	PLE8P8C	8	8	Three-State	256 x 8	63S281A	20N,J,NL
	PLE9P4C	9	4	Three-State	512 x 4	63S241A	16N,J,(20),(NL)
	PLE9P8C	9	8	Three-State	512 x 8	63S481A	20N,J,NL
	PLE10P4C	10	4	Three-State	1024 x 4	63S441A	18N,J,(20),(NL)
	PLE10P8C	10	8	Three-State	1024 x 8	63S881A	24N,J,NS,JS,(28),(NL)
Com.	PLE11P4C	11	4	Three-State	2048 x 4	63S841A	18N,J,(20),(NL)
	PLE11P8C	11	8	Three-State	2048 x 8	63S1681A	24N,J,NS,JS,(28),(NL)
	PLE12P4C	12	4	Three-State	4096 x 4	63S1641A	20N,J,NL
	PLE12P8C	12	8	Three-State	4096 x 8	63S3281A	24N,J,(28),(NL)
	PLE9R8C	9	8	Register	512 x 8	63RA481A	24NS,JS,(28),(NL)
	PLE10R8C	10	8	Register	1024 x 8	63RS881A	24NS,JS,(28),(NL)
	PLE11RA8C	11	8	Register	2048 x 8	63RA1681A	24NS,JS,(28),(NL)
	PLE11RS8C	- 11	8	Register	2048 x 8	63RS1681A	24NS,JS,(28),(NL)
TOTAL	PLE5P8M	5	8	Three-State	32 x 8	53S081	16J,W,(20),(L)
	PLE8P4M	8	4	Three-State	256 x 4	53S141A	16J,W,(20),(L)
	PLE8P8M	8	8	Three-State	256 x 8	53S281A	20J,W,L
	PLE9P4M	9	4	Three-State	512 x 4	53S241A	16J,W,(20),(L)
	PLE9P8M	9	8	Three-State	512 x 8	53S481A	20J,F,L
	PLE10P4M	10	4	Three-State	1024 x 4	53S441A	18J,W,(20),(L)
	PLE10P8M	10	8	Three-State	1024x8	53S881A	24JS,J,W,(28),(L)
Mil.	PLE11P4M	- 11	4	Three-State	2048 x 4	53S841A	18J,W,(28),(L),(20),(L)
	PLE11P8M	11	8	Three-State	2048 x 8	53S1681A	24JS,J,W,(28),(L)
	PLE12P4M	12	4	Three-State	4096 x 4	53S1641A	20J
	PLE12P8M	12	8	Three-State	4096 x 8	53S3281A	24J,W,(28),(L)
	PLE9R8M	9	8	Register	512 x 8	53RA481A	24JS,W,(28),(L)
	PLE10R8M	10	8	Register	1024 x 8	53RS881A	24JS,J,W,(28),(L)
	PLE11RA8M	11	8	Register	2048 x 8	53RA1681A	24JS,W,(28),(L)
	PLE11RS8M	11	8	Register	2048 x 8	53RS1681A	24JS,W,(28),(L)

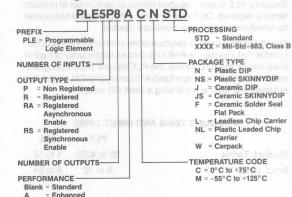
^{*} The PLE11P4M is available in a 20- or 28-pin Leadless Chip Carrier

Programmable Logic Element PLE™ Circuit Family

Features/Benefits

- Programmable replacement for conventional TTL logic
- Reduces IC inventories and simplifies their control
- · Expedites and simplifies prototyping and board layout
- Saves space with 0.3-inch SKINNYDIP® packages (except
- Programmed on standard PROM programmers
- Test and simulation made simple with PLEASM™ software
- Low-current PNP inputs
- Three-state outputs
- Reliable TiW fuses guarantee >98% programming yield

Ordering Information



PLE Circuit Selection Guide

PART NUMBER	INPUTS	OUTPUTS	PRODUCT TERMS	OUTPUT	tpD (ns) MAX*
PLE5P8	w s 5 m of ent	in the set of the total	32	A CONTROL OF SHIP IN THE	25
PLE5P8A	brandsman and	Low th 80 month result	32		15
PLE8P4	8	4	256		30
PLE8P8	8	8	256		28
PLE9P4	9	4	512		35
PLE9P8	9	8	512		30
PLE10P4	10	4	1024		35
PLE10P8	10	8	1024		30
PLE11P4	11	4	2048		35
PLE11P8	11 : 3800	TS, Rengrered Curr	2048	319	35
PLE12P4	12	4	4096		35
PLE12P8	12	8	4096	AINT	35
PLE9R8	9	8	512	8	15
PLE10R8	10	8	1024	8	15
PLE11RA8	11	8	2048	4A3 8	15
PLE11RS8	11	8	2048	8	15

^{*} Clock to output time for registered outputs.

Note: Commercial limits specified.



Logic Element

Joining the world of IdeaLogic™ is a new generation of Highspeed PROMs which the designer can use as *Programmable Logic Elements*. The combination of PLE circuits as logic elements with PAL devices can greatly enhance system speed while providing almost unlimited design freedom.

Basically, PLE circuits are ideal when a large number of product terms is required. On the other hand, a PAL device is best suited for situations when many inputs are needed.

The PLE circuit transfer function is the familiar OR of products, Like the PAL device, the PAE circuit has a single array of fusible links. Unlike the PAL device, the PLE circuits have a programmable OR array driven by a fixed AND array (the PAL device is a programmed AND array driving a fixed OR array).

PRODUCT TERM AND INPUT LINES

	PLE	PAL	
Product Terms	32 to 4096	1 to 16	
Input Lines	5 to 12	6 to 64	

The PLE family features common electrical parameters and programming algorithm, low-current PNP inputs, full Schottky clamping and three-state outputs.

The entire PLE family is programmed on conventional PROM programmers with the appropriate personality cards and socket adapters.

The registered PLE circuits have on-chip "D" type registers, versatile output enable control through synchronous and asynchronous enable inputs, and flexible start-up sequencing through programmable initialization.

Data is transferred into the output registers on the rising edge of the clock. Provided that the asynchronous (E) and synchronous (E) enables are Low, the data will appear at the outputs. Prior to the positive clock edge, register data are not affected by changes in addressing or synchronous enable inputs.

Data control is made flexible with synchronous and asynchronous enable inputs. Outputs may be set to the high-impedance state at any time by setting \overline{E} to a High or if \overline{ES} is High when the rising clock edge occurs. When V_{CC} power is first applied the synchronous enable flip-flop will be in the set condition causing the outputs to be in the high-impedance state.

A flexible initialization feature allows start-up and time-out sequencing with 1:16 programmable words to be loaded into the output registers. With the synchronous INITIALIZE ($\overline{\rm IS}$) pin Low, one of the 16 initialize words, addressed through pins 5,6,7 and 8 will be set in the output registers independent of all other input pins. The unprogrammed state of $\overline{\rm IS}$ words are Low, presenting a CLEAR with $\overline{\rm IS}$ pin Low. With all $\overline{\rm IS}$ column words (A3-AO) programmed to the same pattern, the $\overline{\rm IS}$ function will be used as a single pin control. With all $\overline{\rm IS}$ words programmed High a PRESET function is performed.

The PLE9R8 has asynchronous PRESET and CLEAR functions. With the chip enabled, a Low on the \overline{PR} input will cause all outputs to be set to the High state. When the \overline{CLR} input is set Low the output registers are reset and all outputs will be set to the Low state. The \overline{PR} and \overline{CLR} functions are common to all output registers and independent of all other data input states.

	AND	OR	OUTPUT OPTIONS
PLE	Fixed	Prog	TS, Registered Outputs, Fusible Polarity
FPLA	Prog	Prog	TS, OC, Fusible Polarity
FPGA	Prog	Prog	TS, OC, Fusible Polarity
FPLS	Prog	Prog	TS, Registered Feedback I/O
PAL	Prog	Fixed	TS, Registered Feedback I/O Fusible Polarity

4

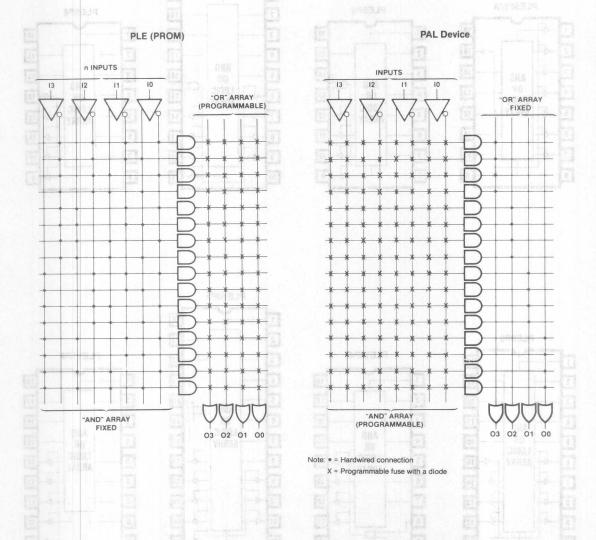
PLEASM™ Software

Software that makes programmable logic easy.

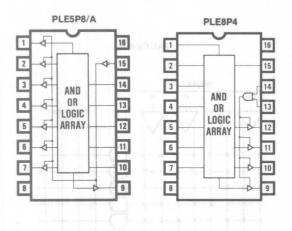
Monolithic Memories has developed a software tool to assist in designing and programming PROMs as PLE circuits. This package called "PLEASM" (PLE Assembler) is available for several computers including the VAX/VMS and IBM PC/DOS. PLEASM

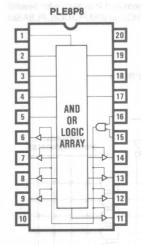
software converts design equation (Boolean and arithmetic) into truth tables and formats compatible with PROM programmers. A simulator is also provided to test a design using a Function Table before actually programming the PLE circuit.

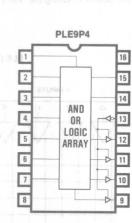
PLEASM software may be requested through the Monolithic Memories IdeaLogic Exchange.

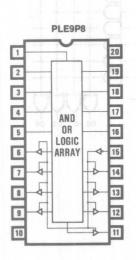


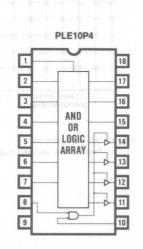
Logic Symbols

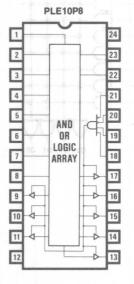


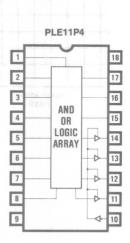






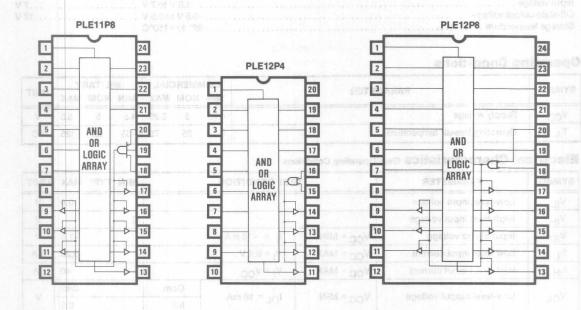


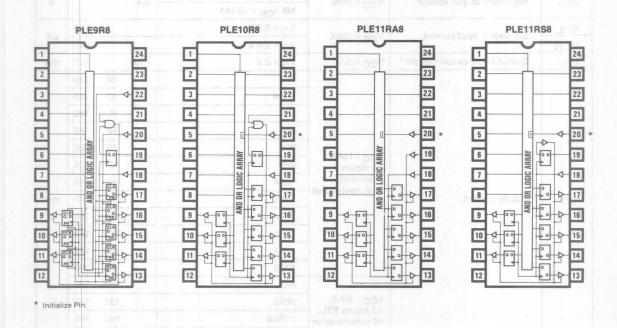




4

Logic Symbols





Absolute Maximum Ratings

	Operating	Programming
Supply voltage V _{CC}	-0.5~V~to~7~V	12 V
Input voltage	-1.5~V~to~7~V	7 V
Off-state output voltage	0.5 V to 5.5 V	12 V
Storage temperature	50 to +1500C	

Operating Conditions

SYMBOL		PARAMETER	115		MMER NOM	CIAL	1.6	NOM		UNIT
VCC	Supply voltage	See S	Region 1	4.75	5	5.25	4.5	5	5.5	V
TA	Operating free-air te	mperature	List	0	25	75	-55	25	125	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TE	ST CONDITION		MIN	TYP†	MAX	UNIT
VIL	Low-level input voltage		TANGE TO		Zavieri general		0.8	V
VIH	High-level input voltage				2		1	V
V _{IC}	Input clamp voltage	V _{CC} = MIN	I _I = -18 mA		447		-1.5	V
IL IS	Low-level input current	V _{CC} = MAX	V _I = 0.4 V				-0.25	mA
I _{IH}	High-level input current	V _{CC} = MAX	V ₁ = V _{CC}				40	μΑ
Вот до технология выполнения положения от положения выполнения выста выполнения выста выполнения выста выполнения выста выполнения выста выполнения выполнения выполнения выста выполнения выполнения		V - MINI	10-10-1	Com	- Barrelland	Charles I and Com-	0.45	V
VOL	Low-level output voltage	V _{CC} = MIN	$I_{OL} = 16 \text{ mA}$	Mil			0.5	V
V	High-level output voltage	V NAINI	Com I _{OH} = -3.2	mA	2.4			V
VOH	High-level output voltage	V _{CC} = MIN	Mil I _{OH} = -2 mA		2.4			V
IOZL	Off-state output current	WAS MAN	V _O = 0.4 V V _O = 2.4 V		-40		-40	μΑ
lozh	On-state output current	V _{CC} = MAX			40			μΑ
los	Output short-circuit current*	V _{CC} = 5 V	V _O = 0 V	aron.	-20		-90	mA
			5P8	print	1833	90	125	
25			5P8A		133	90	125	- 1
111			8P4		- (1)	80	130	1
The second			8P8	g- s.	Fish	90	140	
Miles Marie			9P4		1111	80	130	
Santa .		VCC = MAX	9P8	north and or	2000	104	155	
State of the latest		grounded;	10P4	Torres.	The state of	95	140	
ICC	Supply current	all outputs open	10P8	127	Line	92	160	mA
10			11P4	10 (1)	[6:]	110	150	F 91.
M-04			11P8			135	185	
			12P4	All the same	150	130	175	F .F
		and the second	12P8	- I want	170	150	190	
	description of the second	The second second second	9R8	Marine Trans	1-14	130	180	1
		VCC = MAX	10R8		130 18		180	T Heden
4.1		All inputs TTL; all outputs open	11RA8			140	185	1
			11RS8			140	185	1

[†] Typicals at 5.0 V V_{CC} and 25°C T_A.

Switching Characteristics Over Commercial Operating Conditions

	ZAS	DEVICE T		ANDREMAN ANDREMAN OF		t _{PD} (ns) PROPAGATION DELAY MAX	t _{PZX} AND t _{PXZ} (ns) INPUT TO OUTPUT ENABLE/DISABLE TIME MAX
20	5P8AC	- 0r - r		67	125	15	WOLLSO COLIN HIGHE 20 WC 1
	5P8C					25	20
8113	8P4C		5		OS	30	20, 96.1)
En	8P8C	55 3	35	65	100	28	Rooks of Regal work at 25 to 10
an	9P4C	1 5 8			J.	35	Apelo et 23 mont et 20 miles (45) et
60	9P8C	3-	Ĉ.	3-	0	30	aksots ursugsi mud ur25 state
BII	10P4C	E -	7		8	35	Apols of 83 mov 25 (83) A
	10P8C					30	25
	11P4C		- 84	Apid Greff Trial	g Siteria	stice and an 35 stall greaterings	and and all recover 25 G g responses
-	11P8C	EATLE	100 1000	BUDI BYEK	DO	35	25
	12P4C	ALCOHOLOGICA COMPANY OF THE	4 -7	July P4117 and the man	(L) Talk Car operation	35	25
Bri	12P8C	12				35	30

Switching Characteristics Over Military Operating Conditions

26	DEVICE TYPE	t _{PD} (ns) PROPAGATION DELAY MAX	t _{PZX} AND t _{PXZ} (ns) INPUT TO OUTPUT ENABLE/DISABLE TIME MAX
5P8M		35	30
8P4M		40	30
8P8M		40	30
9P4M		45	30
9P8M		40	30
10P4M		50	30
10P8M		45	30
11P4M		50	30
11P8M		50	30
12P4M		50	30
12P8M		40	35

Operating Conditions

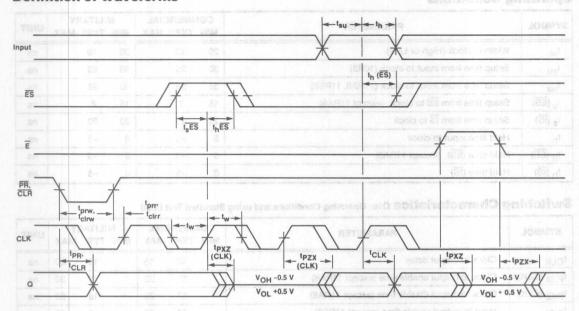
SYMBOL	PARAMETER	(80) (89) 1700 MANUTA DI ANCO	- 7	MMERCIAL TYP* MAX	1	IILITAF TYP*		UNIT
tw	Width of clock (High or Low)	XAN	20	10	20	10		ns
^t prw	Width of preset or clear	Automorphism	20	10	20	10		ns
tclrw	(Low) to Output (High or Low)	对	20	10	20	10		113
tprr	Recovery from preset or clear	CVE	20	11	25	11		ns
tclrr	(Low) to clock High		20	11	25	11	011	113
t _{su}	Setup time from input to clock	- 28	30	22	35	22	28	ns
t _S (ES)	Setup time from ES to clock	35	10	7	15	7	Date	ns
^t h	Hold time from input to clock	00	0	-5	0	-5	Jac	ns
th (ES)	Hold time from ES to clock	48	5	-3	5	-3	DIE	ns

Switching Characteristics Over Operating Conditions and using Standard Test Load

SYMBOL	PARAMETER	COM MIN 1		MAX	MILITAR MIN TYP*		UNIT
^t CLK	Clock to output delay		11	15	11	20	ns
t _{PR}	Preset to output delay		15	25	15	25	ns
t _{CLR}	Clear to output delay		18	25	18	35	ns
t _{PZX} (CLK)	Clock to output enable time anothern pattered visibility	RasaC s	14	25	14	30	ns
t _{PXZ} (CLK)	Clock to output disable time	-	14	25	14	30	ns
t _{PZX}	Input to output enable time (50) graft		10	20	10	25	ns
t _{PXZ}	Input to output disable time		10	20	10	25	ns

[†] Typicals at 5.0 V VCC and 25°C TA.

Definition of Waveforms



- NOTES: 1. Input pulse amplitude 0 V to 3.0 V.
 - 2. Input rise and fall times 2-5 ns from 0.8 V to 2.0 V.
 - 3. Input access measured at the 1.5 V level.
 - 4. Switch S₁ is closed. C_L = 30 pF and outputs measured at 1.5 V level for all tests except tpxz and tpzx.
 - 5. tpZX and tpZX(CLK) are measured at the 1.5 V output level with C_L = 30 pF. S₁ is open for high impedance to "1" test and closed for high impedance to "0" test.

 t_{PXZ} and $t_{PXZ(CLK)}$ are tested with C_L = 5 pF. S_1 is open for "1" to high impedance test, measured at V_{OH} -0.5 V output level; S_1 is closed for "0" to high impedance test measured at V_{OL} +0.5 V output level.

Operating Conditions

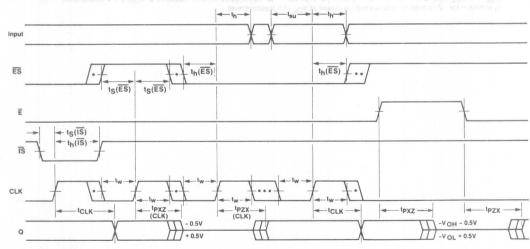
SYMBOL	PARAMETER	COMMERCIAL MIN TYP* MAX	MILITARY MIN TYP* MAX	UNIT
t _w	Width of clock (High or Low)	20 10	20 10	ns
t _{su}	Setup time from input to clock (10R8)	30 25	40 25	ns
t _{su}	Setup time from input to clock (11RA8, 11RS8)	35 28	40 28	ns
t _s (ES)	Setup time from ES to clock (except 11RA8)	15 7	15 8	ns
t _s (IS)	Setup time from IS to clock	25 20	30 20	ns
th	Hold time input to clock	0 -5	0 -5	ns
th (ES)	Hold time (ES) (except 11RA8)	5 -3	5 -3	ns
th (IS)	Hold time (IS)	0 -5	0 -5	ns

Switching Characteristics Over Operating Conditions and using Standard Test Load

SYMBOL	PARAMETER	COMME MIN TYP		MILITAR MIN TYP*	MAX	UNIT
t _{CLK}	Clock to output delay	10	15	10	20	ns
t _{PZX} (CLK)	Clock to output enable time (except 11RA8)	17	25	18	30	ns
t _{PXZ} (CLK)	Clock to output disable time (except 11RA8)	17	25	18	30	ns
^t PZX	Input to output enable time (except 11RS8)	17	25	17	30	ns
t _{PXZ}	Input to output disable time (except 11RS8)	/ 0 s or 7 8 17	25	17	30	ns

^{*} Typicals at 5.0 V VCC and 25°C TA.

Definition of Waveforms



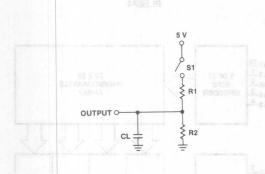
NOTES: 1. Input pulse amplitude 0 V to 3.0 V.

- 2. Input rise and fall times 2-5 ns from 0.8 V to 2.0 V.
- 3. Input access measured at the 1.5 V level.
- 4. Switch S₁ is closed. C_L = 30 pF and outputs measured at 1.5 V level for all tests except tpZx and tpXZ.
- 5. tpzx and tpzx(CLK) are measured at the 1.5 V output level with C_L = 30 pF. S₁ is open for high impedance to "1" test and closed for high impedance to "0" test.

 t_{PXZ} and $t_{PXZ(CLK)}$ are tested with C_L = 5 pF. S_1 is open for "1" to high impedance test, measured at V_{OH} =0.5 V output level: S_1 is closed for "0" to high impedance test measured at V_{OL} *0.5 V output level.

Switching Test Load

Definition of Timing Diagram



WAVEFORM INPUTS OUTPUTS

DON'T CARE; CHANGING; STATE UNKNOWN

NOT APPLICABLE

MUST BE STEADY

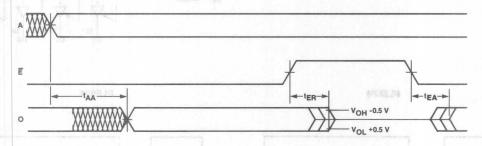
OUTPUTS

CHANGING; STATE UNKNOWN

CENTER LINE IS HIGH IMPEDANCE STATE

4

Definition of Waveforms



NOTES: Apply to electrical and switching characteristics.

Typical at 5.0 V V_{CC} and 25°C T_A.

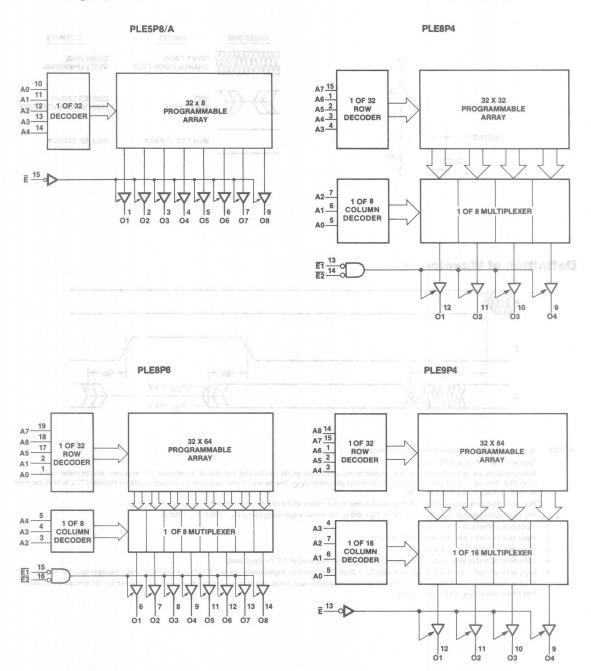
Measurements are absolute voltages with respect to the ground pin on the device and includes all overshoots due to system and/or tester noise. In all PLE devices unused inputs must be tied to either ground or V_{CC}. The series resistor required for unused inputs on standard TTL is NOT required for PLE devices, thus using less parts.

*Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

For commercial operating range R₁ = 200 Ω , R₂ = 390 Ω . For military operating range R₁ = 300 Ω , R₂ = 600 Ω .

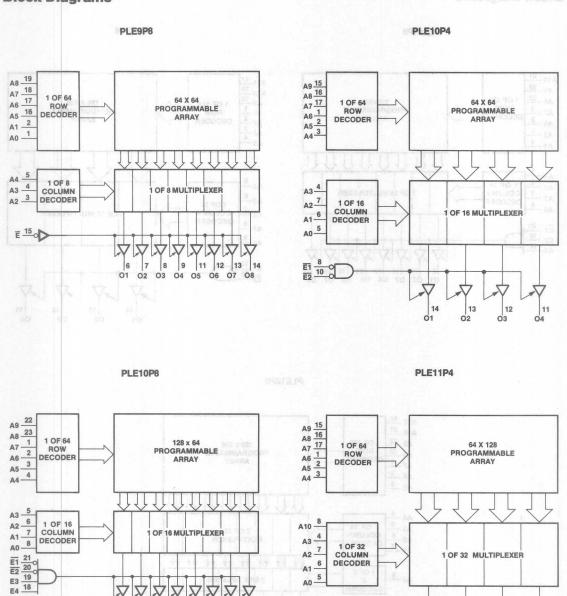
- 1. Input pulse amplitude 0 V to 3.0 V.
- 2. Input rise and fall times 2-5 ns from 0.8 to 2.0 V.
- 3. Input access measured at the 1.5 V level.
- 4. Data delay is tested with switch S_1 closed. C_L = 30 pF and measured at 1.5 V output level.
- 5. tp_{ZX} is measured at the 1.5 V ouput level with C_L = 30 pF. S₁ is open for high-impedance to "1" test and closed for high-impedance to "0" test. [†]PXZ is measured C_L = 5 pF. S₁ is open for "1" to high-impedance test, measured at V_{OH} -0.5 V output level; S₁ is closed for "0" to high-impedance test measured at V_{OH} +0.5 V output level.

Block Diagrams I gains I to not thit &



4

Block Diagrams



E1 10

14

13

02

12

03

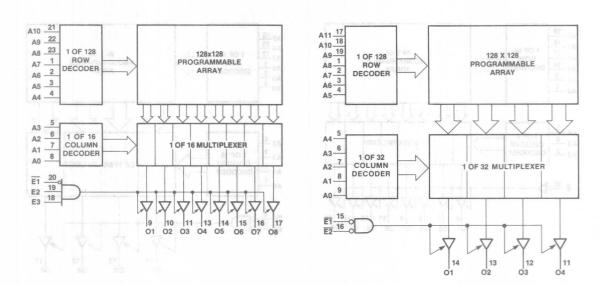
9 10 11 13 14 15 16 17

01 02 03 04 05 06 07 08

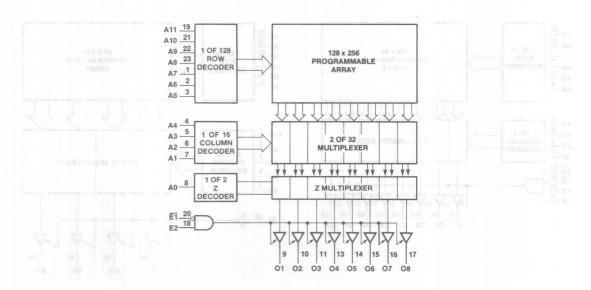
Block Diagrams

PLE11P8

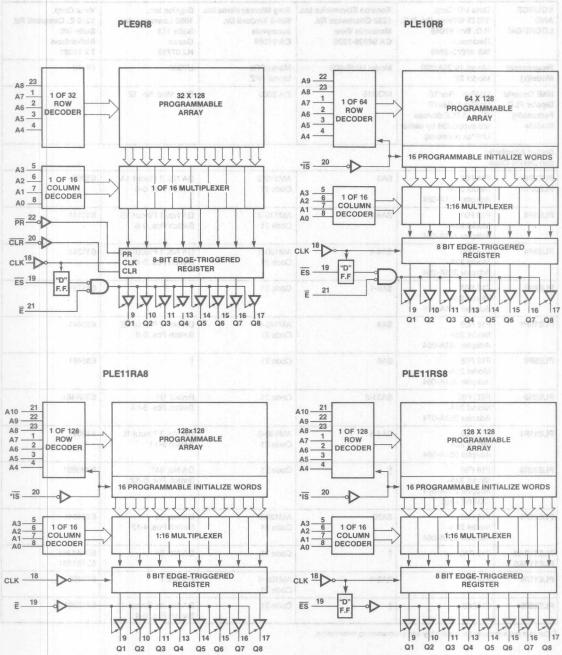
PLE12P4



PLE12P8



Block Diagrams



^{*}IS selects 1:16 programmable initialization words.

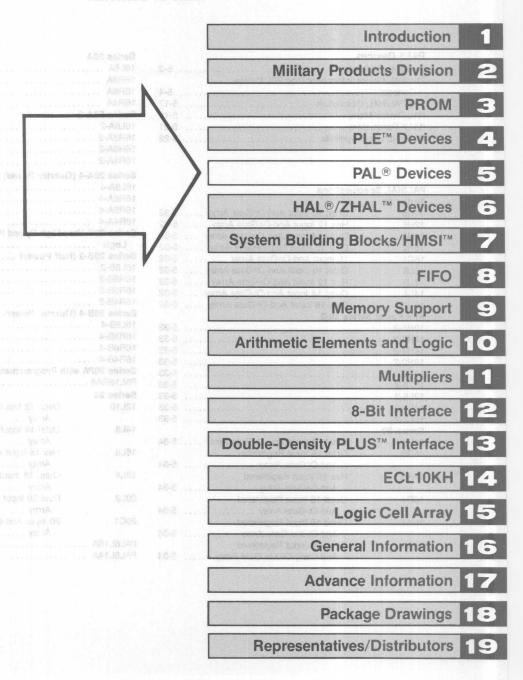
Monolithic Memories PLE Programmer Reference Chart

Monolithic Memories PLE Programmer Reference Chart

SOURCE AND LOCATION	Data I/O Corp. 10525 Willows Rd. N.E. P.O. Box 97046 Redmond WA 98073-9746	Kontron Electronics Inc. 1230 Charleston Rd. Mountain View CA 94039-7230	Stag Microsystems Inc. 528-5 Weddell Dr. Sunnyvale CA 94089	Digelec Inc. 1602 Lawrence Ave. Suite 113 Ocean NJ 07712	Varix Corp. 1210 E. Campbell Rd. Suite 100 Richardson TX 75081
Programmer Model(s)	Model 19/29A/29B Model 22	Model MMP-80S	Model PPX Model PPZ	UP803	OMNI
MMI Generic Bipolar PLE Personality Module	UniPak Rev 10 UniPak II Rev 07 (Not all PLE devices are supported by earlier UniPak revisions)	MOD16 2 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	Zm 2000	FAM Mod. No. 12	AS 2 DECODER AS 4 AS
Socket Adapte and Device Co		-1 -2 0% xu	THE STATE OF THE S		International Control
PLE5P8/ PLE5P8A	F18 P02 Model 22A- Adapter 351A-064	SA3	AM110-2 Code 21	DA No. 2 Pinout 1A Switch Pos. 0-6	63\$081 10 1 5A
PLE8P4	F18 P01 Model 22A- Adapter 351A-064	SA4-2	AM130-2 Code 21	DA No. 1 Pinout 1B Switch Pos. 0-6	63S141
PLE9P4	F18 P03 Model 22A- Adapter 351A-064	SA4-1	AM130-3 Code 21	DA No. 1 Pinout 1D Switch Pos. 2-14	63S241
PLE8P8	F18 P08 Model 22A- Adapter 351A-064	SA6-1	Code 21	NAMA!	63S281
PLE10P4	F18 P05 Model 22A- Adapter 351A-064	SA4	AM140-2 Code 21	DA No. 3 Pinout 1E Switch Pos. 0-6	63S441
PLE9P8	F18 P08 Model 22A- Adapter 351A-064	SA6	Code 21	* 848113.19	63S481
PLE9R8	FEC P65 Model 22A- Adapter 351A-074	SA31-2	Code 21	Pinout 1H Switch Pos. 5-14	63RA481
PLE11P4	F18 P06 Model 22A- Adapter 351A-064	SA4-4 WOA TA	AM140-3 Code 21	DA No. 3 Pinout 1L Switch 5-14	63S841
PLE10R8	F18 P86 Model 22A- Adapter 351A-074 (300 mil pkg)	†-5- 30 EP	Code 21	DA No. 64† Switch Pos. 0-12	63RS881
PLE12P4	F18 P53 Model 22A- Adapter 351A-064	SA20 81 90.1 8 8A 8	AM120-6 Code 21	DA No. 70 Switch Pos. 4-12	63S1641 EACH S CA
PLE11RA8 PLE11RS8	F18 PA3	†	Code 21	DA No. 64	63RA1681 63RS1681
PLE11P8	F18P21	SA5-4	AM100-5 Code 21	DA No. 7	63S1681
PLE12P8	F18P63	+4-8-4a	Code 21	DA No. 64 Pinout 47 Switch Pos. 0-4	63S3281

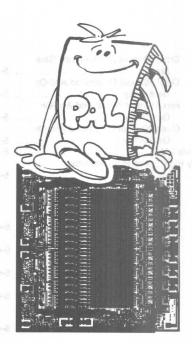
[†] Contact manufacturer for availability and programming information.

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20030	Octal 20 Input Register And-Or-Gate	F F0	20X10 20X8		
20RS4	Array w/product term sharing	5-50		5-89	
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The PAL® Device Concept

Monolithic Memories' family of PAL devices gives designers a powerful tool with unique capabilities for use in new and existing logic designs. The PAL device saves time and money by solving many of the system partitioning and interface problems brought about by increases in semi-conductor device technology.

Rapid advances in large scale integration technology have led to larger and larger standard logic functions; single I.C.s now perform functions that formerly required complete circuit cards. While LSI offers many advantages, advances have been made at the expense of device flexibility. Most LSI devices still require large numbers of SSI/MSI devices for interfacing with user systems. Designers are still forced to turn to random logic for many applications.

The designer is confronted with another problem when a product is designed. Often the function is well defined and could derive significant benefits from fabrication as an integrated circuit. However, the design cycle for a custom circuit is long and the costs can be very high. This makes the risk significant enough to deter most users. The technology to support maximum flexibility combined with fast turnaround on custom logic has simply not been available. Monolithic Memories offers the programmable solution.

The PAL device family offers a fresh approach to using fuse programmable logic. PAL circuits are a conceptually unified group of devices which combine programmable flexibility with high speed and an extensive selection of interface options. PAL devices can lower inventory, cut design cycles and provide high complexity with maximum flexibility. These features, combined with lower package count and high reliability, truly make the PAL device a circuit designer's best friend.

5

The PAL Device—Teaching Old PROMs New Tricks



Monolithic Memories developed the modern PROM and introduced many of the architectures and techniques now regarded as industry standards. As the world's largest PROM manufacturer, Monolithic Memories has the proven technology and high volume production capability required to manufacture and support the PAL device.

The PAL device is an extension of the fusible link technology pioneered by Monolithic Memories for use in bipolar PROMs. The fusible link PROM first gave the digital systems designer the power to "write on silicon". In a few seconds he was able to transform a blank PROM from a general purpose device into one containing a custom algorithm, microprogram, or Boolean transfer function. This opened up new horizons for the use of PROMs in computer control stores, character generators, data storage tables and many other applications. The wide acceptance of this technology is clearly demonstrated by today's multi-million dollar PROM market.

The key to the PROM's success is that it allows the designer to customize the chip quickly and easily to fit his unique requirements. The PAL device extends this programmable flexibility by utilizing proven fusible link technology to implement logic functions. By using PAL circuits the designer can quickly and effectively implement custom logic varying in complexity from random gates to complex arithmetic functions.

ANDs and ORs

The PAL device implements the familiar sum-of-products logic by using a programmable AND array whose output terms feed a fixed OR array. Since the sum-of-products form can express any Boolean transfer function, the PAL circuit uses are only limited by the number of terms available in the AND - OR arrays. PAL devices come in different sizes to allow for effective logic optimization.

Figure 1 shows the basic PAL device structure for a two-input, one-output logic segment. The general logic equation for this segment is:

Output =
$$(I_1 + \overline{f_1})(\overline{I_1} + \overline{f_2})(I_2 + \overline{f_3})(\overline{I_2} + \overline{f_4}) + (I_1 + \overline{f_5})(\overline{I_1} + \overline{f_6})(I_2 + \overline{f_7})(\overline{I_2} + \overline{f_8})$$

where the "f" terms represent the state of the fusible links in the PAL device AND array. An unblown link represents a logic 1. Thus:

fuse blown,
$$f = 0$$

fuse intact, $f = 1$

An unprogrammed PAL device has all fuses intact.

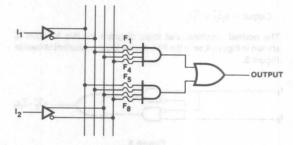


Figure 1

PAL Device Notation

Logic equations, while convenient for small functions, rapidly become cumbersome in large systems. To reduce possible confusion, complex logic networks are generally defined by logic diagrams and truth tables. Figure 2 shows the logic convention adopted to keep PAL device logic easy to understand and use, in the figure, an "x" represents an intact fuse used to perform the logic AND function. (Note: the input terms on the common line with the x's are not connected together.) The logic symbology shown in Figure 2 has been informally adopted by integrated circuit manufacturers because it clearly establishes a one-toone correspondence between the chip layout and the logic diagram. It also allows the logic diagram and truth table to be combined into a compact and easy to read form, thereby serving as a convenient shorthand for PAL circuits. The two-input, oneoutput example from Figure 1, redrawn using the new logic convention, is shown in Figure 3.

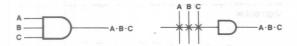


Figure 2

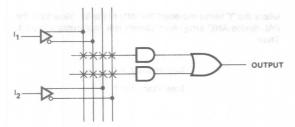


Figure 3

As a simple PAL device example, consider the implementation of the transfer function:

Output =
$$I_1\overline{I_2} + \overline{I_1}I_2$$

The normal combinatorial logic diagram for this function is shown in Figure 4, with the PAL device logic equivalent shown in Figure 5.

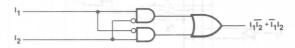


Figure 4

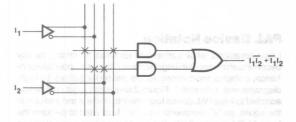


Figure 5

Using this logic convention it is now possible to compare the PAL device structure to the structure of the more familiar PROM and PLA. The basic logic structure of a PROM consists of a fixed AND array whose outputs feed a programmable OR array (Figure 6). PROMs are low-cost, easy to program, and available in a variety of sizes and organizations. They are most commonly

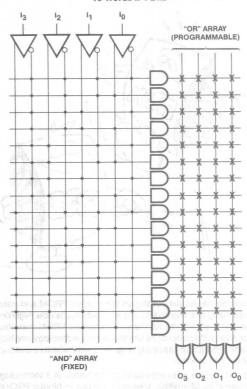


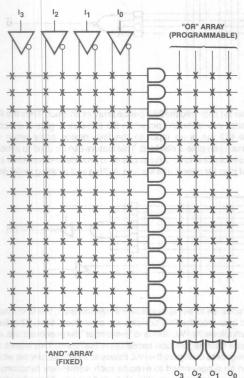
Figure 6

used to store computer programs and data. In these applications the fixed input is a computer memory address; the output is the contents of that memory location.

The basic logic structure of the PLA consists of a programmable AND array whose outputs feed a programmable OR array (Figure 7). Since the designer has complete control over all inputs and outputs, the PLA provides the ultimate flexibility for implementing logic functions. They are used in a wide variety of applications. However, this generality can make PLAs expensive, quite formidable to understand, and costly to program.

The basic logic structure of the PAL device, as mentioned earlier, consists of a programmable AND array whose outputs feed a fixed OR array (Figure 8). The PAL device combines much of the flexibility of the PLA with the low cost and easy programmability of the PROM. Table 1 summarizes the characteristics of the PROM, PLA, and PAL device logic families.





PAL Device 4 In•4 Out•16 Products

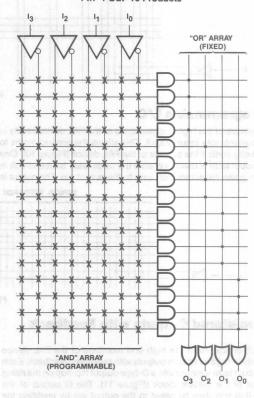


Figure 7

Figure 8

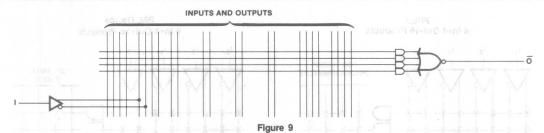
	AND	OR	OUTPUT OPTIONS
PROM	Fixed	Prog	TS,OC
FPLA	Prog	Prog	TS, OC, Prog. Polarity
FPGA	Prog	None	TS, OC, Prog. Polarity
FPLS	Prog	Prog	TS, Registered Feedback, I/O
PAL Device	Prog	Fixed	TS, Registered Feedback, I/O Prog. Polarity

PAL Device Circuits For Every Task

The members of the PAL device family and their characteristics are summarized in the PAL device menu. They are designed to cover the spectrum of logic functions at reduced cost and lower package count. This allows the designer to select the PAL device that best fits his application. PAL device units come in the following basic configurations:

Logic Arrays

PAL device logic arrays are available in sizes from 6x16 (6 input terms, 16 output terms) to 64x32, with both active high and active low output configurations available (ref. PAL device menu). This wide variety of input/output formats allows the PAL device to replace many different sized blocks of combinatorial logic with single packages.



Programmable I/O

A feature of the high-end members of the PAL device family is programmable input/output. This allows the product terms to directly control the outputs of the PAL device (Figure 10). One product term is used to enable the three-state buffer, which in turn gates the summation term to the output pin. The output is

also fed back into the PAL device array as an input. Thus the PAL device drives the I/O pin when the three-state gate is enabled; the I/O pin is an input to the PAL device array when the three-state gate is disabled. This feature can be used to allocate available pins for I/O functions or to provide bi-directional output pins for operations such as shifting and rotating serial data.

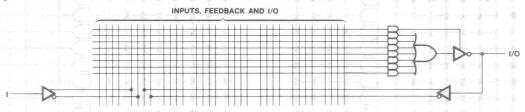
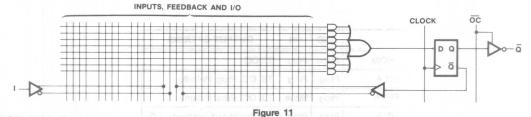


Figure 10

Another feature of the high end members of the PAL device family is registered data outputs with registered feedback. Each product term is stored into a D-type output flip-flop on the rising edge of the system clock (Figure 11). The Q output of the flip-flop can then be gated to the output pin by enabling the active low three-state buffer.

Registered Outputs with Feedback

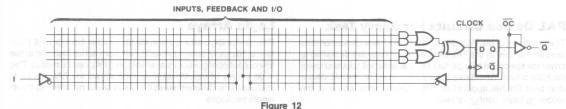
In addition to being available for transmission, the Q output is fed back into the PAL device array as an input term. This feedback allows the PAL device to "remember" the previous state, and it can alter its function based upon that state. This allows the designer to configure the PAL device as a state sequencer which can be programmed to execute such elementary functions as count up, count down, skip, shift, and branch. These functions can be executed by the registered PAL device at rates of up to 40 MHz



XOR PAL Devices

These PAL devices feature an exclusive-OR (XOR) function. The sum of products is segmented into two sums which are then exclusive ORed at the input of the D-type flip-flop (Figure 12). All

of the features of the Registered PAL devices are included in the XOR PAL unit. The XOR function provides an easy implementation of the HOLD operation used in counters and other state sequencers.



5

Arithmetic Gated Feedback

The arithmetic functions (add, subtract, greater than, and less than) are implemented by addition of gated feedback to the features of the XOR PAL device. The XOR at the input of the D-type flip-flop allows carrys from previous operations to be XORed with two variable sums generated by the PAL device array. The flip-flop Q output is fed back to be gated with input

terms A (Figure 13). This gated feedback provides any one of the sixteen possible Boolean combinations which are mapped in the Karnaugh map (Figure 15). Figure 14 shows how the PAL device array can be programmed to perform these sixteen operations. These features provide for versatile operations on two variables and facilitate the parallel generation of carrys necessary for fast arithmetic operations.

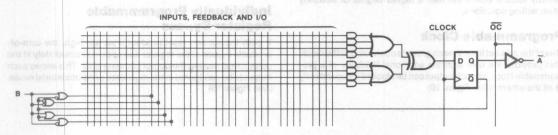


Figure 13

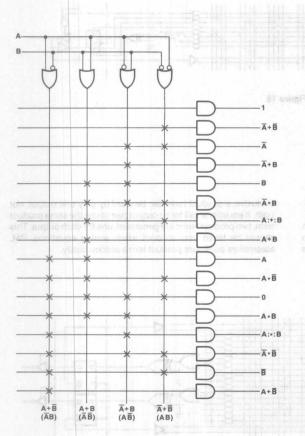


Figure 14

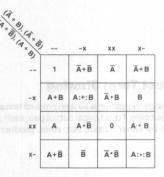


Figure 15

Programmable Output Polarity

The outputs can be programmed either active-low or active-high. This is represented by the exclusive-or gates shown in Figure 13, PAL20RA10 Logic Diagram. When the output polarity fuse is blown, the lower input to the exclusive-or gate is high, so the output is active-high. Similarly, when the output polarity fuse is intact, the output is active-low. The programmable output polarity feature allows the user a higher degree of flexibility when writing equations.

Programmable Clock

One of the product lines in each group is connected to the clock. This provides the user with the additional flexibility of a programmable clock, so each output can be clocked independently of all the others. (See Figure 16)

Programmable Set and Reset

Two product lines are dedicated to asynchronous set and reset. If the set product line is high, the register output becomes a logic 1. If the reset product line is high, the register output becomes a logic 0. The operation of the programmable set and reset overrides the clock. (See Figure 16)

Individually Programmable Register Bypass

If both the set and reset product lines are high, the sum-ofproducts bypasses the register and appears immediately at the output, thus making the output combinatorial. This allows each output to be configured in the registered or combinatorial mode. (See Figure 16)

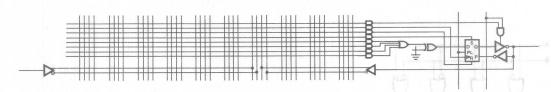


Figure 16

Product Term Sharing

The basic configuration is sixteen product terms shared between two output cells. For a typical output pair, each product term can be used by either output; but, since product term sharing is exclusive, a product term can be used by only one output, not both. If equations call for an output pair to use the same product term, two product terms are generated, one for each output. This should be taken into account when writing equations. PAL assemblers configure product terms automatically.

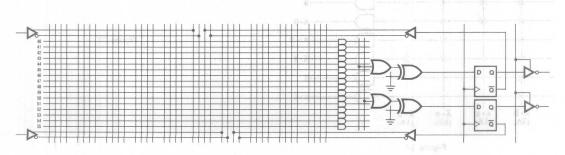


Figure 17

PAL Device Programming

PAL devices can be programmed in most standard PROM programmers with the addition of a PAL device personality card. For details on programming equipment, see the PAL Device Programmer Reference Guide in this databook.

PALASM (PAL Device Assembler)

PALASM is the software used to define, simulate, build, and test PAL device units. PALASM accepts the PAL device Design Specification as an input file. It verifies the design against an optional function table and generates the fuse plot which is used to program the PAL devices. PALASM is available upon request for many computers.

HAL (Hard Array Logic) Device

The HAL device family is the mask programmed version of a PAL device. The HAL device is to a PAL device just as a ROM is to a PROM. A standard wafer is fabricated as far as the metal mask. Then a custom metal mask is used to fabricate aluminum

links for a HAL device instead of the programmable TiW fuses used in a PAL device.

PAL Device Technology

PAL circuits are manufactured using the proven TTL Schottky bipolar TiW fuse process to make fusible-link PROMs. An NPN emitter follower array forms the programmable AND array. PNP inputs provide high impedance inputs (0.25 mA max) to the array. All outputs are standard TTL drivers with internal active pull-up transistors.

PAL Device Data Security

The circuitry used for programming and logic verification can be used at any time to determine the logic pattern stored in the PAL device array. For security, the PAL device has a "last fuse" which can be blown to disable the verification logic. This provides a significant deterrent to potential copiers, and it can be used to protect proprietary designs.



PAL Device Part Numbers

The PAL device part number is unique in that the part number code also defines the part's logic operation. The PAL device numbering system is shown in Figure 17. For example, a PAL 14L4CN would be a 14-input term, 4-output term, active-low PAL device with a commercial temperature range packaged in a 20-pin plastic DIP.

The electronic dice game is simply constructed using a free running oscillator whose output is used to drive two asyn-

chronous modulo six counters. When the user "rolls" the dice (presses a button), the current state of the counters is decoded and latched into a display resembling the pattern seen on an ordinary pair of dice.

A conventional logic diagram for the dice game is shown in Figure 16. It is implemented using standard TTL, SSI and MSI parts, with a total I.C. count of eight: six quad gate packages and two quad D-latches. Looks like a nice clean logic design, right? Wrong!!

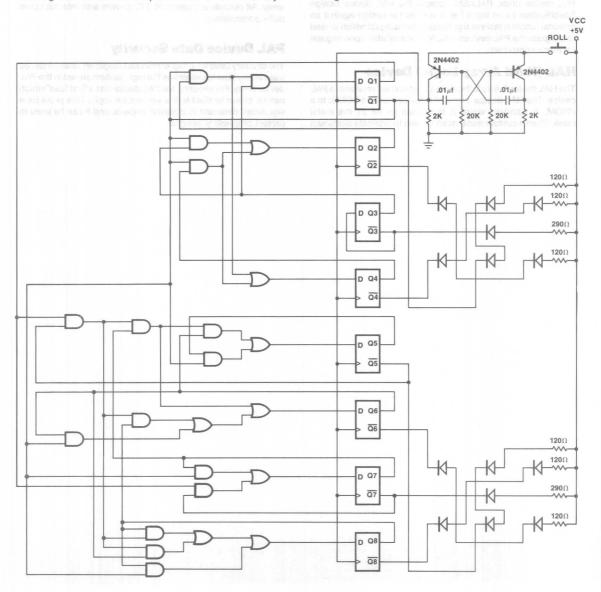
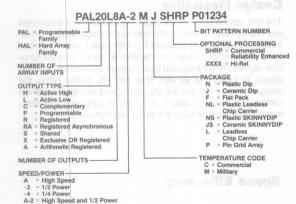


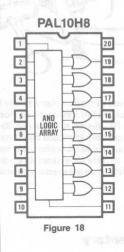
Figure 16



PAL Device Logic Symbols

A-4 = High Speed and 1/4 Power

The logic symbols for each of the individual PAL devices gives a concise functional description of the PAL device logic function. This symbol makes a convenient reference when selecting the PAL device that best fits a specific application. Figure 18 shows the logic symbol for a PAL10H8 array.



A PAL Device Example

As an example of how the PAL device enables the designer to reduce costs and simplify logic design, consider the design of a simple, high-volume consumer product: an electronic dice game. This type of product will be produced in extremely high volume, so it is essential that every possible production cost be minimized.

PAL Device Goes to the Casino

A brief examination of Figure 16 reveals two basic facts: first, the circuit contains mostly simple, combinatorial logic, and second, it uses a clocked state transition sequence. Remembering that the PAL device family contains ample provision for these features, the PAL device catalog is consulted. The PAL16R8 has all the required functions, and the entire logic content of the circuit can be programmed into a single PAL device shown in Figure 19.

In this example, the PAL device effected an eight-to-one package count reduction and a significant cost savings. This is typical of the power and cost-effective performance that the PAL device family brings to logic design.

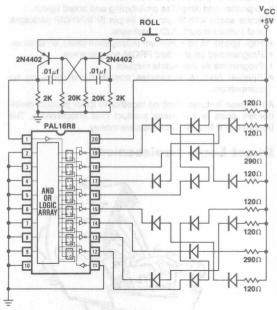


Figure 19

Advantages of Using PAL Devices



The PAL device has a unique place in the world of logic design. Not only does it offer many advantages over conventional logic, it also provides many features not found anywhere else. Among the benefits of the PAL device family:

- Programmable replacement for conventional TTL logic.
- Reduces IC inventories substantially and simplifies their control.
- Reduces chip count by at least 4 to 1.
- Expedites and simplifies prototyping and board layout.
- Saves space with 20-pin and 24-pin SKINNYDIP packages, and surface-mount PLCC packages.
- High speed: 15 ns maximum propagation delay, on B series.
- Programmed on standard PROM programmers.
- · Programmable three-state outputs.
- Special feature eliminates possibility of copying by competitors.

All of these features combine together to lower product development costs and increase product cost effectiveness. The bottom line is that PAL devices save money.

Direct Logic Replacement



In both new and existing designs, the PAL device can be used to replace various logic functions. This allows the designer to optimize a circuit in many ways never before possible. The PAL device is particularly effective when used to provide interfaces required by many LSI functions. The combination of PAL device flexibility and LSI function density makes a powerful team.

Design Flexibility

The PAL device offers the systems logic designer a whole new world of options. Until now, the decision on logic system implementation was usually between SSI/MSI logic functions on one hand and microprocessors on the other. In many cases the function required is too awkward to implement the first way and too simple to justify the second. Now the PAL device offers the designer high functional density, high speed, and low cost. Even better, PAL devices come in a variety of sizes and functions, thereby further increasing the designer's options.

Space Efficiency



By allowing designers to replace many simple logic functions with single packages, the PAL device allows more compact P.C. board layouts. The PAL device space-saving 20-pin and 24-pin SKINNYDIP packages help to reduce board area further while simplifying board layout and fabrication. this means that many multi-card systems can now be reduced to one or two cards, and that can make the difference between a profitable success or an expensive disaster.

Smaller Inventory

The PAL device family can be used to replace up to 90% of the conventional TTL family. This considerably lowers both shelving and inventory cataloging requirements. In addition, small custom modifications to the standard functions are easy for PAL device users, but not so easy for standard TTL users.



High Speed

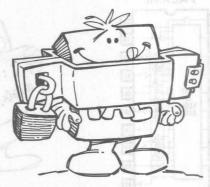


The PAL device family runs faster than or equal to the best of bipolar logic circuits. This makes the PAL device the ideal choice for most logical operations or control sequence which requires a medium complexity and high speed. Also, in many microcomputer systems, the PAL device can be used to handle high-speed data interfaces that are not feasible for the microprocessor alone. This can be used to significantly extend the capabilities of the low-cost, low-speed NMOS microprocessors into areas formerly requiring high-cost bipolar microprocessors.

Easy Programming

The members of the PAL device family can be quickly and easily programmed using standard PROM programmers. This allows designers to use PAL devices with a minimum investment in special equipment. Many types of programmable logic, such as the FPLA, require an expensive, dedicated programmer.

Secure Data



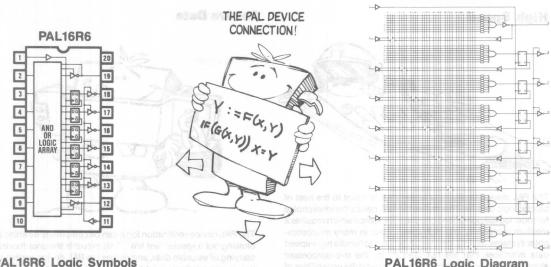
The PAL device verification logic can be completely disabled by blowing out a special "last link". This prevents the unauthorized copying of valuable data, and makes the PAL device perfect for use in any application where data integrity must be carefully guarded.

Summary

The PAL device family of logic devices offers logic designers new options in the implementation of sequential and combinatorial logic designs. The family is fast, compact, flexible, and easy to use in both new and existing designs. It promises to reduce costs in most areas of design and production with a corresponding increase in product profitability.

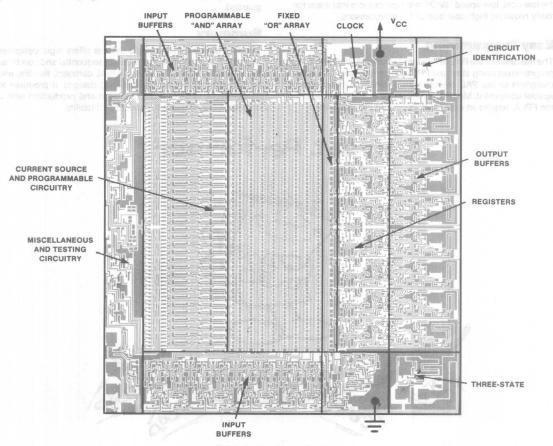
A Great Performer!





PAL16R6 Logic Symbols

PAL16R6 Logic Diagram



PAL® (Programmable Array Logic) Devices HAL® (Hard Array Logic) Devices

Features/Benefits

- Reduces SSI/MSI chip count greater than 5 to 1
- Saves space with SKINNYDIP® packages
- Reduces IC inventories substantially
- Expedites and simplifies prototyping and board layout
- PALASM®2 silicon compiler provides easy design entry
- . Security fuse reduces possibility of copying by competitors

Description

The PAL device family utilizes an advanced Schottky TTL process and the Bipolar PROM fusible link technology to provide user-programmable logic for replacing conventional SSI/MSI gates and flip-flops at reduced chip count.

The HAL device family utilizes standard Low-Power Schottky TTL process and automated mask pattern generation directly from logic equations to provide a semi-custom gate array for replacing conventional SSI/MSI gates and flip-flops at reduced chip count.

The PAL device lets the systems engineer "design his own chip" by blowing fusible links to configure AND and OR gates to perform his desired logic function. Complex interconnections which previously required time-consuming layout are thus "lifted" from PC board etch and placed on silicon where they can be easily modified during prototype check-out or production.

The PAL/HAL device transfer function is the familiar sum of products. Like the PROM, the PAL device has a single array of fusible links. Unlike the PROM, the PAL device is a programmable AND array driving a fixed OR array (the PROM is a fixed AND array driving a programmable OR array).

In addition the PAL/HAL device provides these options:

- Variable input/output pin ratio
- Programmable three-state outputs
- · Registers with feedback
- Arithmetic capability
- Exclusive-OR gates

Unused input pins should be tied directly to V_{CC} or GND. Product terms with all fuses blown assume the logical high state, and product terms connected to both true and complement of any single input assume the logical low state. Registers consist of D-type flip-flops which are loaded on the low-to-high transition of the clock. PAL/HAL device Logic Diagrams are shown with all fuses blown, enabling the designer to use the diagrams as coding sheets. PALASM software automatically generates a similar diagram, called the fuse plot.

The entire PAL device family is programmed using inexpensive conventional PROM programmers with appropriate personality and socket adapter cards. Once the PAL device is programmed and verified, two additional fuses may be blown to defeat verification. This feature gives the user a proprietary circuit which is very difficult to copy.

To design a HAL, the user first programs and debugs a PAL device using PALASM and the "PAL DEVICE DESIGN SPECIFICATION" standard format. This specification is submitted to Monolithic Memories where it is computer-processed and assigned a bit pattern number, e.g., H01234.

Monolithic Memories will provide a PAL device sample for customer qualification. The user then submits a purchase order for a HAL of the specified bit pattern number, e.g., HAL18L4 H01234. For details on ordering HAL devices, please refer to the brochure, *ProPAL*, *HAL*, and *ZHAL Devices: The Logical Solutions for Volume Programmable Logic*, available from Monolithic Memories.

PAL* (Programmable Array Logic), PALASM*, HAL* and SKINNYDIP* are registered trademarks of Monolithic Memories.

HMSI** is a trademark of Monolithic Memories.

Outputs within a bank must either be all registered or all combinatorial. Whether or not a bank of registers is bypassed depends on how the outputs are defined in the equations. A colon followed by an equal sign [:=] specifies a registered output with feedback which is updated after the low-to-high transition of the clock. An equal sign [=] defines a combinatorial output which bypasses the register. Registers are bypassed in banks of eight. Bypassing a bank of registers eliminates the feedback lines for those outputs.

Output Polarity

Output polarity is defined by comparison of the pin list and the equations. If the logic sense of a specific output in the pin list is different from the logic sense of that output as defined by its equation, the output is inverted or active low polarity. If the logic sense of a specific output in the pin list is the same as the logic sense of that output as defined by its equation, the output is active high polarity. Note that the P, RA, RS, and MegaPAL devices have programmable output polarity.

Product Term Sharing (RS, MegaPAL Devices)

The basic configuration is sixteen product terms shared between two output cells. For a typical output pair, each product term can be used by either output; but, since product term sharing is exclusive, a product term can be used by only one output, not both. If equations call for an output pair to use the same product term, two product terms are generated, one for each output. This should be taken into account when writing equations. PAL device assemblers configure product terms automatically.

Product Term Editing

A unique feature of product term sharing is the ability to edit the design after the device has been programmed. Without this feature, a new PAL device had to be programmed if the user needed to change his design. Product term editing allows the user to delete an unwanted product term and reprogram a previously unused product term to the desired fuse pattern. This feature is made possible by the product term sharing architecture. Since each product term can be routed to either output in a given pair by selecting one of two steering fuses, it is possible to blow both of the steering fuses thereby completely disabling that product term. Once disabled, that product term is powered down, saving typically 0.25 mA. The desired change may now be programmed into one of the previously unused product terms corresponding to that output pair. Additional edits can be made as long as there are unused product terms for the output in question.

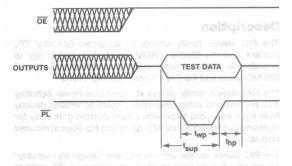
PRESET Feature (PAL64R32 only)

Register banks of eight may be PRESET to all highs on the outputs by setting the PRESET pin (PS) to a Low level. Note from the Logic Diagram that when the state of an output is High, the state of the register is Low due to the inverting tri-state buffer.

(RA, MegaPAL Devices)

Preload pins have been added to enable the testability of each state in state-machine design. Typically, for a modulo-n counter or a state machine there are many unreachable states for the registers. These states, and the logic which controls them are untestable without a way to "set-in" the desired starting state of the registers. In addition, long test sequences are sometimes needed to test a state machine simply to reach those starting states which are legal. Since complete logic verification is needed to ensure the proper exit from "illegal" or unused states, a way to enter these states must be provided. The ability to preload a given bank of registers is provided in this device.

To use the preload feature, several steps must be followed. First, a high level on an assertive-low output enable pin disables the outputs for that bank of registers. Next, the data to be loaded is presented at the output pins. This data is then loaded into the register by placing a low level on the PRELOAD pin. PRELOAD is asynchronous with respect to the clock.



Programmable Set and Reset (RA Family only)

In each SMAC, two product lines are dedicated to asynchronous set and reset. If the set product line is high, the register output becomes a logic 1. If the reset product line is high, the register output becomes a logic 0. The operation of the programmable set and reset overrides the clock. Note that set and reset are in reference to the register, independent of polarity.

Individually Programmable Register Bypass (RA Family only)

If both the set and reset product lines are high, the sum-ofproducts bypasses the register and appears immediately at the output, thus making the output combinatorial. This allows each output to be configured in the registered or combinatorial mode.

Programmable Clock (RA Family only)

One of the product lines in each group is connected to the clock. This provides the user with the additional flexibility of a programmable clock, so each output can be clocked independently of all the others.

Monolithic Memories PAL® Device Menu

				DESCRIPTION	AS 221	MAXI	MUM
FAMILY	PART NUMBER	PACKAGE		OUTPL	JTS	tpD*	lcc
		THE STATE OF THE S	INPUTS	COMBINATORIAL	REGISTERED	ns	mA
Meta Juni	PAL10H8 PAL12H6 PAL14H4	INSCENSED	10 12 14	8 6 4	_	35 35 35	
Small 20 Combinatorial	PAL16H2 PAL16C1 PAL10L8 PAL12L6 PAL14L4 PAL16L2	20N, J, NL, F, L	14 16 16 10 12 14 16	2 2 8 6 4	07.181.144 1.081.144 1.081.14 1.081.14 1.081.14	35 40 35 35 35 35	90
08 53	PAL10H8-2	67	10	8	ANTIQUE ANTIQUE	19	toured.
Small 20-2 Combinatorial	PAL12H6-2 PAL14H4-2 PAL16H2-2 PAL16C1-2 PAL10L8-2 PAL12L6-2	20N, J, NL, F, L	12 14 16 16 10 12	4 2 2 2	7-2 JOS. 17 7-705. 17 7-705. 17 7-835. 17	60	45
	PAL14L4-2 PAL16L2-2		14 16	4 2	78 PER 18		multipri
Medium 20 Standard	PAL16L8 PAL16R8 PAL16R6 PAL16R4	20N, J, NL	16 16 16 16	8 2 4	8 6 4	35	180
Medium 20A Standard	PAL16L8A PAL16R8A PAL16R6A PAL16R4A	20N, J, NL, W, L	16 16 16 16	$\frac{1}{2}$	8 6 4	25	180
Medium 20A-2 Standard	PAL16L8A-2 PAL16R8A-2 PAL16R6A-2 PAL16R4A-2	20N, J, NL, F, L	16 16 16 16	8 2 4	8 6 4	35	90
Medium 20A-4 Standard	PAL16L8A-4 PAL16R8A-4 PAL16R6A-4 PAL16R4A-4	20N, J, NL, F, L	16 16 16 16	8 2 4	8 6 4	55	50
Medium 20B Standard	PAL16L8B PAL16R8B PAL16R6B PAL16R4B	20N, J, NL, W, L	16 16 16 16	The Zan State of	8 6 4	15	180
Medium 20B-2 Standard	PAL16L8B-2 PAL16R8B-2 PAL16R6B-2 PAL16R4B-2	20N, J, NL, W, L	16 16 16 16	8 2 4	8 6 4	25	90
Medium 20B-4 Standard	PAL16L8B-4 PAL16R8B-4 PAL16R6B-4 PAL16R4B-4	20N, J, NL, W, L	16 16 16 16	8 2 4	8 6 4	35	55
Medium 20AP Programmable Polarity	PAL16P8A PAL16RP8A PAL16RP6A PAL16RP4A	20N, J, NL	16 16 16 16	8 2 4	8 6 4	25/30**	180
Large 20 Arithmetic	PAL16X4 PAL16A4	20N, J, NL, F, L	16 16	4 4	4 4	40	225 240
Large 20RA Asynchronous	PAL16RA8	20N, J, NL	16	_	8	30/35**	170

^{*} Minimum commercial \mathbf{t}_{SU} for devices with all registered outputs.

^{**} Polarity fuse programmed (active High).

N = Plastic DIP NS = Plastic SKINNYDIP

J = Ceramic DIP

JS = Ceramic SKINNYDIP

NL = Plastic Leaded Chip Carrier (PLCC)

P = Pin Grid Array
L = Leadless Chip Carrier (LCC)

W = Cerpack

F = Ceramic Solder Seal Flat Pack

Monolithic Memories PAL® Device Menu

PAL Circuit Series 24

	271	9100		DESCRIPTION	P V. UKY THIS	MAXI	MUM
FAMILY	PART NUMBER	PACKAGE	93 -	OUTPL	JTS	t _{PD} *	lcc
		8	INPUTS	COMBINATORIAL	REGISTERED	ns	mA
Small 24 Combinatorial	PAL12L10 PAL14L8 PAL16L6 PAL18L4 PAL20L2 PAL20C1	24NS, JS, W, 28NL, 28L	10 14 16 18 20 20	10 8 6 4 2 2		40	100
Small 24A Decoder	PAL6L16A PAL8L14A	24NS,JS, 28NL	6 8	16 14	<u> </u>	25	90
Medium 24A Standard	PAL20L8A PAL20R8A PAL20R6A PAL20R4A	24NS, JS, W, 28NL, 28L	20 20 20 20	$\frac{1}{2}$	8 6 4	25 S-0	210
Medium 24A-2 Standard	PAL20L8A-2 PAL20R8A-2 PAL20R6A-2 PAL20R4A-2	24NS, JS, W, 28NL, 28L	20 20 20 20	8 2 4	8 6 4	35	105
Medium 24B Standard	PAL20L8B PAL20R8B PAL20R6B PAL20R4B	24NS, JS, W, 28NL, 28L	20 20 20 20	8 2 4		15	210
Medium 24X Exclusive OR	PAL20L10 PAL20X10 PAL20X8 PAL20X4	24NS, JS, W, 28NL, 28L	20 20 20 20	10 2 4	10 8 4	50	165 180 180 180
Medium 24XA Exclusive OR	PAL20L10A PAL20X10A PAL20X8A PAL20X4A	24NS, JS, W, 28NL, 28L	20 20 20 20	10 - 2 6	10 8 4	30	165 180 180 180
Large 24RS Shared Product Terms	PAL20S10 PAL20RS10 PAL20RS8 PAL20RS4	24NS, JS, W, 28NL, 28L	20 20 20 20	10 - 2 6	10 8 4	35/40** 35 35/40** 35/40**	240 240 240 240
Large 24RA Asynchronous	PAL20RA10	24NS, JS, W, 28NL, 28L	20	- Mile Ma	10	30/35**	200

PAL Circuit Series MegaPAL™

	30 3	8		MAXIMUM		
FAMILY	PART NUMBER	PACKAGE	INPUTS	REGISTERED OUTPUTS	t _{PD} *	I _{CC} mA
1500 Gates	PAL32R16	40N, J, 44NL, 44L	32	16	40/45**	280
5000 Gates	PAL64R32	88P, 84L	64	32	50/55**	640

 $[\]ensuremath{^{\star}}$ Minimum commercial $\ensuremath{t_{\text{SU}}}$ for devices with all registered outputs.

^{**} Polarity fuse programmed (active High).

fMAX Parameters

The parameter f_{MAX} is the maximum speed at which the PAL device is guaranteed to operate. Because flexibility inherent to PAL devices allows a choice of clocked flip-flop designs, for the convenience of the user, f_{MAX} for the B-speed devices is specified to address two major classes of synchronous designs.

The simplest type of synchronous design can be described as a data path application. In this case, data is presented to the data terminal of the flip-flop and clocked through; no feedback is

employed (Figure 1). Under these conditions, the frequency of operation is limited by the greater of the data setup time (t_{SU}) or the minimum clock period (t_{W} high + t_{W} low). This parameter is designated t_{MAX} (no feedback).

For synchronous sequential designs, i.e., state machines, where logical feedback is required, inputs to flip-flop data terminals originate from the device input pins or flip-flop outputs via the internal feeback paths (Figure 2). Under these conditions, f_{MAX} is defined as the reciprocal of $(t_{SU}+t_{CLK})$ and is designated f_{MAX} (feedback).

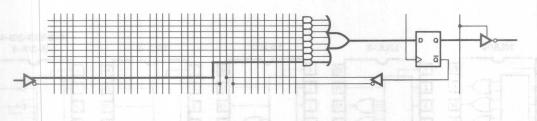


Figure 1. No Feedback

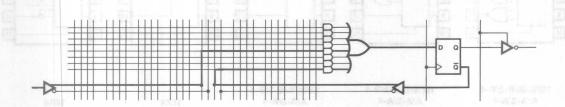
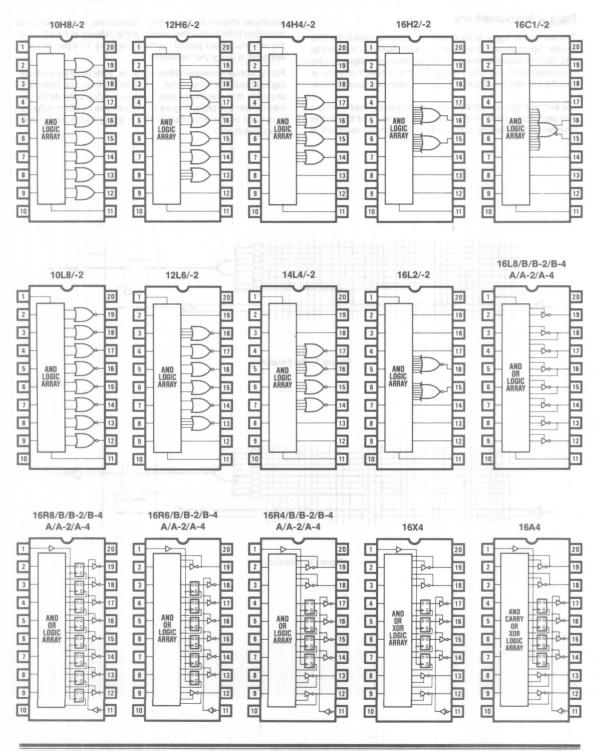
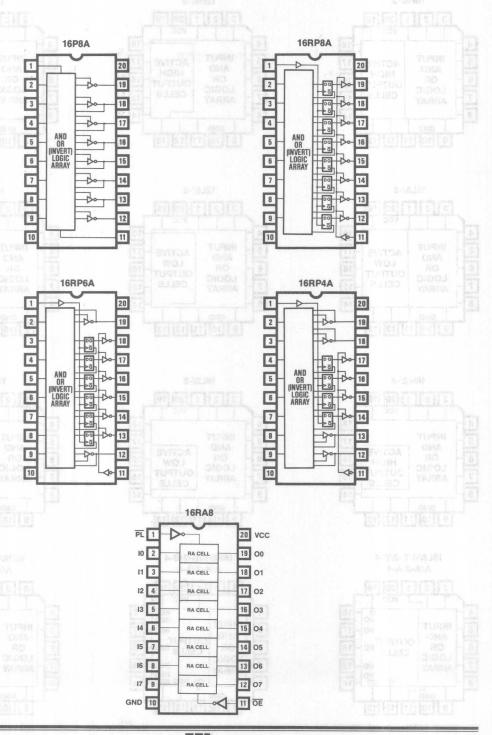
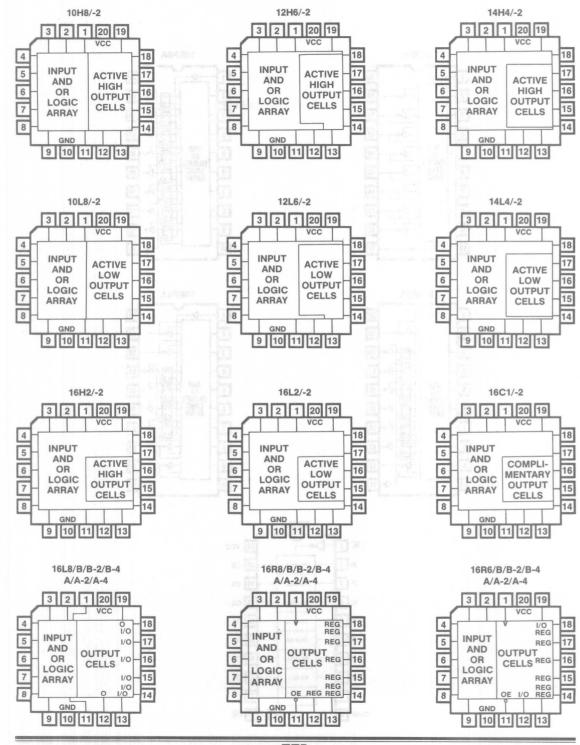
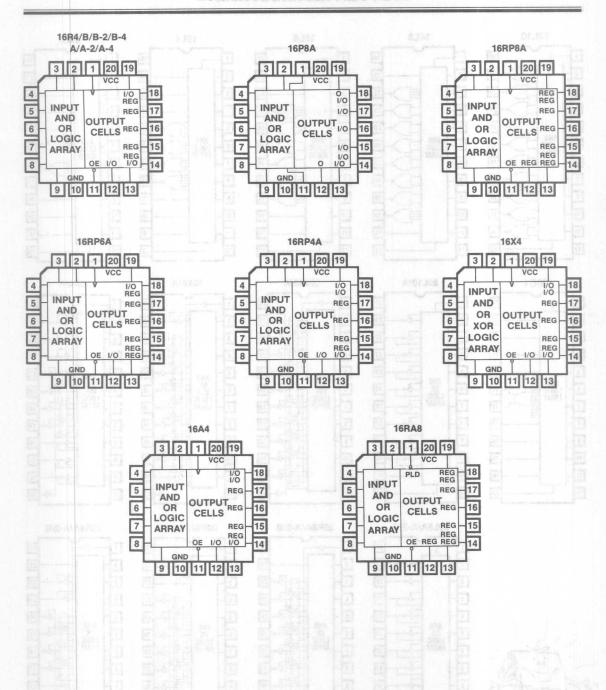


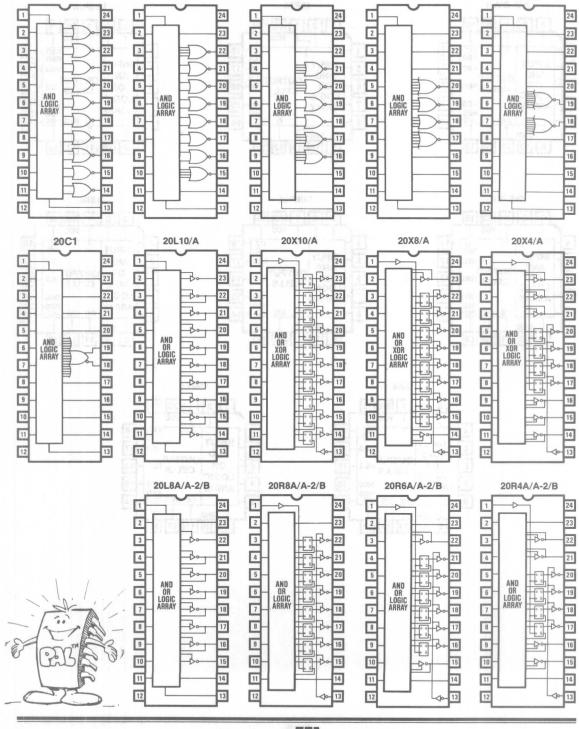
Figure 2. Feedback



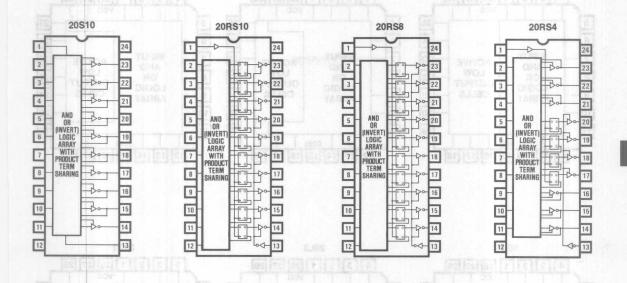


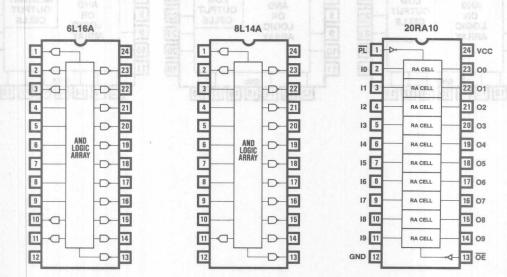


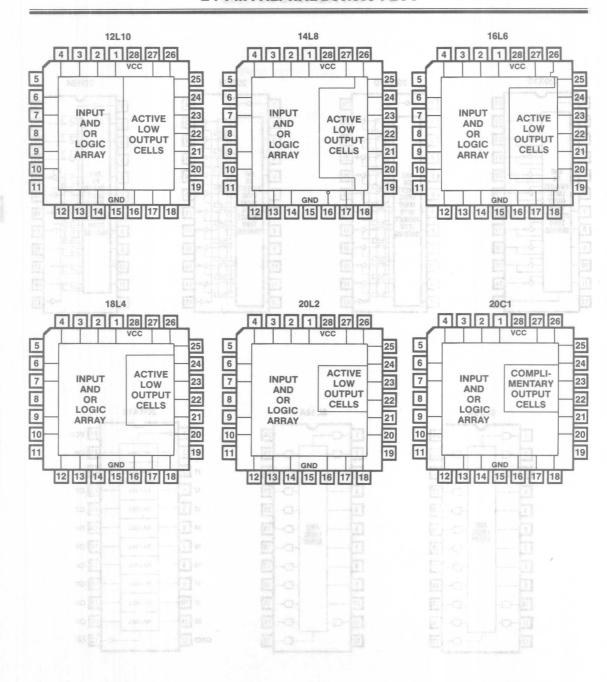




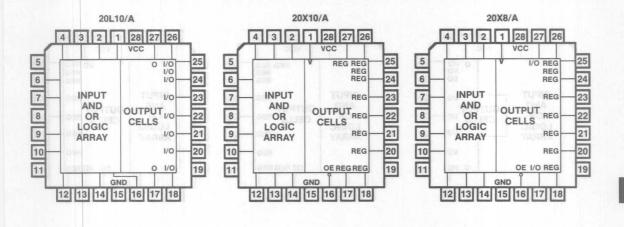


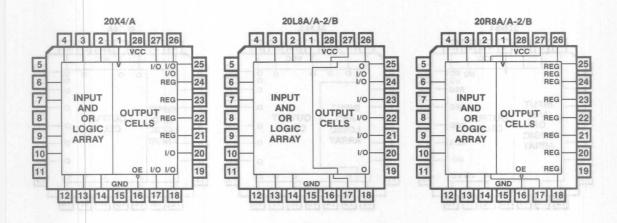


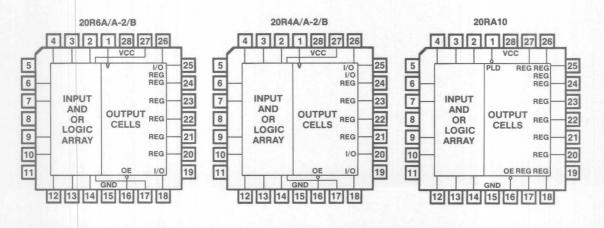


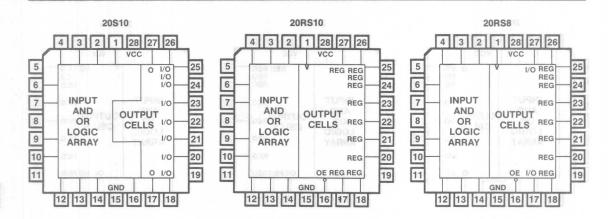


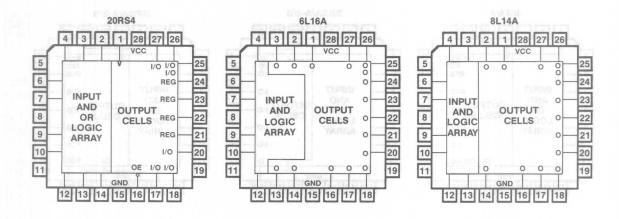


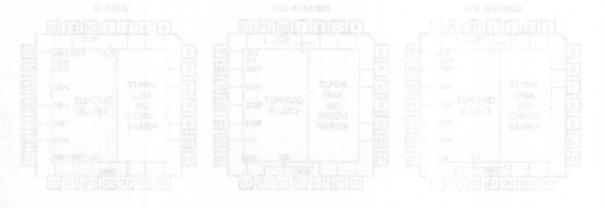




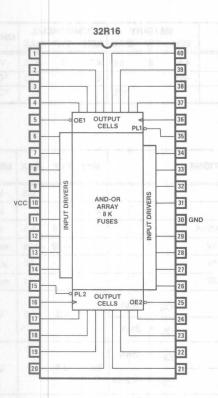


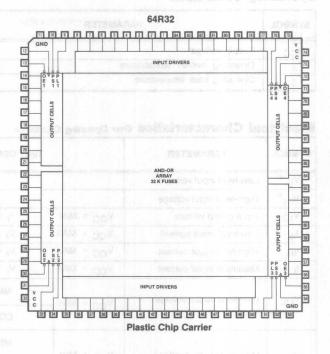


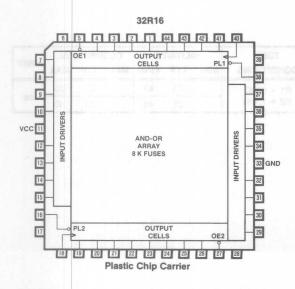












Standard PAL/HAL Devices Series 20

SYMBOL	PARAMETER	MIN	TYP	MAX	12. 10.00	MMER(MAX	UNIT
VCC	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
TA	Operating free-air temperature	-55			0		75	°C
TC	Operating case temperature			125			and the same	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS	(a)	MIN	TYP	MAX	UNIT
V _{IL} *	Low-level input voltage		- Ini		Total		0.8	V
V _{IH} *	High-level input voltage	2		200	2	15		V
VIC	Input clamp voltage	V _{CC} = MIN	I _I = -18mA	Tar .	12.11	-0.8	-1.5	V
IIL	Low-level input current	V _{CC} = MAX	V ₁ = 0.4V			-0.02	-0.25	mA
T _{IH}	High-level input current	V _{CC} = MAX	V _I = 2.4V				25	μΑ
41	Maximum input current	V _{CC} = MAX	V _I = 5.5V	Fig.			1	mA
VOL	Low-level output voltage	V _{CC} = MIN	MIL	I _{OL} = 8mA	15 14	0.3	0.5	V
PERM	on de la company de la comp		COM	I _{OL} = 8mA				
.,		V MINI	MIL	I _{OH} = -2mA	0.4	0.0	-100	.,
VOH	High-level output voltage	V _{CC} = MIN	СОМ	I _{OH} = -3.2mA	2.4	2.8		V
los	Output short-circuit current **	V _{CC} = 5V		VO = 0V	-30	-70	-130	mA
Icc	Supply current	V _{CC} = MAX				55	90	mA

Switching Characteristics

SYMBOL	PARAMETER		TEST	MILITARY			COI	UNIT		
			CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
	Input or feed-	Except 16C1	R1 = 560Ω		25	45		25	35	23
^t PD	back to output	16C1	$R2 = 1.1k\Omega$		25	45		25	40	ns

Operating Conditions

SYMBOL	PARAMETER	AND TERRAM	RY	COI	MER	CIAL	UNIT	
STMBOL	TARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	Oldii
VCC	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
TA	Operating free-air temperature	-55	11	125	0	e is to the	75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TI	EST CONDITIONS		MIN TYP	MAX	UNIT
V _{IL} *	Low-level input voltage					0.8	V
VIH*	High-level input voltage			A STATE OF THE STATE OF	2		V
VIC	Input clamp voltage	V _{CC} = MIN	I ₁ = -18mA		-0.8	-1.5	V
IL	Low-level input current	V _{CC} = MAX	V ₁ = 0.4V		-0.02	-0.25	mA
ΉΗ	High-level input current	V _{CC} = MAX	V ₁ = 2.4V	ebellov	luar. Isve-riolin	25	μΑ
4/	Maximum input current	V _{CC} = MAX	V _I = 5.5V	SURF	input clama vo	1	mA
VOL	Low-level output voltage	V _{CC} = MIN	Mil - DOV	I _{OL} = 4mA	liga inte 0.3	0.5	V
Am I	V a.	AGG - MINA	Com 4 = 50V	I _{OL} = 4mA	gor muribalis		
Vari	High-level output voltage	= 101 - MIN	Mil Mil OOV	I _{OH} = -1mA	2.4 2.8		oV.
VOH	A S S S S S S S S S S S S S S S S S S S	V _{CC} = MIN	Com	I _{OH} = -1mA	gare swel-ripin		IOV
los	Output short-circuit current **	V _{CC} = 5V		VO = 0V	-30 -70	-130	mA
lcc	Supply current	V _{CC} = MAX	AAM = DOV	Diag(ND)	30	45	mA

SYMBOL	PARAMETER	TEST	MILITARY			CO	UNIT		
STMBOL	FARAMETER	IEST	MIN	TYP	MAX	MIN	TYP	MAX	ONIT
^t PD	Input or feedback to output	R1 = $1.12k\Omega$ R2 = $2.2k\Omega$		45	80	Wall had	45	60	ns

SYMBOL	CHARGE YEAT PARAMETER			IILITAR 4/A4 O TYP	55	COM	MMER TYP	CIAL	UNIT
VCC	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
A las	Wildle - 4 - 10 - 1-2	Low	25	10	711	25	10	0	7
tw	Width of clock	High	25	10		25	10		ns
	Set up time from	16R8, 16R6, 16R4	45	25		35	25		
tsu	input or feedback to clock	16X4, 16A4	55	30		45	30		ns
th	Hold time	ang Conditons	0	-15	4870	0	-15	(SECOR	ns
TA	Operating free-air temperature	PROCEEDINGS TEST	-55		unit.	0	162	75	°C
TC	Operating case temperature	*			125				°C

Electrical Characteristics

SYMBOL	PARAMETER		TEST	CONDITIONS	MIN	TYP	MAX	UNIT
V _{IL} *	Low-level input voltage			30.14 J.J. J. J	- major	1027521	0.8	V
VIH*	High-level input voltage	10.3 - 1		WWW - DOY	2	134-11-12	1937-1	V
VIC	Input clamp voltage	VCC = MIN	7	Ij 0 = -18 mA	i hugai	-0.8	-1.5	V
ILT.	Low-level input current	V _{CC} = MAX		V _I = 0.4 V		-0.02	-0.25	mA
MiHt 80	High-level input current	V _{CC} = MAX		V _I = 2.4 V	TI TH	level-v	25	μΑ
lj .	Maximum input current	V _{CC} = MAX)	V _I = 5.5 V			1	mA
Va	Low level output voltage	V _{CC} = MIN Mil 16X4/A4 only I _{OL} = 12 mA 0.3		0.3	0.5	V		
VOL	Low-level output voltage VCC = MIN		Com	I _{OL} = 24 mA	0.0 0.0			l v
M	High land autout saltenes and	Manage MAINE	Mil 16X4/A4 only IOH = -2 mA		VCC = MIN Mil 16X4/A4 only IOH = -2 mA 2.4 2.8		San A	V
VOH	High-level output voltage	VCC = MIN	Com	IOH = -3.2 mA	2.4	2.8		V
lozL†	0.00 AV = 0.00 AV	V	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	V _O = 0.4 V	dur-Ra	As Tuq	-100	μΑ
lozh†	Off-state output current	V _{CC} = MAX		XAM = VO = 2.4 V	rigire	sply or	100	μΑ
los**	Output short-circuit current	V _{CC} = 5 V		V _O = 0 V	-30	-70	-130	mA
			16R4, 16	6R6, 16R8, 16L8		120	180	
ICC	Supply current	V _{CC} = MAX	16X4	and and and and an analysis	decom	160	225	mA
	AND THE RESERVE OF THE PERSON		16A4		170 240		240	and the

SYMBOL	ga.	PARAMETER	CONDITIONS		ILITA 4/A4 C TYP	DNLY		MER		UNIT
4	Input or feed-	16R6, 16R4, 16L8						25		
tPD	back to output	16X4, 16A4			30	45		30	40	ns
tCLK	Clock to output	or feedback			15	25		15	25	ns
tpzx	Pin 11 to output	enable except 16L8			15	25		15	25	ns
tpxz	Pin 11 to output	disable except 16L8			15	25		15	25	ns
	Input to	16R6, 16R4, 16L8	$R_1 = 200 \Omega$ $R_2 = 390 \Omega$					25	35	
tPZX	output enable	16X4, 16A4	112 - 330 12		30	45		30	40	ns
	Input to	16R6, 16R4, 16L8						25	35	
tPXZ	output disable 16X4, 16A4	16X4, 16A4			30	45		30	40	ns
6	Maximum	16R8, 16R6, 16R4					16	25		N 41 1
fMAX	frequency	16X4, 16A4		12	22		14	4 22		MH:

SYMBOL	ST SE XAM OF PAR	AMETER	MIN	IILITAF TYP	MAX	COI	MMER(MAX	UNIT
VCC	Supply voltage	(A)	4.5	5	5.5	4.75	5	5.25	o.A
tw	Width of clock	Low	20	10		15	10	N L	ns
W	Width of Clock	High	20	10		15	10		ns
t _{su}	Set up time from input or feedback to clock	16R8A, 16R6A, 16R4A	30	15	on do	25	15	8	ns
th	Hold time		0	-10		0	-10	H L	ns
TA	Operating free-air temperatur	е	-55	analeçin.	IN There	0	nus eq	75	°C
TC	Operating case temperature				125		- 10		°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
VIL*	Low-level input voltage			opallov	ruo n	9/8 - W	0.8	V
VIH*	High-level input voltage			spattov	2	wel dr	iH .	V
VIC	Input clamp voltage	VCC = MIN	I _I = -18mA	500	lov or	-0.8	-1.5	V
AHL 35	Low-level input current †	V _{CC} = MAX	V ₁ = 0.4V	† friáncio	fug/i	-0.02	-0.25	mA
adin as	High-level input current †	V _{CC} = MAX	V ₁ = 2.4V	dement †	lucini. Is	gh-tevr	25	μА
Adl	Maximum input current	V _{CC} = MAX	$V_1 = 5.5V$	Inemus	ndu:	nua nel	1 1	mA
VOL	Low-level output voltage	V _{CC} = MIN	Mil	I _{OL} = 12mA	adilico	0.3	0.5	V
	Amis = Jol	moo	Com	I _{OL} = 24mA				
V	High-level output voltage	ANN.	Mil	I _{OH} = -2mA	2.4	2.8		
VOH	Ans.c== Hol	V _{CC} = MIN	Com	$I_{OH} = -3.2mA$	2.4	2.0		HOV
OZL	Non-rov			V _O = 0.4V			-100	μА
lozh	Off-state output current †	V _{CC} = MAX		V _O = 2.4V	AUDRU S	DIELS/	100	μΑ
los	Output short-circuit current **	V _{CC} = 5V	Ve = pav	VO = OV	-30	-70	-130	mA
Icc -	Supply current	V _{CC} = MAX	XAN = onV		10000	120	180	mA

CVMDOL	D.	ARAMETER	TEST	MIL	LITAR	RY	COM	MER	CIAL	UNIT
SYMBOL	CO WKENCH	ARAMETER	CONDITIONS	MIN T	TYP	MAX	MIN	TYP	MAX	UNII
t _{PD}	Input or feed- back to output	16R6A, 16R4A, 16L8A			15	30	-396	15	25	ns
tCLK	Clock to output	or feedback		0.70010	10	20	Sirght.	10	15	ns
tPZX	Pin 11 to output e	nable except 16L8A			10	25	further	10	20	ns
tPXZ	Pin 11 to output d	isable except 16L8A	R ₁ = 200 Ω	Iquaxes	11	25	bitugilu	11	20	ns
tPZX	Input to output enable	16R6A, 16R4A, 16L8A	$R_2 = 390 \Omega$	S-ABPIG	10	30	eide	10	25	ns
t _{PXZ}	Input to output disable	16R6A, 16R4A, 16L8A		SHARK	13	30	9 48	13	25	ns
fMAX	Maximum frequency	16R8A, 16R6A, 16R4A		20	40	(ens)	28.5	40	sto ent	МН

SYMBOL		PARAMETER ASS			MAX	COI	MMER O	MAX	UNIT
VCC	Supply voltage	2.4	4.5	5	5.5	4.75	5	5.25	V
	Width of clock	Low	25	10		25	10		
tw	Width of clock	High	25	10		25	10	V.	ns
^t su	Set up time from input or feedback to clock	16R6A-2 16R4A-2 16R8A-2	50	25	one of the	35	25	3	ns
th	Hold time	6	0	-15	74	0	-15	-	ns
TA	Operating free-air temperatur	е	-55	ALTERIC S	125	0	ritan bert	75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS		MIN TYP MAX	UNIT
V _{IL} *	Low-level input voltage			1,61.01	tri;ni kwal-um. 0.8	V
VIH*	High-level input voltage			te missings.	2 Imal digital	V
VIC	Input clamp voltage	V _{CC} = MIN	I _I = -18mA	3644	-0.8 -1.5	V
ALC 3	Low-level input current †	V _{CC} = MAX	V ₁ = 0.4V	S 13 13	-0.02 -0.25	mA
ЧН	High-level input current †	V _{CC} = MAX	V ₁ = 2.4V	curren !	25	μА
Apr :	Maximum input current	V _{CC} = MAX	V ₁ = 5.5V	Leur	un ii sh maski 1	mA
VOL	Low-level output voltage	V _{CC} = MIN	Mil	I _{OL} = 12mA	0.3 0.5	o'v
	Valleg a TO	me©	Com	I _{OL} = 24mA		
V	High-level output voltage	MAR - ANN	Mil	I _{OH} = -2mA	2.4 2.8	n.V.
Vон	Holland Holland	V _{CC} = MIN	Com	I _{OH} = -3.2mA	2.4 2.0	V
lozL	Off state output ourset t	V MAY	YAM =	V _O = 0.4V	-100	μΑ
lozh	Off-state output current †	V _{CC} = MAX		V _O = 2.4V	100	μΑ
los	Output short-circuit current **	V _{CC} = 5V	Ve = 50.1	VO = 0V	-30 -70 -130	mA
lcc	Supply current	V _{CC} = MAX	Vec = Max		60 90	mA

1	NI TYT YES	NAME STATE BOOK STATE	TEST	M	ILITAF	RY	COI	MMER	CIAL	UNIT
SYMBOL	PARAMETER		CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
t _{PD}	Input or feed- back to output	16L8A-2 16R6A-2 16R4A-2			25	50	To plu Regionals	25	35	ns
tCLK	Clock to output	or feedback		As tat	15	25	Terrible	15	25	ns
tPXZ/ZX	Pin 11 to output o	lisable/enable except 16L8A-2	$R_1 = 200\Omega$	ASIST	15	25	Latina	15	25	ns
t _{PZX}	Input to output enable	16L8A-2 16R6A-2 16R4A-2	$R_2 = 390\Omega$,AM	25	45	8.436	25	35 100	ns
t _{PXZ}	Input to output disable	16L8A-2 16R6A-2 16R4A-2		e Apri	25	45	e dia	25	35	ns
fMAX	Maximum frequency	16R8A-2 16R6A-2 16R4A-2		14	25	-31	16	25	gld	MHz

Quarter Power Series 20A-4 16L8A-4, 16R8A-4, 16R6A-4, 16R4A-4

Operating Conditions

SYMBOL	LARD SERMAGO PAR	RAMETER	ABI	MIN	TYP	MAX	COL	MMER C	MAX	UNIT
Vcc	Supply voltage	1.4		4.5	5	5.5	4.75	5	5.25	٧
	VALIDADE OF STORY	(1)	Low	40	20		30	20		
tw	Width of clock Hig			40	20	×	30	20		ns
t _{su}	Set up time from input or feedback to clock	16R8A-4 16R6A-4 16R4A-4	288	90	45	NYG	60	45		ns
th	Hold time		RAS	0	-15	01 TOB0	0	-15		ns
TA	Operating free-air temperatur	re		-55		125	0	a hate 1	75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
VIL*	Low-level input voltage			moltelens	2009 F (5)	as t	0.8	V
VIH*	High-level input voltage				2	-tradeción		V
VIC	Input clamp voltage	V _{CC} = MIN	I ₁ = -18mA	RETERLA	PAT .	-0.8	-1.5	V
IIL	Low-level input current †	V _{CC} = MAX	V _I = 0.4V			-0.02	-0.25	mA
ЧН	High-level input current †	V _{CC} = MAX	V ₁ = 2.4V		Gregori (Co.		25	μΑ
l ₁	Maximum input current	V _{CC} = MAX	V _I = 5.5V	эдалогч	100	ot 000	1	mA
VOL	Low-level output voltage	0.37 14 - 1401	Mil	I _{OL} = 4mA	bion 184	0.3	0.5	V
Au e	V4	VCC = MIN	Com = OoV	I _{OL} = 8mA	agritual i			191
Am		E N	Mil	I _{OH} = -1mA	-	urikeb		- 4
VOH	High-level output voltage	V _{CC} = MIN	Com	I _{OH} = -1 mA		2.8		V
lozL	Off-state output current†	V _{CC} = MAX	XAM = moV	V _O = 0.4V	ist is		-100	μΑ
IOZH	on state surput surrout	3 - 00	1/2 = 00V	V _O = 2.4V	5.5	turd 6	100	μΑ
los	Output short-circuit current**	V _{CC} = 5V	MANA	V _O = 0V	-30	-70	-130	mA
lcc	Supply current	V _{CC} = MAX				30	50	mA

SYMBOL		PARAMETER	TEST		ILITAF			MMER		UNIT
That	AND REMOVED	182			TYP	MAX	MIN	TYP	MAX	RELIVI
t _{PD}	Input or feed- back to output	16R6A-4 16R4A-4 16L8A-4	trigino of sibed	hast to	35	75	BIJA)	35	55	ns
tCLK	Clock to outpu	t or feedback		U8000)	20	45	alue	20	35	ns
t _{PXZ/ZX}	Pin 11 to output o	n 11 to output disable/enable — except 16L8A-4		dar /q	15	40	gripo U	15	30	ns
t _{PZX}	Input to output enable	16R6A-4 16R4A-4 16L8A-4	$R_1 = 800\Omega$ $R_2 = 1.56k\Omega$	181 lei	30	65	etus t	30	50	ns
t _{PXZ}	Input to output disable	16R6A-4 16R4A-4 16L8A-4			30	65	ight	30	50	ns
f _{MAX}	Maximum frequency	16R8A-4 16R6A-4 16R4A-4		8	18	venoy	11	18		МН

SYMBOL	PAR	AMETER	MIN	COMMERCIAL TYP MAX	UNIT
V _{CC}	Supply voltage	H p	4.75	5 5.25	V
	OF OF S	Low	10	6	200
t _w	Width of clock	High	10	5	ns
t _{su}	Setup time from input or feedback to clock	16R8B 16R6B 16R4B	15	10 - Burn Lines	ns
th	Hold time		0	-10	ns
TA	Operating free-air temperatur	re	0	25 75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	A many TEST	CONDITION	COMMER MIN TYP	CIAL MAX	UNIT
V _{IL} *	Low-level input voltage	100 No. 10 No. 1	EAM = and I	- International	0.8	V
V _{IH} *	High-level input voltage	168 20 1/2)	CANA	2	Z. I	V
VIC	Input clamp voltage	V _{CC} = MIN	I _I = -18 mA	-0.8	-1.5	V
I _{IL} †	Low-level input current	V _{CC} = MAX	V _I = 0.4 V	-0.02	-0.25	mA
I _{IH} †	High-level input current	V _{CC} = MAX	V _I = 2.4 V		25	μΑ
II	Maximum input current	V _{CC} = MAX	V _I = 5.5 V		1	mA
VOL	Low-level output voltage	V _{CC} = MIN	OL = 24 mA	0.3	0.5	V
Vон	High-level output voltage	V _{CC} = MIN	I _{OH} = -3.2 mA	2.4 2.8		V
lozL†	Off state output ourrent	V MAY	V _O = 0.4 V		-100	μΑ
lozh†	Off-state output current	V _{CC} = MAX	V _O = 2.4 V	to legith meis-	100	μΑ
los**	Output short-circuit current	V _{CC} = 5 V	V _O = 0 V	-30 -70	-130	mA
Icc	Supply current	V _{CC} = MAX	W. Land	120	180	mA

SYMBOL	PARAME	TER	TEST CONDITIONS	MIN	MER TYP	CIAL	UNIT
t _{PD}	16L8B, 16R4B, 16R6B input or fee	dback to output	a analysis and a	i tui .u	12	15	ns
^t CLK	Clock to output or feedback excep	ot 16L8B	Pal 13	, tho	8	12	ns
t _{PZX}	Pin 11 to output enable except 16	L8B	Commercial	in timbe	10	15	ns
t _{PXZ}	Pin 11 to output disable except 16	L8B	$R_1 = 200 \Omega$		10	15	ns
t _{PZX}	Input to output enable	16R6B, 16R4B, and 16L8B	$R_2 = 360 \Omega$	SAL AM	12	22	ns
tPXZ	Input to output disable	16R6B, 16R4B, and 16L8B	MACERILL HE		12	20	ns
frank	16R8B, 16R6B, 16R4B	Feedback		37	45	130	MHz
[†] MAX	Maximum frequency	No feedback	beatters a con-	50	55		IVITIZ

SYMBOL	PARAMETER		MIN	COMMERCIAL TYP	MAX	UNIT
VCC	Supply voltage	4.7	4.75	5	5.25	V
	Width of clock	Low	15	10		
t _w Width o	Width of clock	High	15	10		ns
t _{su}	Setup time from input or feedback to clock	16R8B-2 16R6B-2 16R4B-2	25	15	guiea stront	ns
th	Hold time	8	0	-10	in blois	ns
TA	Operating free-air temperatur	re	O multiples	25	75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	GMGO TEST (CONDITION	COMMERCI MIN TYP I		UNIT
V _{IL} *	Low-level input voltage		49silov	Light level-wo.	0.8	V
V _{IH} *	High-level input voltage		eyadov	2		V
VIC	Input clamp voltage	V _{CC} = MIN	I _I = -18 mA	-0.8	-1.5	V
I _I L [†]	Low-level input current	V _{CC} = MAX	V _I = 0.4 V	-0.02 -	0.25	mA
I _I H [†]	High-level input current	V _{CC} = MAX	V _I = 2.4 V	ug hvsl-dolf	25	μΑ
Ham	Maximum input current	V _{CC} = MAX	00 V _I = 5.5 V	udri meritesk	1	mA
VOL	Low-level output voltage	V _{CC} = MIN	I _{OL} = 24 mA	0.3	0.5	V
VOH	High-level output voltage	V _{CC} = MIN	I _{OH} = -3.2 mA	2.4 2.8		V
lozL†	Off state output ourrent	V - MAY XAME	V _O = 0.4 V	ugree stars-NC	-100	μΑ
lozh†	Off-state output current	V _{CC} = MAX	V _O = 2.4 V	-	100	μΑ
los**	Output short-circuit current	V _{CC} = 5 V	V _O = 0 V	-30 -100	-250	mA
Icc	Supply current	V _{CC} = MAX	00/	60	90	mA

SYMBOL	PARAMETER PARAMETER	TEST CONDITIONS	COMMER MIN TYP	UNIT	
t _{PD}	Input or feedback to output 16L8B-2, 16R4B-2, and 16R6B-2	à BBJBT kygtup of X16	17	25	ns
tCLK	Clock to output or feedback except 16L8B-2	grosse Hopel and no h	10	15	ns
t _{PZX}	Pin 11 to output enable except 16L8B-2	Commercial	10	20	ns
t _{PXZ}	Pin 11 to output disable except 16L8B-2	$R_1 = 200 \Omega$	ntue of 111	20	ns
tPZX	Input to output enable 16R6B-2, 16R4B-2, and 16L8B-2	$R_2 = 390 \Omega$	10	25	ns
tPXZ	Input to output disable 16R6B-2, 16R4B-2, and 16L8B-2	107,4-88R01 eldsalb t	13	25	ns
fMAX	Maximum frequency 16R8B-2, 16R6B-2, and 16R4B-2	uency 16788-4, 16791	28.5 40		MHz

Quarter-Power Series B-4 16L8B-4, 16R8B-4, 16R6B-4, 16R4B-4

Operating Conditions

SYMBOL	AM SYT PAR	AMETER	пея	MIN	COMMERCIAL TYP MAX	UNIT
V _{CC}	Supply voltage	4.7		4.75	5 slov Maqué 5.25	oV.√
	Width of clock	Low	3840	25	10	
t _w W	Width of clock	High	rigi	25	10	ns
t _{su}	Setup time from input or feedback to clock	16R8B-4 16R6B-4 16R4B-4	8月3日-2 月6日-2 月4日-2	35	25 seal to tool	ns
th	Hold time	0		0	-10 and bloH	ns
TA	Operating free-air temperatur	re		0 101511	25 m grumog 0 75	°C

Electrical Characteristics Over Operating Conditions of pulsaring conditions o

SYMBOL	MORE MAN PARAMETER MORE	TEST CO	NDITION	AUTBALA	COMMERCIAL MIN TYP MAX	UNIT
V _{IL} *	Low-level input voltage			.pal. w	nuqui(Jave)-woul 0.8	V
V _{IH} *	High-level input voltage			aj estat k	2nt level-dglid	V
V _{IC}	Input clamp voltage	V _{CC} = MIN	I _I = -18 m	A	-0.8 -1.5	V
hit as	Low-level input current	V _{CC} = MAX	V _I = 0.4 V	678.00	-0.02 -0.25	mA
liHt as	High-level input current	V _{CC} = MAX	V _I = 2.4 V		ngal level-della 25	μΑ
I _{IASH} 1	Maximum input current	V _{CC} = MAX	V _I = 5.5 V	0.37107	ugni mombasii 1	mA
VOL	Low-level output voltage	V _{CC} = MIN	I _{OL} = 8 mA	- gadho , Ji	0.3 0.5	V
VOH	High-level output voltage	V _{CC} = MIN	I _{OH} = -1 mA	es roy ti	2.4 2.8	V
lozL†	Off-state output current	V - MAY	V _O = 0.4 V		-100	μΑ
lozh†	Off-state output current	V _{CC} = MAX	V _O = 2.4 V	5 (19)(1.)	Lighted etels 100	μΑ
los**	Output short-circuit current	V _{CC} = 5 V	V _O = 0 V	us a contract	-30 -100 -250	mA
1 _{CC}	Supply current	V _{CC} = MAX	v.		30 55	mA

Switching Characteristics Over Operating Conditions and the second of th

SYMBOL	PARAMETER REPORTED FOR THE PARAMETER PARAMETER REPORTED FOR THE PARAMETER PARA	TEST CONDITIONS	COMMEI MIN TYP		UNIT
t _{PD}	Input or feedback to output 16L8B-4, 16R4B-4, and 16R6B-4	Selat léque obba	25	35	ns
t _{CLK}	Clock to output or feedback except 16L8B-4	n or) edisadk ancopy	0 UC of 115	25	ns
t _{PZX}	Pin 11 to output enable except 16L8B-4	Jät Igeaxe sin ne L	terag of 715	25	ns
t _{PXZ}	Pin 11 to output disable except 16L8B-4	$R_1 = 800 \Omega$ $R_2 = 1.56K \Omega$	0 uo of 115	25	ns
tPZX	Input to output enable 16R6B-4, 16R4B-4, and 16L8B-4	81 .S-868-2, 18	10 tuo of 25	35	ns
t _{PXZ}	Input to output disable 16R6B-4, 16R4B-4, and 16L8B-4	of select 19968-2, to	10/40 of 25	35	ns
fMAX	Maximum frequency 16R8B-4, 16R6B-4, and 16R4B-4	Jend, 15888-2, 168	16 25	M	MHz

SYMBOL	COMMERCIAL MAN	PARAMETER	MIN	COMMERCIAL TYP MAX	UNIT		
Vcc	Supply voltage	au.a		4.75	5 5.25	V	
t _W	Addabb of alast.	Low		20	14 pols to regill	ns	
r _W	Width of clock	High	High		Prepad sales 6 ages		
an.	Setup time from input	16RP8A	Polarity fuse intact	25	to tug 15 of emit gute8	l led	
tsu	or foodbook to clock	Polarity fuse blown	30	20 11- 080-014	ns		
th	Hold time	ar I	Polanty fuse intact	0	-10	ns	
TA	Operating free-air temper	ature	Palanty fues blown	0	75	°C	
TC	Operating case temperatu	ire 38			Prevoice Load time	°C	

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST	CONDITIO	NC	MIN	TYP	MAX	UNIT
VIL*	Low-level input voltage	PERSONAL TOOLS			100 0.00 0.00		0.8	V
VIH*	High-level input voltage				2			V
VIC	Input clamp voltage	V _{CC} = MIN		= -18 mA	V HATER I	-0.8	-1.5	V
IIL†	Low-level input current	VCC = MAX	VI	= 0.4 V	r juligen e	-0.02	-0.25	mA
Iнt	High-level input current	V _{CC} = MAX	VI	= 2.4 V	CHANGE.	erd spill	25	μΑ
1	Maximum input current	V _{CC} = MAX	VI	= 5.5 V	D I PORT	SULPHIA STATE	1	mA
VOL	Low-level output voltage	V _{CC} = MIN	loL	= 24 mA	a stangen en	0.3	0.5	V
VOH	High-level output voltage	V _{CC} = MIN	ЮН	= -3.2 mA	2.4	2.8	THE STATE OF	V
lozu†	0#-1-1	Na - AMAY	Vo	= 0.4 V	XII AIRES	TUBE TVE	-100	μΑ
lozh†	Off-state output current	V _{CC} = MAX	Vo	= 2.4 V	1307	(Blanch of	100	μΑ
los**	Output short-circuit current	V _{CC} = 5 V	Vo	= 0 V	-30	-70	-130	mA
ICC	Supply current	V _{CC} = MAX	0-334	2/19/10/2 80	018 07 210 11	120	180	mA

SYMBOL	PARAMET	PARAMETER YEST		MIN	COMMERCIAL	MAX	UNIT
tPD	Input or feedback to output	Polarity fuse intact	postni saut v	Polsin	15	25	ns
4FD	16P8A, 16RP6A, 16RP4A	Polarity fuse blown	nwold sauf y	thaloff.	20 11111100	30	113
tCLK	Clock to output or feedback	01			landbeat to 10 top of MacIC	15	ns
tpzx	Pin 11 to output enable except 16P8A Pin 11 to output disable except 16P8A				taarauchon10 yas 1 toqo	20	ns
tpxz			$R_1 = 200 \Omega$ $R_2 = 390 K\Omega$	1	seen augnon 11 myas of lucin	20	ns
tPZX	Input to output enable	16RP6A, 16RP4A, and 16P8A	112 000 1112		alds at 10 HO CITTOR		ns
tpxz	Input to output disable	16RP6A, 16RP4A, and 16P8A			sidere 13 più o di fico	25	ns
an 0	Maximum frequency	Polarity fuse intact		28.5	40		ZX41
fMAX	16RP8A, 16RP6A, 16RP4A Polarity fuse blown			25	33		MHz

SYMBOL	LALDREVE GO PAR	AMETER	MIN	COMMERCIAL TYP MAX	UNIT
VCC	Supply voltage	475	4.75	5 4 9 4 9 5.25	V
t _W	Width of clock	NS .	20	13	ns
twp	Preload pulse width	01-10-10-10-10-10-10-10-10-10-10-10-10-1	35	15	ns
t _{su}	Setup time for input or feedb	ack to clock	20	Selup time is 10 tops	ns
tsup	Preload setup time	Polenty fine blown 30	25	roolog if Augustal to	ns
200	0	Polarity fuse intact	10	-2 eggl back	
th	Hold time	Polarity fuse blown	0	Operating fit 6- in his mea	ns
thp	Preload hold time		25	nancime 5 so princingO	ns
TA	Operating free-air temperatu	re	0	75	°C
TC	Operating case temperature				°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TI	EST CONDITION	MIN TYP MAX	UNIT
VIL	Low-level input voltage		Marie and Company	3.0	V
VIH	High-level input voltage	34	VANCE COLUMN	2	V
VIC	Input clamp voltage	V _{CC} = MIN	I _I = -18 mA	-0.8 -1.5	V
I _L	Low-level input current	V _{CC} = MAX	V _I = 0.4 V	-0.02 -0.25	mA
ΉΗ	High-level input current	V _{CC} = MAX	V ₁ = 2.4 V	25	μΑ
1	Maximum input current	V _{CC} = MAX	V _I = 5.5 V		mA
VOL	Low-level output voltage	V _{CC} = MIN	I _{OL} = 8 mA	0.3 0.5	V
Vон	High-level output voltage	V _{CC} = MIN	I _{OH} = -3.2 mA	2.4 2.8	V
loz	Off-state output current	V _{CC} = MAX	V _O = 2.4 V/V _O = 0.4 V	-100 100	μΑ
los	Output short-circuit current	V _{CC} = 5 V	V _O = 0 V	-30 -70 -130	mA
Icc	Supply current	V _{CC} = MAX		135 170	mA

SYMBOL	PARAM	PARAMETER		MIN	COMMERCIAL TYP	MAX	UNIT
1 61	Input or feedback	Polarity fuse intact	Taler seen	UNBION	20	30	ns
tPD	to output	Polarity fuse blown	especial each y	Polari	At 401 25 9691 A89	35	ns
tCLK	Clock to output or feed	back		10	Anad ret 17 ligtur of the	30	ns
ts	Input to asynchronous	The second secon		A6981	DEDIKE EIGHT 22 ICH ID CT FT	35	ns
t _R	Input to asynchronous			1698	sonxe exter 27 rolling of 17	40	ns
tPZX	Pin 11 to output enable		R ₂ = 1.1 KΩ	89801	10	20	ns
tpxz	Pin 11 to output disable		A89	gr cine	10	20	ns
tPZX	Input to output enable		A SHIPMA.	onno.	18	30	ns
tPXZ	Input to output disable	2.50	russ intact	rinalah	15	30	ns
fMAX	Maximum frequency	alo:	rounid accid	20	35 44 4 444	BI .	MHz

Operating Conditions

SYMBOL	PARAMETER		MILITARY MIN TYP MAX		COMMERCIAL MIN TYP MAX			UNIT
Vcc	Supply voltage	4.5	5	5.5	4.75	5	5.25	٧
TA	Operating free-air temperature	-55		118-95	0	STATE OF	75	°C
TC	Operating case temperature	7		125				°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	MOTTORIOD TE	TEST CONDITIONS	ASTOM.	MIN	TYP	MAX	UNIT
V _{IL} *	Low-level input voltage		45 7-10-4	ecatiov too	M fav	- inir	0.8	V
VIH*	High-level input voltage	rri Gil' = r. pl	MIN - noV	egalics	2	fager	1	V
VIC	Input clamp voltage	V _{CC} = MIN	I _I = -18mA	linearup tur	gal lev	-0.8	-1.5	V
IIL	Low-level input current	V _{CC} = MAX	V _I = 0.4V	HISTORY BUS	ti lev	-0.02	-0.25	mA
1н	High-level input current	V _{CC} = MAX	V ₁ = 2.4V	Inexaup fut	al mu	sheet s	25	μΑ
l _l	Maximum input current	V _{CC} = MAX	V ₁ = 5.5V	mul voltage	Sic fa .	, rako l	1	mA
VOL	Low-level output voltage	V _{CC} = MIN	MIL	I _{OL} = 8mA	lo ler pede l	0.3	0.5	V
Am 0	9 01	ACC SMILA	СОМ	I _{OL} = 8mA	er ist	Qu-7		357
		V - AMN	MIL	I _{OH} = -2mA	0.4	0.0		
VOH	High-level output voltage	V _{CC} = MIN	СОМ	I _{OH} = -3.2mA	2.4	2.8		V
los	Output short-circuit current **	V _{CC} = 5V	a consta green o	VO = OV	-30	-70	-130	mA
lcc	Supply current	V _{CC} = MAX		9707M8ARAN		60	100	mA

SYMBOL	PARAMETER	TEST	N	IILITAF	RY	COI	MMER	CIAL	UNIT
	PARAMETER	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
t _{PD}	Input or feedback to output	R1 = 560Ω R2 = $1.1k\Omega$		25	45		25	40	ns

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TI CONTRACTOR OF THE PARTY OF T	EST CONDITION		MIN	TYP	MAX	UNIT
V _{IL} *	Low-level input voltage				20 100		0.8	V
V _{IH} *	High-level input voltage			aca o	2	ave -W	ral I	V
VIC	Input clamp voltage	V _{CC} = MIN	I _I = -18 mA	gasth	tage if t	-0.8	-1.5	V
JIL! OF	Low-level input current	V _{CC} = MAX	V _I = 0.4 V	FG)	Hargr	-0.02	-0.25	mA
HH S	High-level input current	V _{CC} = MAX	V _I = 2.4 V	1891 (npan .	SAU A	25	μΑ
h (8)	Maximum input current	V _{CC} = MAX	XA V _I = 5.5 V	Barri	indef.	aupiris	1	mA
VOL	Low-level output voltage	V _{CC} = MIN	I _{OL} = 8 mA	39	the the	0.3	0.5	V
VOH	High-level output voltage	V _{CC} = MIN	I _{OH} = -3.2 mA		2.4	2.8		V
los **	Output short-circuit current	V _{CC} = 5 V	V _O = 0 V	181 0 10	-30	-70	-130	mA
lcc	Supply current	V _{CC} = MAX				60	90	mA

SYMBOL	PARAMETER	TEST	COMMERCIAL TYP	MAX	UNIT
t _{PD}	Input to output propagation delay	R1 = 560 Ω R2 = 1.1 KΩ	15	25	ns

Fast Series 24A 20L8A, 20R8A, 20R6A, 20R4A

Operating Conditions

SYMBOL	PARAMETER 8			ILITAR		COI		UNIT	
				TYP	MAX	MIN	TYP	MAX	
VCC	Supply voltage	4.5	5	5.5	4.75	5	5.25	V	
t _w	Width of clock	Low	20	7		15	7		
	High	20	7		15	7		ns	
^t su	Set up time from input or feedback to clock	20R8A 20R6A 20R4A	30	15	THE STREET	25	15		ns
th	Hold time		0	-10		0	-10		ns
TA	Operating free-air temperature		-55			0		75	°C
TC	Operating case temperature		970		125	St. C. S.	113/12		°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	T	EST CONDITIONS		MIN	TYP	MAX	UNIT
V _{IL} *	Low-level input voltage	- 60	operation problem	eno solipine	la and	uto I	0.8	V
VIH*	High-level input voltage	MOT POMOS TES		Marten	2	STERPELLE	10	V
VIC	Input clamp voltage	V _{CC} = MIN	I _I = -18mA		eren au	-0.8	-1.5	V
TIL	Low-level input current †	V _{CC} = MAX	V _I = 0.4V	Amalica in	net los	-0.02	-0.25	mA
IIH	High-level input current †	V _{CC} = MAX	V ₁ = 2.4V	angle.	v ancri	n ti-oni-	25	μΑ
1	Maximum input current	V _{CC} = MAX	V ₁ = 5.5V	20/00/20 2	egeni II.	al-ear.h	1	mA
VOL	Low-level output voltage	V _{CC} = MIN	Mil	I _{OL} = 12mA	qrii le-	0.3	0.5	V
Am	16 E.O A/S	32 = 101	Com	I _{OL} = 24mA	qni a umikeh nuci k resum	es-sus J		1016
V	8.8 4,2 Am s	S-E-HOI	⊬ Mil oo∀	IOH = -2mA	2011	i-right		Ho ⁷
VOH	High-level output voltage	V _{CC} = MIN	Com	I _{OH} = -3.2mA	2.4	2.8	1750	V
IOZL	18 - 07- 08-	U = ON		V _O = 0.4V	-rioric		-100	μΑ
lozh	Off-state output current †	V _{CC} = MAX	XAW JAY	V _O = 2.4V	000 Tal.5.	yqque	100	μΑ
los	Output short-circuit current **	V _{CC} = 5V		VO = OV	-30	-90	-130	mA
¹ CC	Supply current	V _{CC} = MAX				160	210	mA

SYMBOL	PARAMETER		TEST	MILITARY			COI	UNIT		
			CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	Oldi
t _{PD}	Input or feed- back to output	20R6A 20R4A 20L8A	S-Ad 103 1		15	30	05 S	15	25	ns
tCLK	Clock to output of	or feedback		dons	10	20	STLIC O	10	15	ns
tPZX	Pin 13 to output e	nable except 20L8A		orke etc	10	25	alue pi	10	20	ns
tpxz	Pin 13 to output d	isable except 20L8A	$R_1 = 200\Omega$		11	25	30%	11	20	ns
t _{PZX}	Input to output enable	20R6A 20R4A 20L8A	$R_2 = 390\Omega$	8	10	30	191.00 08 G-A	10	25	ns
t _{PXZ}	Input to output disable	20R6A 20R4A 20L8A			13	30	19400 C	13	25	ns
fMAX	Maximum frequency	20R8A 20R6A 20R4A		20	40	yaneur Rask-21	28.5	40		MHz

SYMBOL	OFFICE OF THE THE PARA	METER	MIN	COMMERCIAL TYP MAX	UNIT
Vcc	Supply voltage	No.	4.75	5.0910v (1995.25	OVV
	7 38 7	Low	25	10 Santa Louring	
t _W	t _w Width of clock	High	25	10	ns
t _{su}	Setup time from input or feedback to clock	20R8A-2, 20R6A-2, 20R4A-2	35	or 25 less to man	ns
th	Hold time	0	0	-15	ns
TA	Operating free-air temperature		0	25 75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	Т	EST CONDITION	MIN	TYP	MAX	UNIT
V _I L*	Low-level input voltage	Amara = II	1/4 100V	A SEC. LA	TE/CI II	0.8	V
VIH*	High-level input voltage	AVO - IA	XBN 100A Illens	2	ISVD-	WG I	V
VIC	Input clamp voltage	VCC = MIN	I _I = -18 mA	Norn	-0.8	-1.5	V
TIL†	Low-level input current	V _{CC} = MAX	V _I = 0.4 V	THERM	-0.02	-0.25	mA
Ін†	High-level input current	V _{CC} = MAX	V _I = 2.4 V		Inches !	25	μΑ
lj S	Maximum input current	V _{CC} = MAX	V _I = 5.5 V		10.10	1	mA
VOL	Low-level output voltage	V _{CC} = MIN	I _{OL} = 24 mA		0.3	0.5	V
Vон	High-level output voltage	V _{CC} = MIN	I _{OH} = -3.2 mA	2.4	2.8		V
lozL†	Off state outside surrent	V MAY	V _O = 0.4 V	righter	SVALA	-100	μΑ
lozh†	Off-state output current	V _{CC} = MAX	V _O = 2.4 V			100	μΑ
los**	Output short-circuit current	V _{CC} = 5 V	V _O = 0 V	-30	-70	-130	mA
Icc	Supply current	V _{CC} = MAX	XAM - OOV I sens	- lugher	80	105	mA

SYMBOL	PARAMETER YAS	TEST	MILITARY MIN TYP MAX	COMMERCIAL MIN TYP MAX	UNIT
t _{PD}	Input or feedback to output 20L8A-2 20R6A-2 20R4A-2	ASJI	25 50	hest 25 and 35	ns
t _{CLK}	Clock to output or feedback except 20L8A-2		15 25	15 25	ns
t _{PXZ/ZX}	Pin 13 to output disable/enable except 20L8A-2	0	3.08 10 15 25	15 25	ns
t _{PZX}	Input to output enable 20L8A-2 20R6A-2 20R4A-2	Commercial $R_1 = 200 \Omega$ $R_2 = 390 \Omega$	25 45	25 35	ns
t _{PXZ}	Input to output disable 20L8A-2 20R6A-2 20R4A-2	ASJE	25 45	25 35	ns
f _{MAX}	Maximum frequency 20R8A-2 20R6A-2 20R4A-2	AARO	14 19	16 19	MHz

SYMBOL		PARAMETER		MIN	COMMERCIAL TYP MAX	UNIT
Vcc	Supply voltage	l a	14	4.75	5 5.25	V
an I	NACIDAL OF STREET	Low	DP 1	10	6 pelo lo rebilit	_w j
w	t _w Width of clock High 2088B 2086	20R8B, 20R6B, 20R4B	12	8 lengt ou fe?	ns	
t _{su}	Setup time from ir or feedback to clo		08 20110B, 20110B, 20114B	15	input of 10 ⁸ of 10 sugai	ns
t _h	Hold time		38-	0 shufani	somet station withrego	ns
TA	Operating free-air	temperature		0 940	75	°C

SYMBOL	PARAMETER	TEST	CONDITION	COMMER MIN TYP	CIAL	UNIT
V _{IL} *	Low-level input voltage		vortage	ndur skal-uit	0.8	V
V _{IH} *	High-level input voltage	Aridi - A II	10 00 str	2	144	V
VIC	Input clamp voltage	V _{CC} = MIN	I _I = -18 mA	-0.8	-1.5	٧
I _{IL} †	Low-level input current	V _{CC} = MAX	V _I = 0.4 V	-0.02	-0.25	mA
I _{IH} †	High-level input current	V _{CC} = MAX	V ₁ = 2.4 V		25	μΑ
1 30	Maximum input current	V _{CC} = MAX	V ₁ = 5.5 V equation (ligtuo lavai-iu	od 1	mA
VOL	Low-level output voltage	V _{CC} = MIN	I _{OL} = 24 mA	0.3	0.5	V
Vон	High-level output voltage	V _{CC} = MIN	I _{OH} = -3.2 mA	2.4 2.8		V
lozL†	Off state output output	V - MAY	V _O = 0.4 V	igluo ist-rig	-100	μΑ
lozh†	Off-state output current	V _{CC} = MAX	V _O = 2.4 V		100	μΑ
los**	Output short-circuit current	V _{CC} = 5 V	V _O = 0 V	-30 -70	-130	mA
lcc	Supply current	V _{CC} = MAX	ourcant You is like.	140	210	mA

SYMBOL	PARAMETER	01.108	TEST	MIN	DMMERCIAL TYP	MAX	UNIT
t _{PD}	Input or feedback to output 20L8B, 20R6B, 20R4B	875	parating Condition	neo esite	12	15	ns
tCLK	Clock to output or feedback e	except 20L8B	100	METER	8	12	ns
tPZX	Pin 13 to output enable excep	ot 20L8B	Commercial R ₁ = 200 Ω	hietuo	10	15	ns
tPXZ	Pin 13 to output disable excep	ot 20L8B			018 S AXOS 8	12	ns
t _{PZX}	Input to output enable 20R6B, 20R4B, 20L8B	= 200 ft	R ₂ = 390 Ω	свораскі вісері віністврів вхорі	12	18	ns
t _{PXZ}	Input to output disable 20R6B, 20R4B, 20L8B	E 380 ci	A THE	a axoept 201010	12 000 01	15	ns
, 81 B	Maximum frequency	Feedback		37	40	otest.	MHz
^f MAX	20R8B, 20R6B, 20R4B	No feedback		45	50		IVIMZ

SYMBOL	LAIORETHOD PAR	LAGORGOMOGI PARAMETER			RY MAX	COI	MERC TYP	MAX	UNIT
Vcc	Supply voltage	Supply voltage		5	5.5	4.75	5	5.25	V
	Width of clock	Low	40	20	T	35	20		7478200
t _w	width of clock	High	30	10		25	10	į.	ns
t _{su}	Set up time from input or feedback to clock	20X10, 20X8, 20X4	60	38	den in	50	38	3 1	ns
th	Hold time		0	-15	N. C. IVI	0	-15		ns
TA	Operating free-air temperatur	е	-55			0	tid trigi	75	°C
TC	Operating case temperature	0	6	Wist-	125	Strike Er	theol		°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITI	ONS	MIN T	YP MAX	UNIT
V _{IL} *	Low-level input voltage	POLITICIA DE 182	7	1. 199 M	ad	0.8	V
VIH*	High-level input voltage			Propies 1	2	Anna de la	V
VIC	Input clamp voltage	V _{CC} = MIN	I _I = -18	mA	Or Monday	0.8 -1.5	V
- III	Low-level input current †	V _{CC} = MAX	V ₁ = 0.4\		-0	.02 -0.25	mA
ΉΗ	High-level input current †	V _{CC} = MAX	V ₁ = 2.4\	/		25	μΑ
	Maximum input current	V _{CC} = MAX	V ₁ = 5.5\	/	1000	1	mA
VOL	Low-level output voltage	VCC = MIN	Mil	I _{OL} = 12mA	nout amus	0.3 0.5	V
	3.0 8.0 Am #0	VCC - WIIIV	Com	I _{OL} = 24mA	guo teval	MO.1	TOA
V	12 mA 2.6	- Hol	VOIM MILDY	I _{OH} = -2mA	dua loval-r	foil#(HOV
VOH	High-level output voltage	V _{CC} = MIN	Com V	I _{OH} = -3.2mA		2.8 -tic	I SCV
lozL	M: 0(- 00- V) = QV		V _O = 0.4V	p-morte suc	_100	μΑ
lozн	Off-state output current †	V _{CC} = MAX	Xater CDV	V _O = 2.4V	ins also yes	100	μΑ
los	Output short-circuit current **	V _{CC} = 5V		V _O = 0V	-30 -7	70 –130	mA
Icc	Supply current	V _{CC} = MAX	20X10	20X8 20X4	12	20 180	mA
Icc	Supply current	V _{CC} = MAX	20L10	有面面的 我	9	0 165	mA

CVMDOL	PARAMETER	TEST	M	ILITA	RY	CO	MMER	CIAL	UNIT	
SYMBOL	PARAMETER	CONDITIONS	MIN TY		MAX	MIN	TYP	MAX	ONIT	
t _{PD}	Input or feedback to output 20X8, 20X4, 20LID	B Come	BUIGE For URSE for	35	60	alur es	35	50	ns	
tCLK	Clock to output or feedback except 20L10		1	20	35	opinio t	20	30	ns	
tPXZ/ZX	Pin 13 to output disable/enable except 20L10	$R_1 = 200 \Omega$		20	45	92.8	20	35	ns	
t _{PZX}	Input to output enable except 20X10	R ₂ = 390 Ω		35	55		35	45	ns	
t _{PXZ}	Input to output disable except 20X10			35	55	est ma	35	45	ns	
fMAX	Maximum frequency 20X10, 20X8, 20X4	lo leedback	10.5	16	/ Alexidan Consu	12.5	16		MHz	

SIMBOL	OFESH WOO CHAT PAR	AMETER	ast	MIN	COMMERCIAL TYP MAX	UNIT
VCC	Supply voltage	8.2		4.75	510 Ageue 5.25	V
	16 15 10	Low		25	15	
w Width of clock	High		15	7	ns	
^t su	Setup time from input or feedback to clock	20X10A 20X8A 20X4A	017 88 84	30	fucini meni ami quees vocas 20 juni isali is	ns
th	Hold time	0	. *	0	-15 to 17 bloss	ns
TA	Operating free-air temperatur	·e	E CONTRACTOR	0	25 75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST	CONDITION	MIN TYP	MAX	UNIT
V _{IL} *	Low-level input voltage		entio/	Lanii, st-so	0.8	V
V _{IH} *	High-level input voltage	A-31 - A	IM = gr/V spo	2 90 50 120	rit i	V
V _{IC}	Input clamp voltage	V _{CC} = MIN	I _I = -18 mA	the state of the same of	-1.5	V
l _{IL} † as	Low-level input current	V _{CC} = MAX	V ₁ = 0.4 V	-0.02	-0.25	mA
I _{IH} †	High-level input current	V _{CC} = MAX	V _I = 2.4 V	Light number	25	μА
110 80	Maximum input current	V _{CC} = MAX	V _I = 5.5 V	glue is solwin	1	mA
VOL	Low-level output voltage	V _{CC} = MIN	^I OL = 24 mA	0.3	0.5	V
VOH	High-level output voltage	V _{CC} = MIN	I _{OH} = -3.2 mA	2.4 2.8	gart,	V
lozL†	Off state output ourset	V - MAY	V _O = 0.4 V		-100	μА
lozh†	Off-state output current	V _{CC} = MAX	V _O = 2.4 V	higher of 1	100	μΑ
los**	Output short-circuit current	V _{CC} = 5 V	V _O = 0 V	-30 -70	-130	mA
Am bis	Curati	V - MAY	20X10A,20X8A,20X4A	140	180	A
ICC	Supply current	V _{CC} = MAX	20L10A	115	165	mA

SYMBOL	PAR	TEST	MIN TYP MAX			UNIT	
t _{PD}	Input or feedback to output 2	0L10A, 20X8A, and 20X4A	Adequeur IO	300,00	23	30	ns
tCLK	Clock to output or feedback		OF THE BUILDING STREET		10	15	ns
t _{PZX}	Pin 13 to output enable excep	t 20L10A	Commercial		11	20	ns
t _{PXZ}	Pin 13 to output disable excep	ot 20L10A	$R_1 = 200 \Omega$	siden	10	20	ns
t _{PZX}	Input to output enable	20X8A, 20X4A, and 20L10A	$R_2 = 360 \Omega$		19	30	ns
t _{PXZ}	Input to output disable	20X8A, 20X4A, and 20L10A	20894	aldes	15	30	ns
fMAX	Maximum frequency	20X10A, 20X8A, and 20X4A	ency 2048/10, 2	22.2	32	4]	MHz

SYMBOL	JANUAR ZUBLÜCK SKY	PARAMETER	1.307	MIN	TYP	RY MAX	COM	MMER TYP	CIAL	UNIT
VCC	Supply voltage	Branch Control of		4.5	5	5.5	4.75	5	5.25	o V
	Width of clock	Low		20	10		15	10		
tw	width of clock	High	; (g)	20	10		15	10		ns
t _{su}	Setup time from input or feedback to clock	20RS10 20RS8 20RS4	ACTION METER ALIKE	40	25	rof (sa	35	25		ns
th	Hold time			0	-10		0	-10		ns
TA	Operating free-air tempe	rature		-55	N	sc 1 113	0	est ald	75	°C
TC	Operating case temperat	ure				125	Ly option			°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	Marine Comment	TEST CONDITI	ON	MIN TYP MAX	UNIT
V _{IL} *	Low-level input voltage	the falls dright and			0.8	V
VIH*	High-level input voltage				2	V
VIC	Input clamp voltage	V _{CC} = MIN	I _I = -18 mA	1 1991	-0.8 -1.5	V
I/L†	Low-level input current	V _{CC} = MAX	V _I = 0.4 V		-0.02 -0.25	mA
I _{IH} †	High-level input current	V _{CC} = MAX	V _I = 2.4 V	(0) 40140	25	μΑ
16 18	Maximum input current	V _{CC} = MAX	V _I = 5.5 V	74 111/1/3	ident (SHAH-High) 1	mA
VOL	Low-level output voltage	V _{CC} = MIN	Mil	I _{OL} = 12 mA	0.3 0.5	V
*OL	Low level output voltage	VCC IVIIIV	Com	I _{OL} = 24 mA	glub sess sp.	e V
1/		N/ 1 N/ 1	Mil	I _{OH} = -2 mA		
VOH	High-level output voltage	V _{CC} = MIN	Com	I _{OH} = -3.2 mA	2.4 2.8	V
loz _L †	Off-state output current	W - MAY	XARL BOX	V _O = 0.4 V	uc no esta e 110 -100	μΑ
lozh†	On-state output current	V _{CC} = MAX		V _O = 2.4 mA	100	μr.
los**	Output short-circuit current	V _{CC} = 5 V	A 9 = 30 x	V _O = 0 V	-30 -70 -130	mA
lcc	Supply current	V _{CC} = MAX	MASA = NOV		175 240	mA

SYMBOL	PARA	METER	TEST CONDITIONS	MIN	TYP	RY MAX	CON	MER TYP	MAX	UNIT
******	Input or feedback	Polarity fuse intact			25	40		25	35	-
^t PD	to output 20S10, 20RS8, 20RS4	Polarity fuse blown	A Rati	BISU RA	30	45		30	40	ns
tCLK	Clock to output or feed	back	Commercial $R_1 = 200 \Omega$	74,72.00 F = 100	12	20		12	17	ns
t _{PZX}	Pin 13 to output enable	except 20S10	R ₂ = 390 KΩ		10	25		10	20	ns
t _{PXZ}	Pin 13 to output disable	e except 20S10		Section Section	11	25		11	20	ns
t _{PZX}	Input to output enable	20S10, 20RS8, 20RS4	AOL	SS Ige	25	35	n wet	25	35	ns
t _{PXZ}	Input to output disable	20S10, 20RS8 20RP4	Military $R_1 = 390 \Omega$		13	30	11 10 6 12 4 0	13	25	ns
fMAX	Maximum frequency	20RS10, 20RS8, 20RS4	$R_2 = 750 \Omega$	18	28	Janes G	20	28		MHz

SYMBOL	PARAMETERS OF THE PARAMETERS O	TER	MIN	TYP	RY MAX	COI	MMER TYP		UNIT
Vcc	Supply voltage		4.5	5	5.5	4.75	5	5.25	JOV
	Width of clock	Low	25	13		20	13		ns
t _w	Width of Glock	High	25	13		20	13		1115
twp	Preload pulse width		45	15	rillolw	35	15		ns
t _{su}	Setup time for input or feedback to	clock facial early white	25	10	transit s	20	10		ns
tsup	Preload setup time	Polanty fuse blown	30	5		25	5		ns
80	30 25	Polarity fuse intact	10	-2	emil s	10	-2		guel
th	Hold time	Polarity fuse blown	0	-6		0	-6		ns
thp	Preload hold time		30	5	emil	25	5		ns
TA	Operating free-air temperature		-55	Enody	af In-	0	Imeq(75	°C
TC	Operating case temperature			udste	125	BO GO	Jereqt.		°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	577	TEST CONDITION	MIN	TYP	MAX	UNIT
V _{IL} *	Low-level input voltage	OFFICE CONTRACT	H5Y31			0.8	V
V _{IH} *	High-level input voltage		epatiov is	2	si-e-o.l		V
VIC	Input clamp voltage	V _{CC} = MIN	I _I = -18 mA	grilles.	-0.8	-1.5	V
IIL 9	Low-level input current	V _{CC} = MAX	V ₁ = 0.4 V	er grast	-0.02	-0.25	mA
I _{IH}	High-level input current	V _{CC} = MAX	V _I = 2.4 V	and to	1-40	25	μΑ
fig. 35	Maximum input current	V _{CC} = MAX	V _I = 5.5 V	elat lavi	High-k	1	mA
VOL	Low-level output voltage	V _{CC} = MIN	I _{OL} = 8 mA	Minimu	0.3	0.5	V
Vон	High-level output voltage	V _{CC} = MIN	I _{OH} : Mil-2 mA Com-3.2 mA	2.4	2.8		V
loz	Off-state output current	V _{CC} = MAX	V _O = 2.4 V/V _O = 0.4 V	-100		100	μΑ
los**	Output short-circuit current	V _{CC} = 5 V	V _O = 0 V	-30	-70	-130	mA
Icc	Supply current	V _{CC} = MAX			155	200	mA

SYMBOL	PARAMETE	R	TEST		TYP	RY MAX		TYP		UNIT
		Polarity fuse intact			20	35		20	30	
^t PD	Input or feedback to output	Polarity fuse blown			25	40		25	35	ns
tCLK	Clock to output or feedback		Mico galeragia n	10	17	35	10	17	30	ns
ts	Input to asynchronous set	ECONDITIONS MI		HBT	22	40		22	35	ns
t _R	Input to asynchronous reset		D - 500 0		27	45		27	40	ns
t _{PZX}	Pin 13 to output enable		$R_1 = 560 \Omega$	naio9	10	25	40 0	10	20	ns
tPXZ	Pin 13 to output disable		$R_2 = 1.1 \text{ K}\Omega$	2080	10	25	10.03	10	20	ns
tPZX	Input to output enable	D (668 = 18			18	35	une i	18	30	ns
t _{PXZ}	Input to output disable				15	35	1211	15	30	ns
fMAX	Maximum frequency			16	35	darbe:	20	35	7	MHz

SYMBOL	MOSSIMMOD YRAT PARAM	ETER Har	MILITARY MIN TYP MAX	COMMERCIAL MIN TYP MAX	UNIT
Vcc	Supply voltage		4.5 5 5.5	4.75 5 5.25	V
	Milde of class.	Low	25	20	
tw	Width of clock	High dorld	25	20	ns
twp	Preload pulse width		45 Albiw	35 paoles I	ns
20 T	25 10	Polarity fuse intact	50 adbest to tugni	40 mis quisa	ns
^t su	Setup time for input to clock	Polarity fuse blown	50 emil	40 beoletq	ns
t _{sup}	Preload setup time	Polarity tuse Intact	30	25	ns
th	Hold time	Polarity fuse blown	0 -10	0 -10	ns
thp	Preload hold time		10 em	5 _{ort beolet} 9	ns
TA	Operating free-air temperature		-55 unstegmed tis-	0 pnimeyO 75	°C
ТС	Operating case temperature		125	Operating car	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITION	MIN TYP MAX	UNIT
V _{IL} *	Low-level input voltage	7 34 1 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4	ep lov	8.0 High-level inpu	V
VIH*	High-level input voltage	Am 81 - = -11	Mild = cray open	ov cement dens	V
V _{IC}	Input clamp voltage	V _{CC} = MIN	XAII = -18 mA	00 15	V
HE I SS	Low-level input current	V _{CC} = MAX	XAIVI= 0.4 V	-0.02 -0.25	mA
ЛН Т	High-level input current	V _{CC} = MAX	XA VI = 2.4 V	unoi mumbusi 25	μΑ
4 20	Maximum input current	V _{CC} = MAX	V _I = 5.5 V	igher level-would 1	mA
V	Com-32,rrA [21 ,28	Algorithm and	Mil IOL = 8 mA	0.3 0.5	HV
VOL	Low-level output voltage	V _{CC} = MIN	Com I _{OL} = 8 mA	Univo etiste-110	sol
AVE DE	Lijeh level evtevt veltees	- NAINI	Mil I _{OH} = -2 mA	2.4 2.8	V
VOH	High-level output voltage	V _{CC} = MIN	Com I _{OH} = -3.2 mA	Supply during 1	23
lozL	0#	V - MAY	V _O = 0.4 V	-100	μΑ
lozh	Off-state output current	V _{CC} = MAX	V _O = 2.4 V	100	μΑ
los**	Output short-circuit current	V _{CC} = MAX	V _O = 0 V	-30 -70 -130	mA
lcc	Supply current	V _{CC} = MAX		200 280	mA

SYMBOL	PAR	AMETER	TEST	MILITARY MIN TYP MAX	MIN TYP MA	
40 02	(A) (A)	Polarity fuse intact		50	hyae or hughi 4	0 ns
^t PD	Input to output	Polarity fuse blown		55	4	
tCLK	Clock to output or f	eedback		30	tho of Et aid 2	5 ns
t _{PZX}	Output enable	BE	$R_1 = 560 \Omega$ $R_2 = 1.1 KΩ$	25	intuo of tugni 2	0 ns
t _{PXZ} 08	Output disable	16		310.56 25	afua at tugal 2	0 ns
fMAX	Maximum frequenc	e at		14 monaug	a 16 numbral/4	MHz

SYMBOL	PARAME	ETER	MIN	COMMERCIAL TYP MAX	UNIT
Vcc	Supply voltage		4.75	disaw 5 uc baoler 5.25	ov.V
t _w	Wide of start.	Low	20	Preload setup time	met.
W	Width of clock	High	20	Preload void time	ns
	Cot and the of the state of the	Polarity fuse intact	40	ribly se o team?	ns
^t su	Setup time from input to clock	Polarity fuse blown	40	Preset recovery limit	TIS
th	Hold time	CALL MANAGEMENT AND ASSESSMENT OF THE PARTY.	0	-10	ns
TA	Operating free-air temperature		0	75	°C
TC	Operating case temperature				°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST	CONDITION	MIN	MMER TYP	CIAL	UNIT
V _{IL} *	Low-level input voltage					0.8	V
V _{IH} *	High-level input voltage			2			V
VIC	Input clamp voltage	V _{CC} = MIN	I _I = -18 mA		-0.8	-1.5	V
IIL	Low-level input current	V _{CC} = MAX	V ₁ = 0.4 V		-0.02	-0.25	mA
I _{IH}	High-level input current	V _{CC} = MAX	V ₁ = 2.4 V			25	μΑ
II	Maximum input current	V _{CC} = MAX	V _I = 5.5 V			1	mA
VOL	Low-level output voltage	V _{CC} = MIN	I _{OL} = 8 mA		0.3	0.5	V
VOH	High-level output voltage	V _{CC} = MIN	I _{OH} = -0.4 mA	2.4	2.8		V
lozL	Off state output ourrant	V - MAY	V _O = 0.4 V			-100	μΑ
lozh	Off-state output current	V _{CC} = MAX	V _O = 2.4 V			100	μΑ
los**	Output short-circuit current	V _{CC} = 5 V	V _O = 0 V	-10	-40	-60	mA
lcc	Supply current	V _{CC} = MAX			400	640	mA

SYMBOL	P	ARAMETER	TEST CONDITIONS	MIN	UNIT		
	Innut to output	Polarity fuse intact				50	-
^t PD	Input to output	Polarity fuse blown				55	ns
^t CLK	Clock to output or feedbac	k				22	ns
t _{PZX}	Output enable		$R_1 = 560 \Omega$ $R_2 = 1.1 K\Omega$			30	ns
t _{PXZ}	Output disable					30	ns
t _{PRH}	Preset to output					35	ns
fMAX	Maximum frequency			16	20		MHz

SYMBOL		PARAMETER		MIN	COMMERCIAL TYP MAX	UNIT
t _{wp}	Preload pulse width	81.8		35	Strick Adding	ns
t _{sup}	Preload setup time	20	wal	50	www.hammona/	ns
thp	Preload hold time	08	Agit-I	5		ns
t _{PRW}	Preset pulse width	649	Pearity Lastintics	25	Se apriliana kumana	ns
t _{PRR}	Preset recovery time	Die]	nwold as a year.	35		ns

Electrical Characteristics over Operating Conditions

Switching Character Lice Over Opening Conditions

Output Register PRELOAD

The PRELOAD function allows the register to be loaded from data placed on the output pins. This feature aids functional testing of sequential designs by allowing direct setting of output states. The procedure for PRELOAD is as follows:

Series 20PA

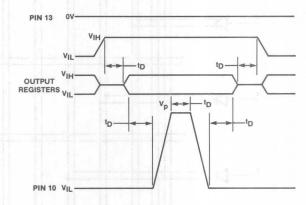
- 1. Raise V_{CC} to 4.5 V.
- 2. Disable output registers by setting pin 11 to VIH.
- 3. Apply VII NIH to all registered output pins.
- 4. Pulse pin 8 to V_D, then back to 0 V.
- 5. Remove VIL /VIH from all output registers.
- 6. Lower pin 11 to V_{IL} to enable the output registers.
- 7. Verify for VOI NOH at all registered output pins.

Series 24RS/24XA

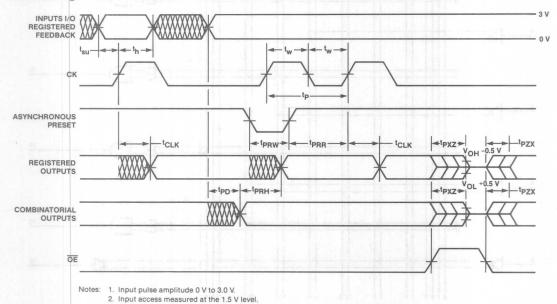
- 1. Raise V_{CC} to 4.5 V.
- 2. Disable output registers by setting pin 13 to $V_{\mbox{\scriptsize IH}}$.
- 3. Apply V_{IL}/V_{IH} to all registered output pins.
- 4. Pulse pin 10 to V_p, then back to 0 V.
- 5. Remove VII /VIH from all output registers.
- 6. Lower pin 13 to V_{IL} to enable the output registers.
- 7. Verify for VOL/VOH at all registered output pins.

Power-Up RESET

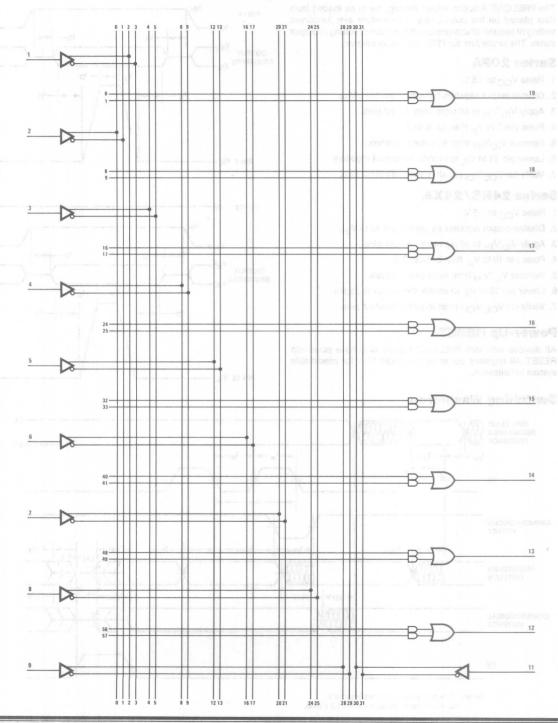
All devices with this PRELOAD feature also have power-up RESET. All registers power up to a logic high for predictable system initialization.



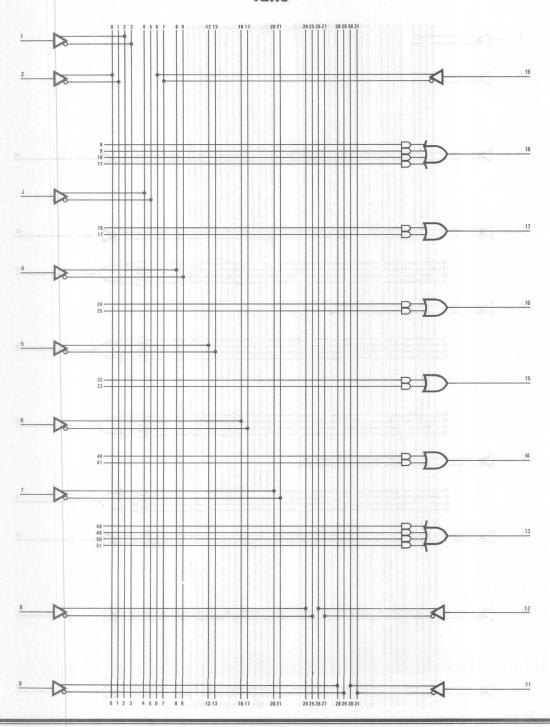
Switching Waveforms



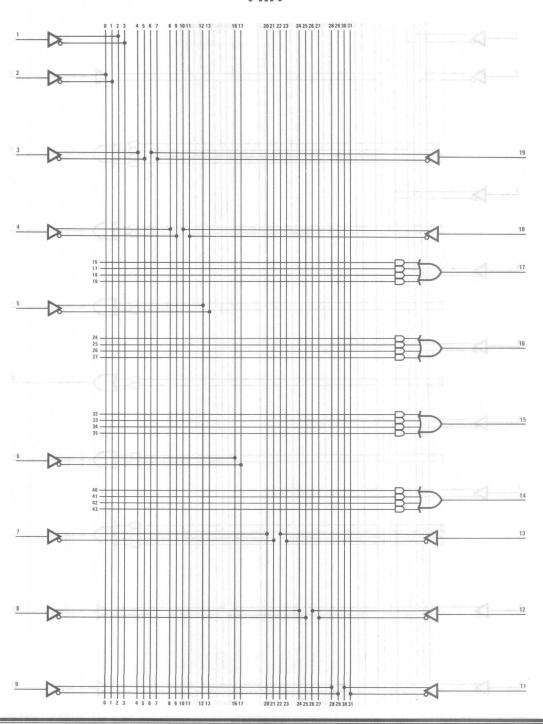




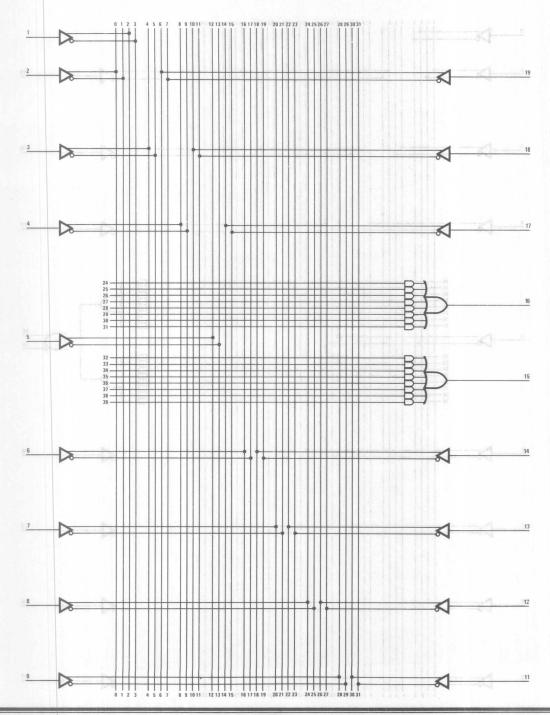
12H6



14H4

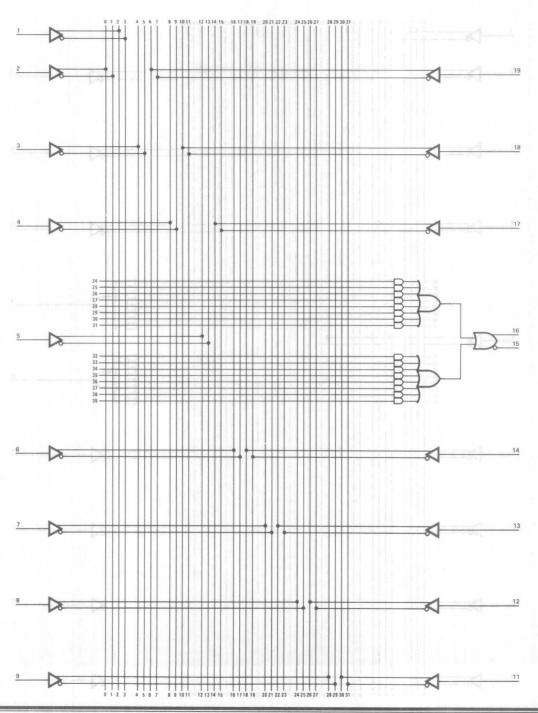


16H2

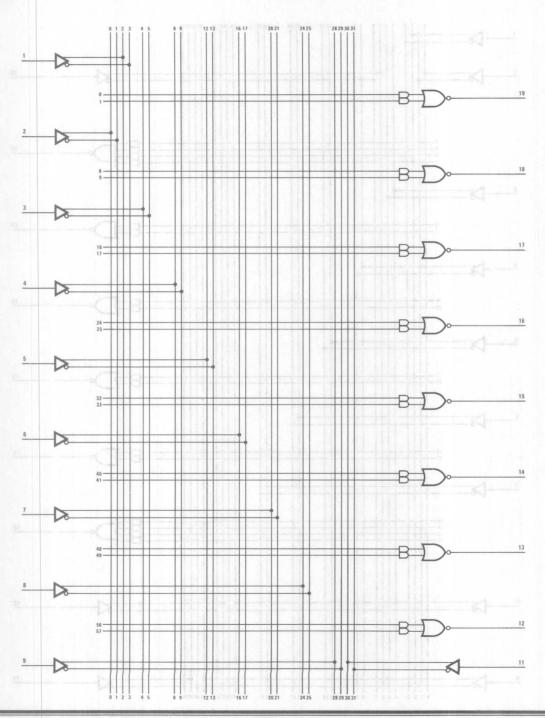


5

16C1

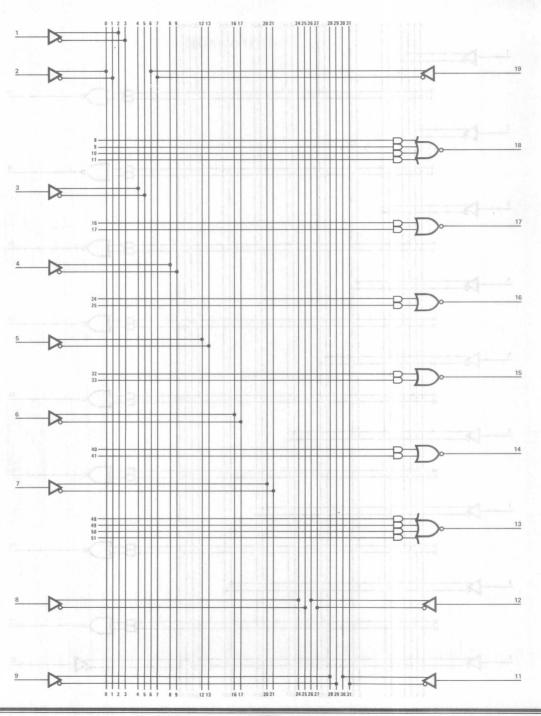


10L8



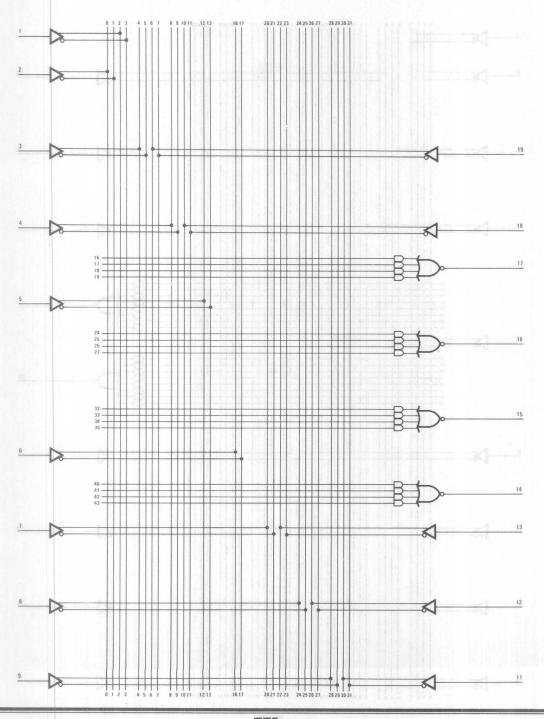
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12L6

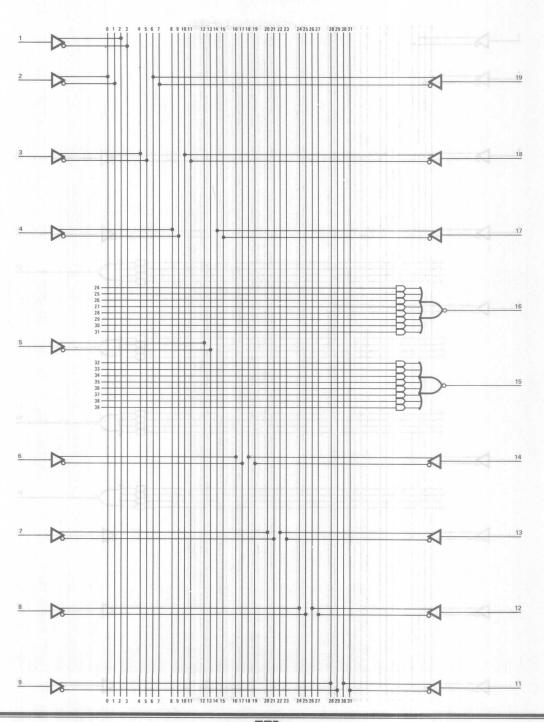


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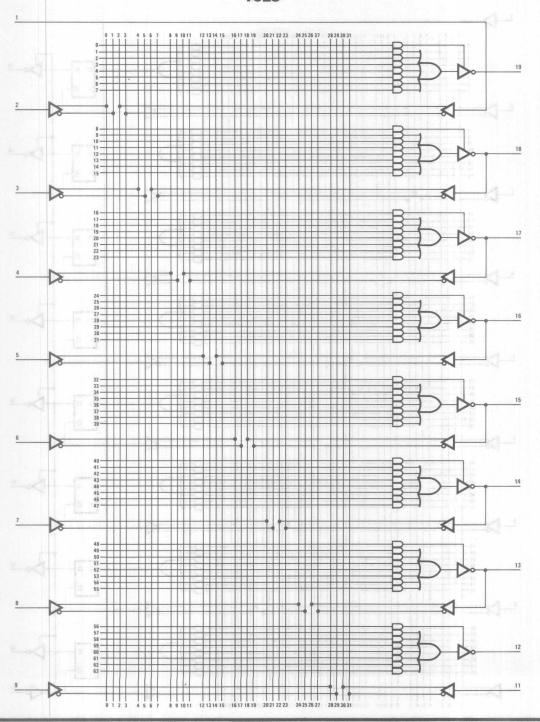
14L4

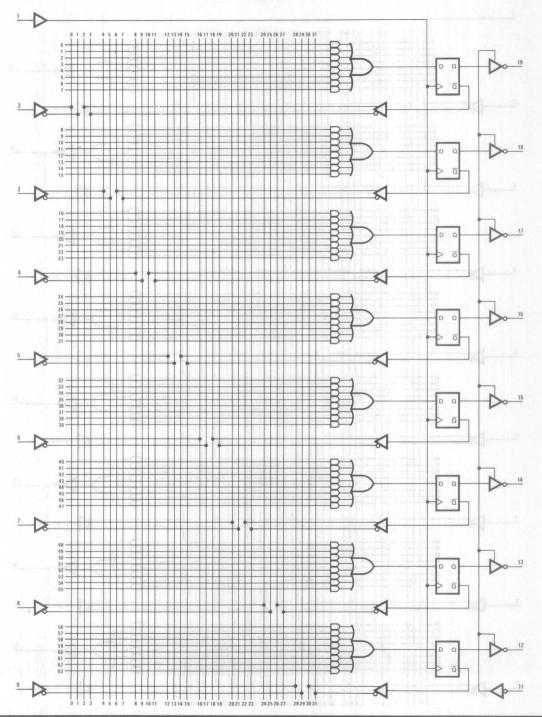


16L2

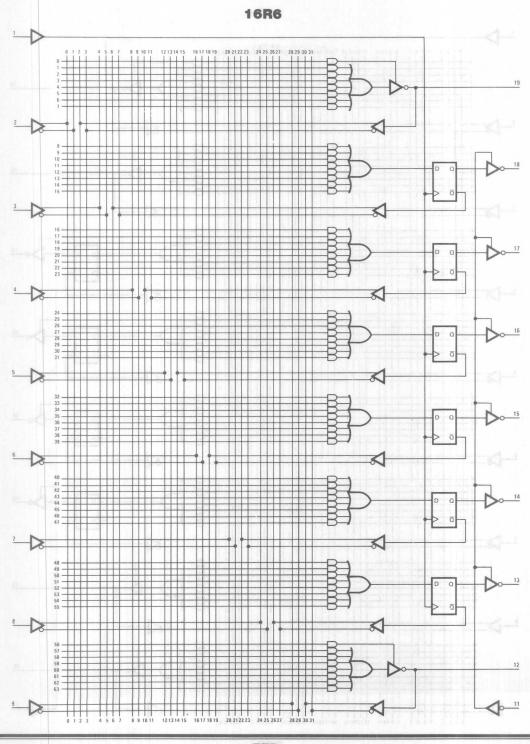


16L8

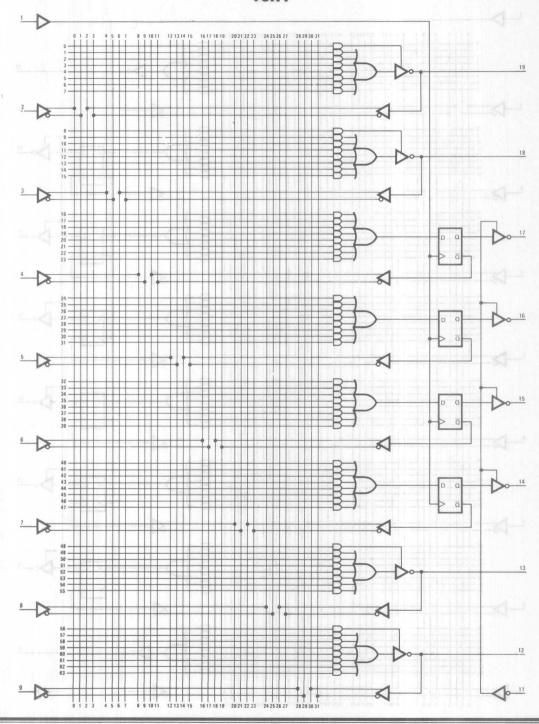




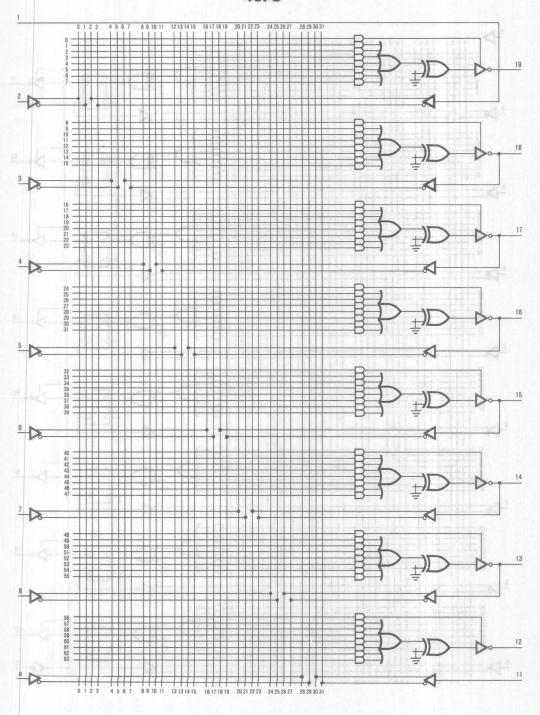




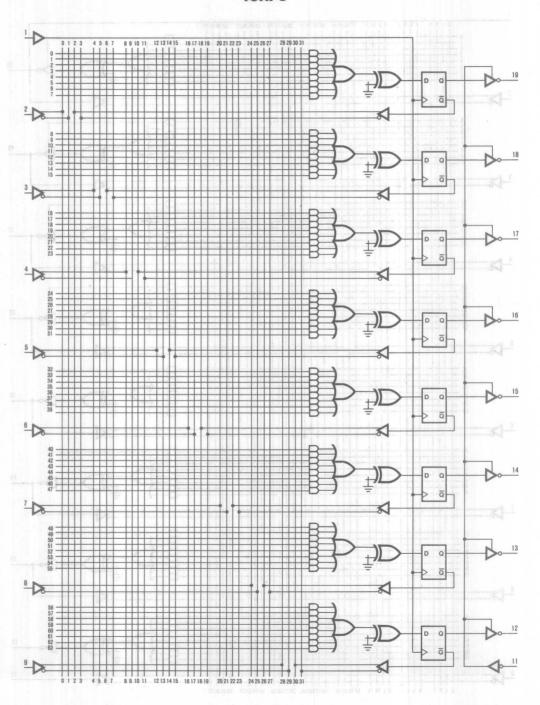
16R4



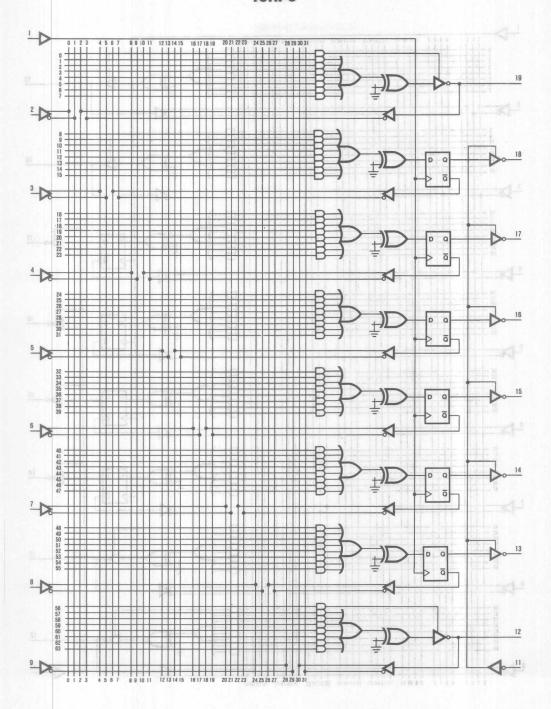
16P8



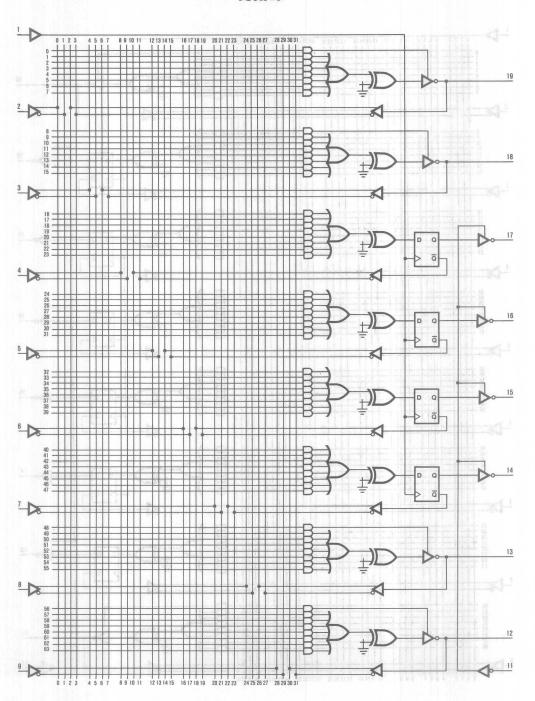
16RP8



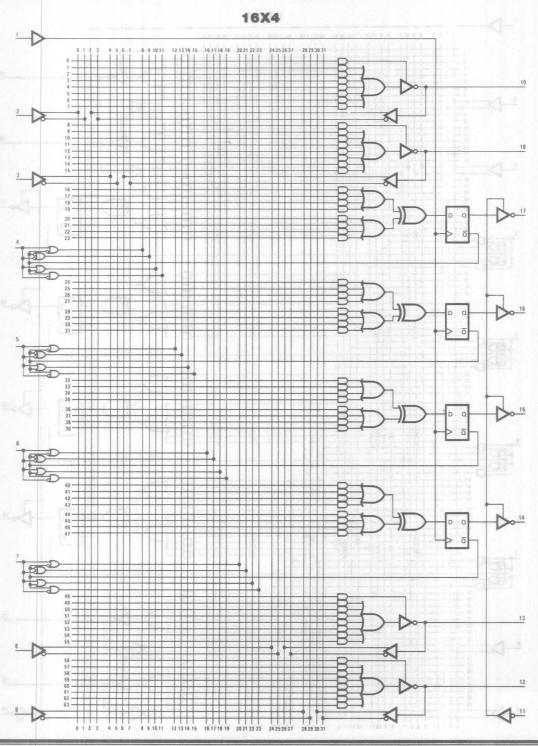
16RP6

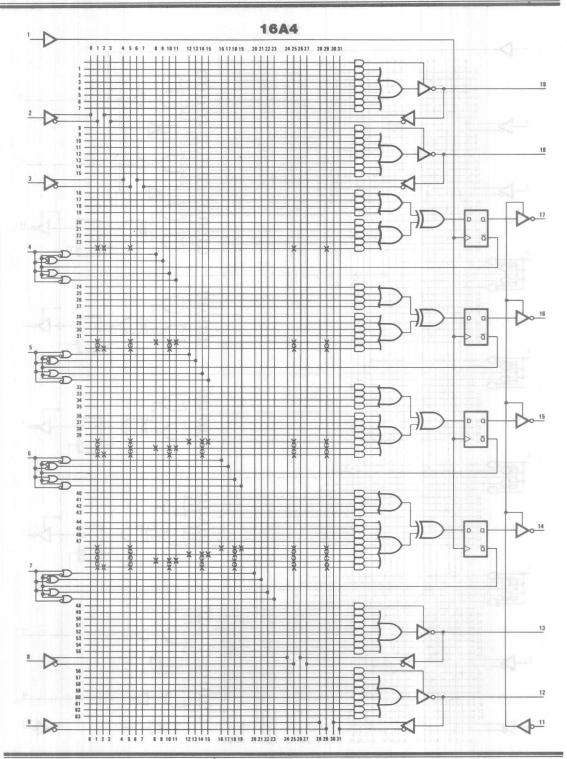


16RP4

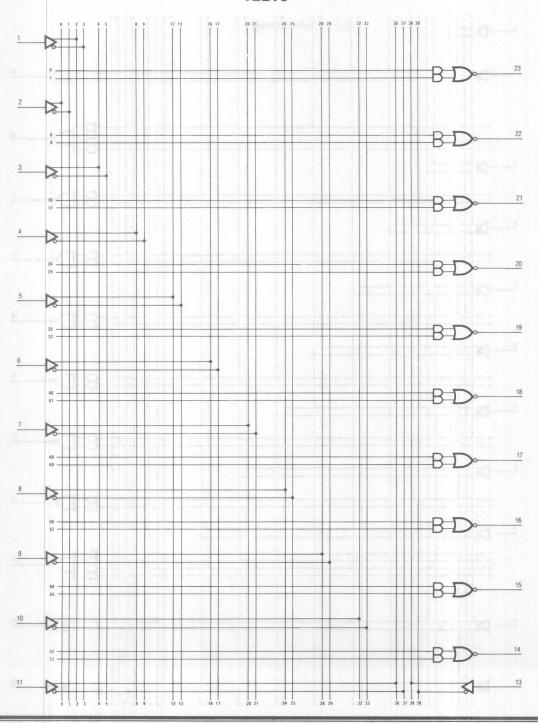


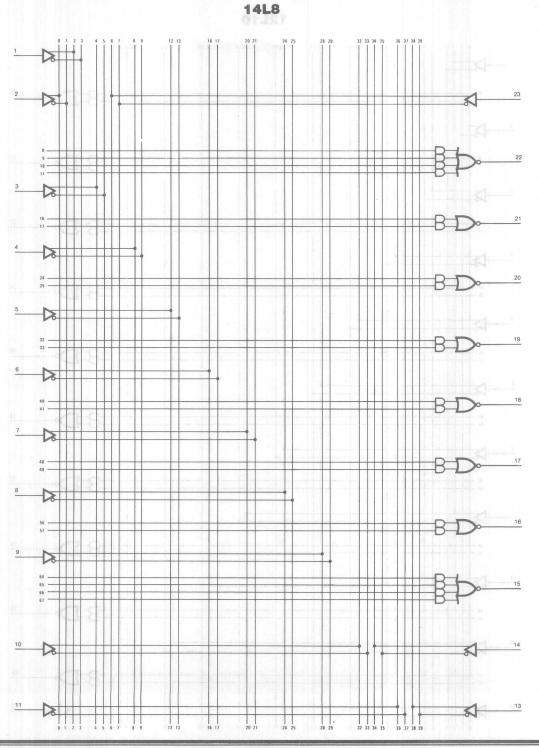






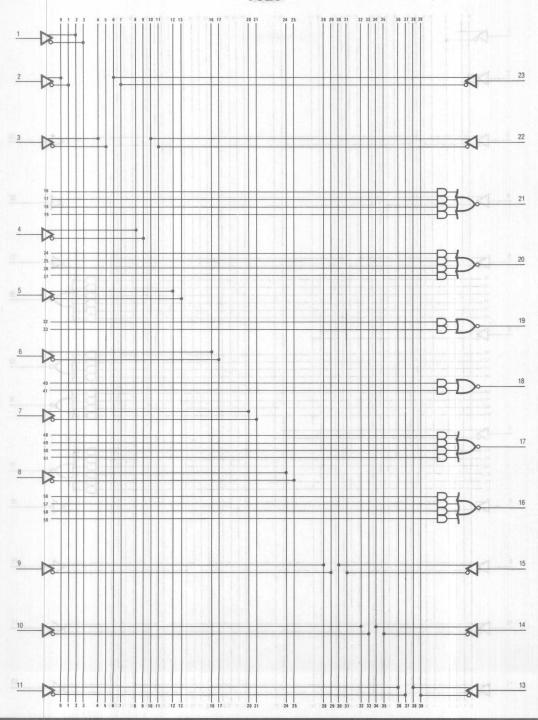
12L10



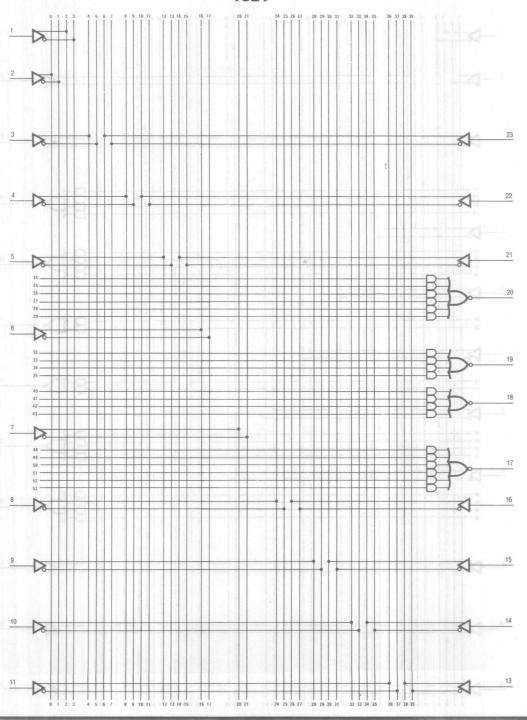


5-76

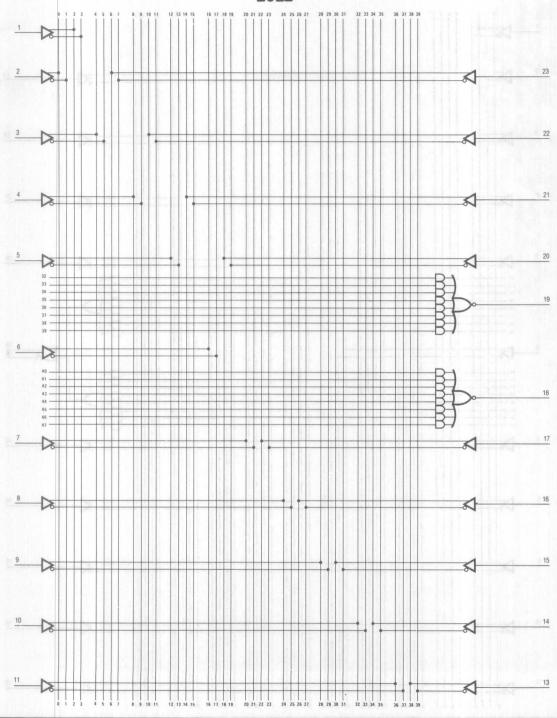
16L6



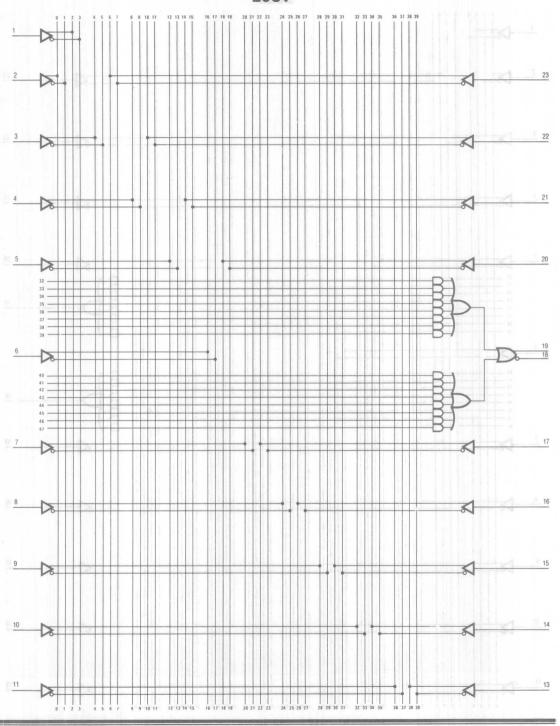






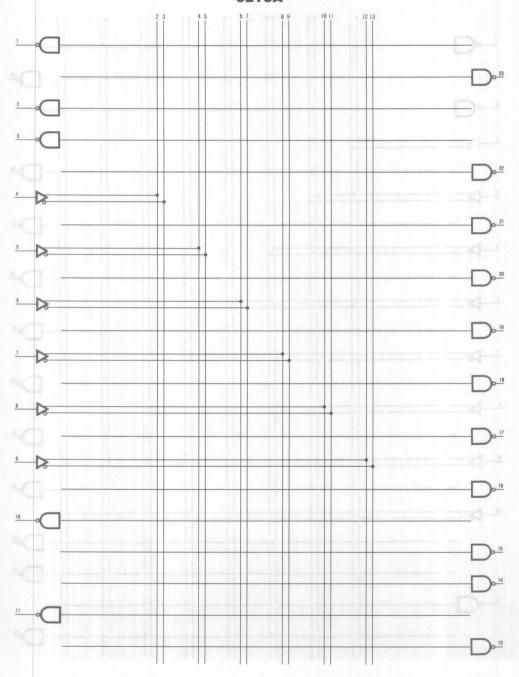






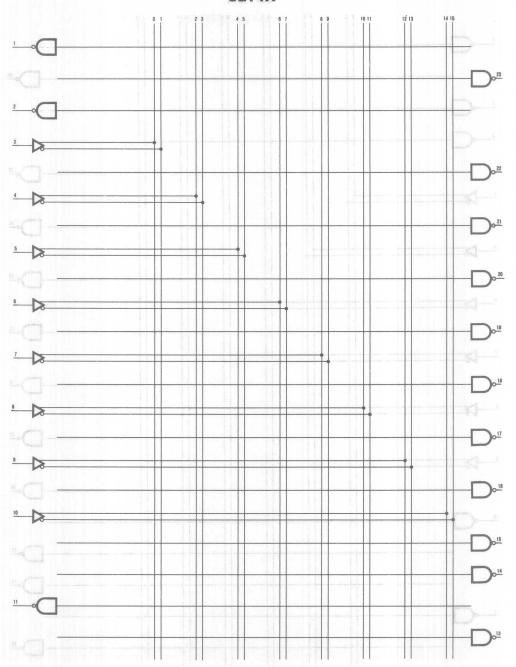
Logic Diagram

6L16A

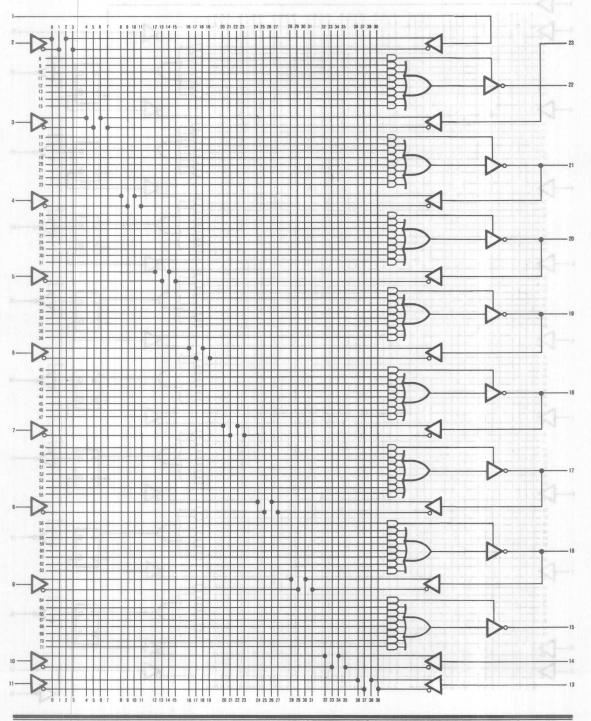


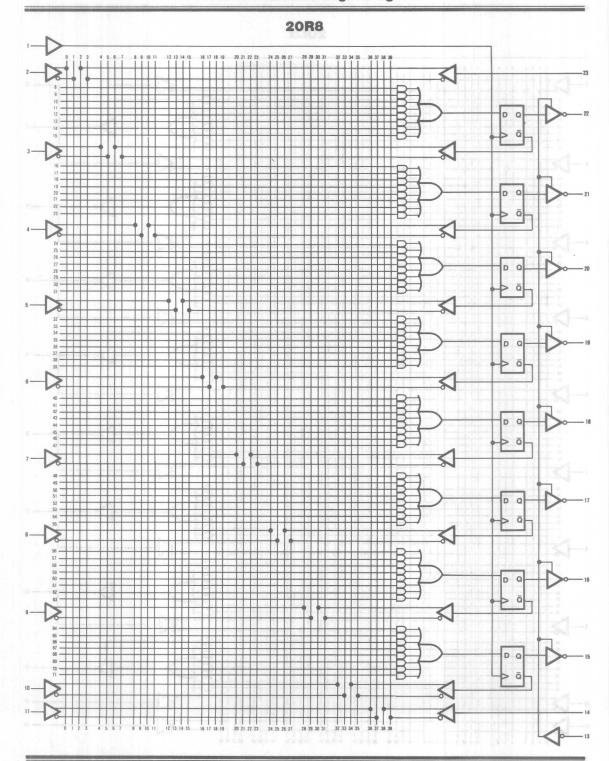
Logic Diagram

8L14A

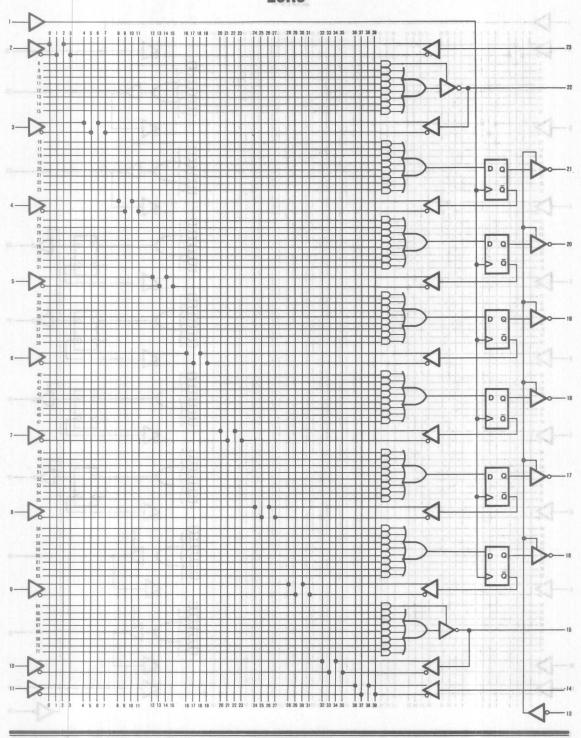


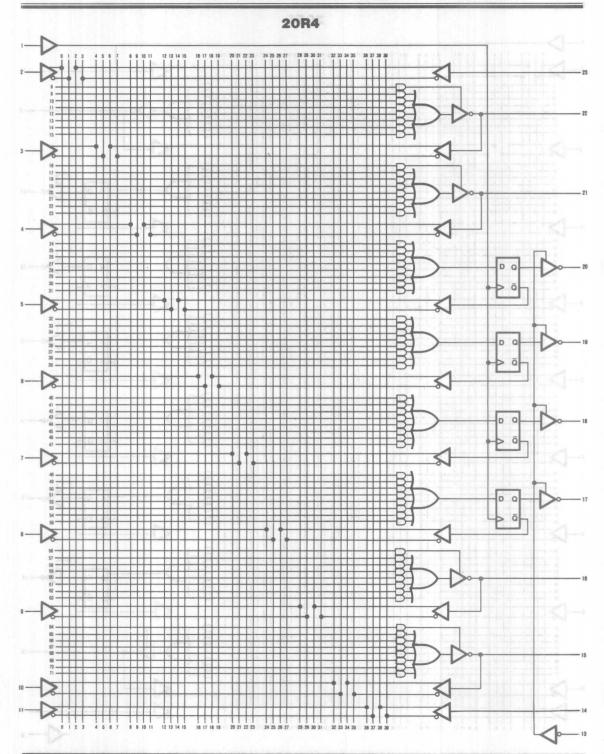
20L8



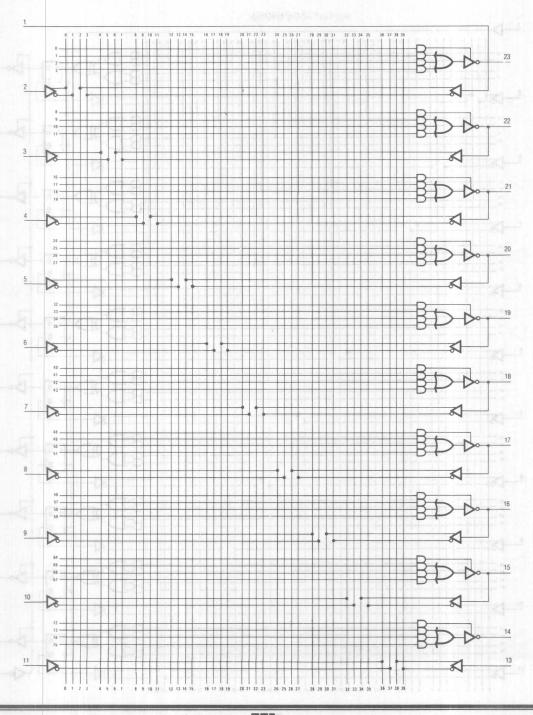


20R6

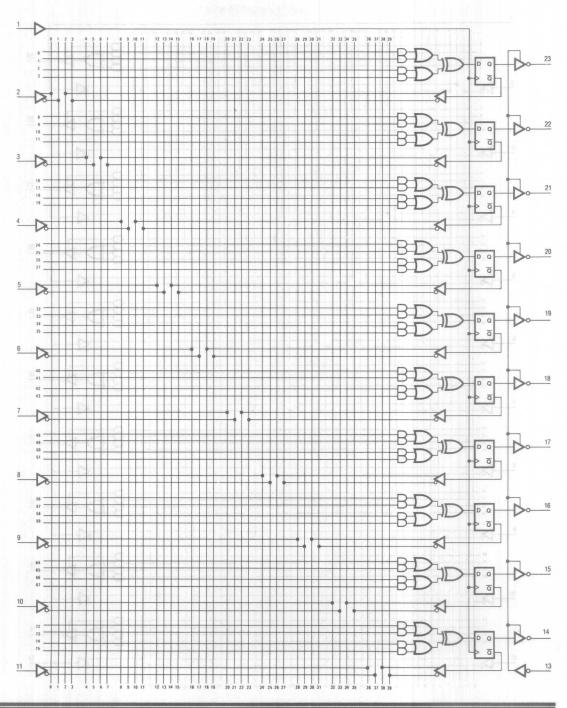




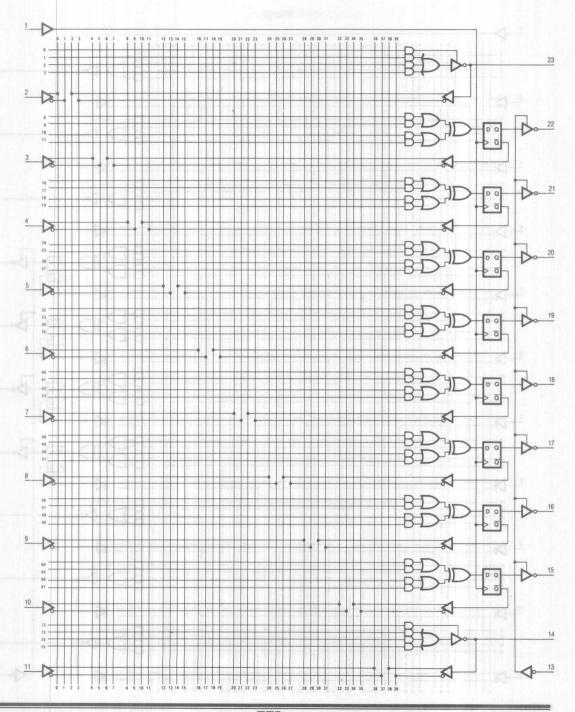
20L10



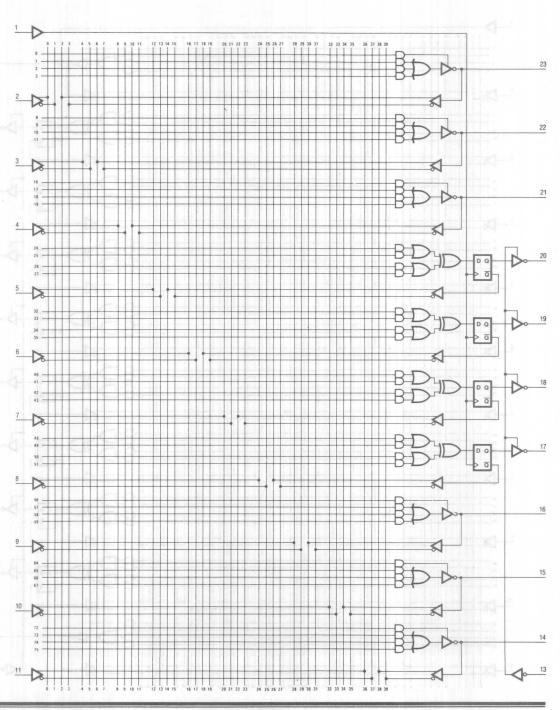
20X10



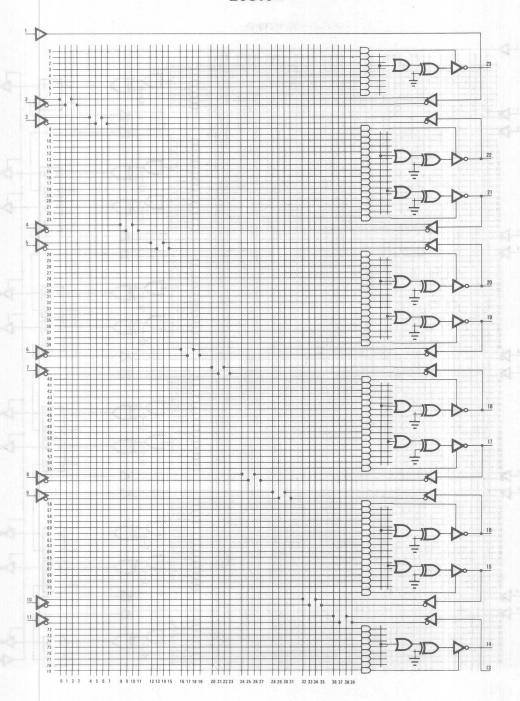
20X8



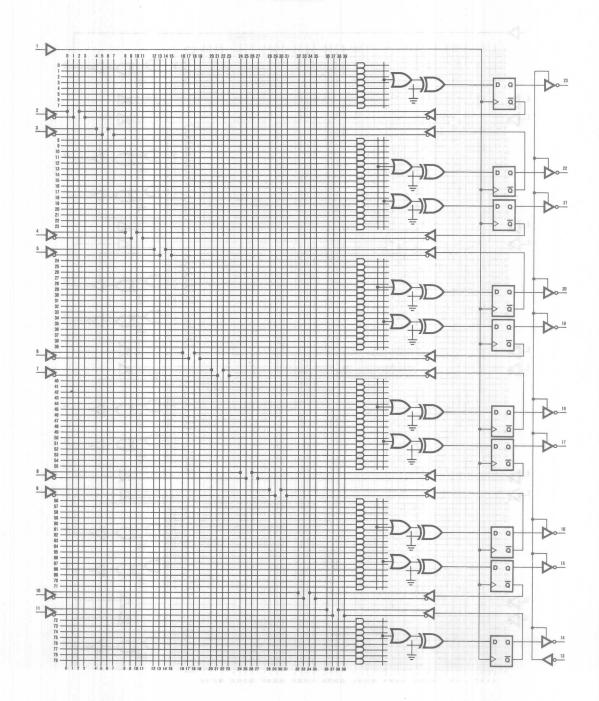
20X4



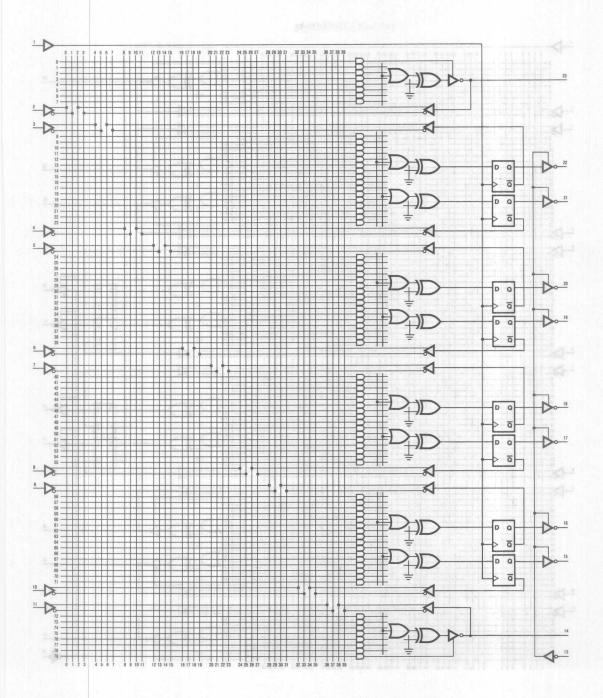
20510



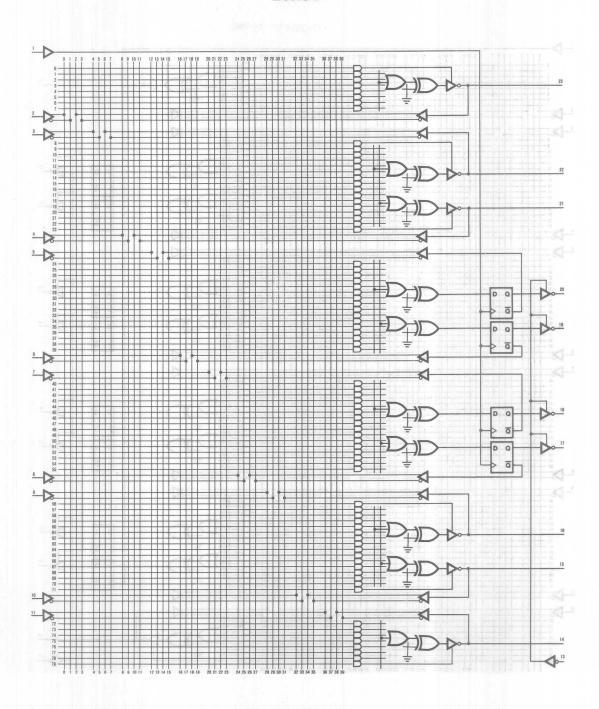
20RS10

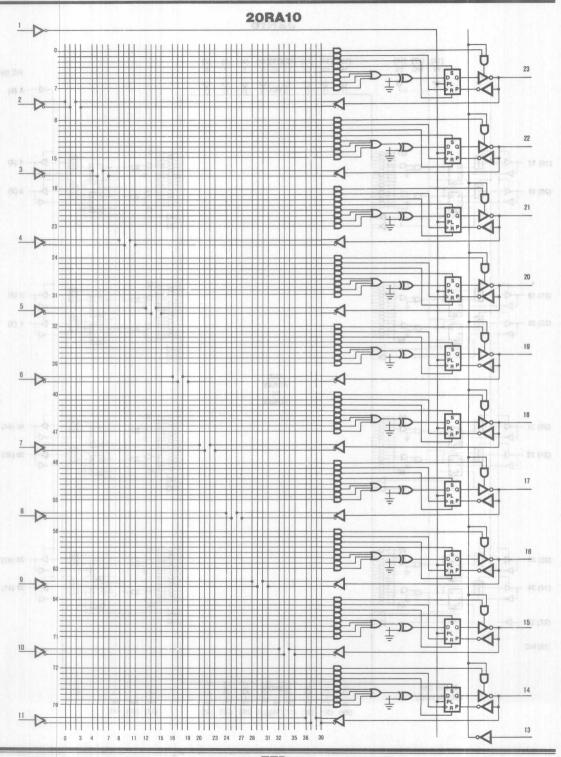


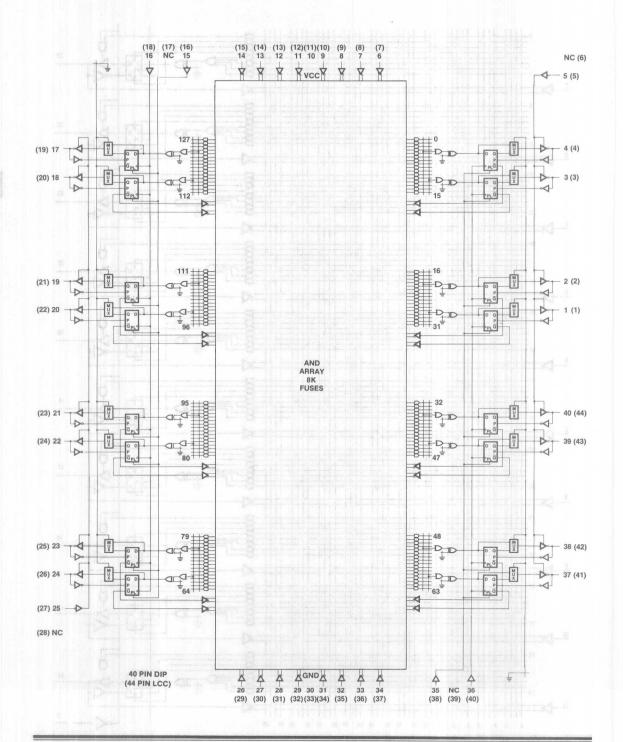
20RS8

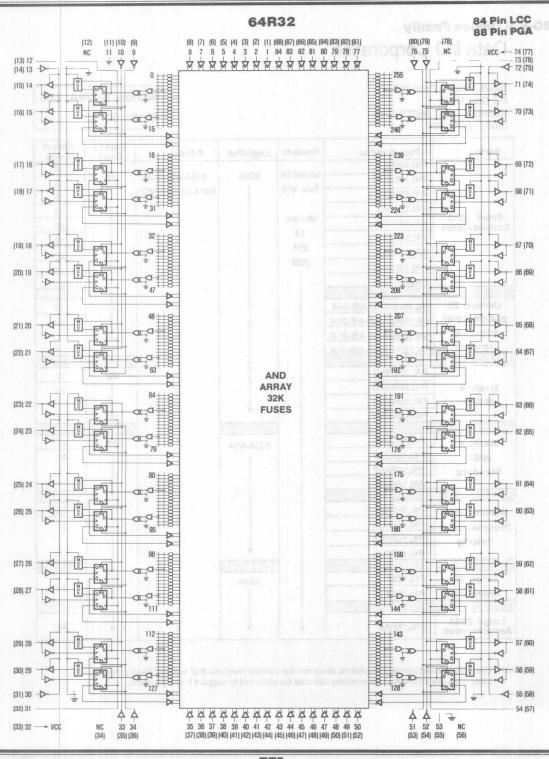


20RS4









Data I/O Corporation

10525 Willows Road N.E. PO Box 97046 Redmond, WA 98073-9746 (800) 247-5700

Models 19, 29A, 29B Model 60

Series	Part Number	System	LogicPak	Adapter	Family Code	Pinou
N TEL GO	PAL10H8/-2			TERM A	The state of	18
	PAL10L8/-2	Model 60	303A	303A-002-V08	22	13
	PAL12H6/-2	Rev. V05		303A-011A/B-VO1	HEAL	19
	PAL12L6/-2			1 1	上上十	14
Small 20/-2 Combinatorial	PAL14H4/-2	Models:		13 1		20
	PAL14L4/-2	19		18-15		15
	PAL16H2/-2	29A		1590		22
	PAL16L2/-2	29B				16
(54) 124-1-24()	PAL16C1/-2			1841.4		21
Medium 20/	PAL16L8/A/-2/-4/B-2/-4			100		17
20A/20A-2/4/	PAL16R8/A/-2/-4/B-2/-4			超 型®		24
20B-2/-4	PAL16R6/A/-2/-4/B-2/-4			E E		191
Standard	PAL16R4/A/-2/-4/B-2/-4					*
	PAL16L8B/D		ULA.	650	30	17
Medium 20B/D	PAL16R8B/D	YA	RESA	ing		24
	PAL16R6B/D		90		-	0 1
	PAL16R4B/D	2012	049-¥			+
Medium	PAL16L8BP		303A-V04		22	17
20BP	PAL16R8BP		303A-V04			67
Standard	PAL16R6BP			55/		
	PAL16R4BP					11-1-2
Medium 20PA	PAL16P8A				11.5	30
Programmable	DALLASDESA			55E		31
Polarity	PAL16RP6A					
Folianty	PAL16RP4A		+	1811		
Large 20	PAL16X4		303A			Mari Fed
Arithmetic	PAL16A4		3007			24
Large 20RA Asynchronous	PAL16RA8					30

24-Pin and MegaPAL™ Device Families

Data I/O

Series	Part Number	System	LogicPak™	Adapter	Family Code	Pinou
System Under	PAL12L10	Model 60	303A	303A-002-V08	22	01
Mound it profite	PAL14L8	Rev. V05		303A-011A/B-V01	81780 U	02
Small 24	PAL16L6				1000000000	03
Combinatorial	PAL18L4	Models:19	STEPHENS	Part Number		04
	PAL20L2	29A		S107-01-12	9	05
	PAL20C1	29B		S-18 / O/ J/		12
Small 24A	PAL6L16A			9-78HS1 1/		48
Decoder	PAL8L14A			(3-10-2-1-0 (3-1-1-1-1-1-1-1-1-1-1-1-1-1-1-1-1-1-1-1	SAU SAU	49
	1			10 VS 56 A L	Cu Balta	
Medium 24A/	PAL20L8A/-2/B			D. 10 LOS F 12		26
24A-2/B	PAL20R8A/-2/B			WAR 159 15		27
Standard	PAL20R6A/-2/B			C 16/20 1/2	G.	
Standard	PAL20R4A/-2/B					
	PAL20L10			-18-85A- 2-VAR-107	AS 55	06
Medium 24X Exclusive-OR	PAL20X10			AS-91- EASTOL	49 106	23
	PAL20X8			LEGAL STANSIEL		13.00
	PAL20X4		1	S. Blood (2002)		
	PAL20L10A		303A-V04	o de la Li		06
Medium 24XA	PAL20X10A		303A-V04	gwianat u		36
Exclusive-OR	PAL20X8A			12.16 (18.84Z)	9	30
	PAL20X4A			3/8*861.3/	9	+
				0.00 to 14		
Large 24RS	PAL20S10			RESPONDE		43
Shared	PAL20RS10	4		98898134	9 1	44
Product Terms	PAL20RS8			2(7),343,1 LA		46
	PAL20RS4					40
Large 24A Registered XOR	PAL22RX8A			303A-011A/B-V01	L Asoc L edar	78
Large 24/A Varied XOR	PAL32VX10/A			ALSENTALA	y.	77
Large 24RA Asynchronous	PAL20RA10		303A	303A-002-V08 303A-011A/B-V01	20 E	45
ECL Combinatorial	PAL10H20P8 1		303A-V04	303A-001ME	ARO	42
MegaPAL™	PAL32R16	Mandaloop	303A	303A-008-A/B	1 secr	47
Devices	PAL64R32	Model 29B		-23/A/B	+	84

Not supported on Model 19

Digelec

1602 Lawrence Ave. Suite 113 Ocean, NJ 07712 (201) 493-2420

System UP803

Series	Part Number	FAM 52 Rev.	Adapter	Adapter Rev
	PAL10H8/-2	5.4	DA53	A-3
	PAL10L8/-2	1 685	281,2001	
	PAL12H6/-2			
Small 20/-2	PAL12L6/-2		PALGLIGA	Smith 24A
Combinatorial	PAL14H4/-2		AM JEJAS	19bere0
	PAL14L4/-2		885448 02 IA9	
	PAL16H2/-2		EVEL/ABBOSLIA*1	Medium 24A/
	PAL16L2/-2		PALEORBA-2/B	24A-278
	PAL16C1/-2		ENS-VAMPOS JAS	barbagiB
Medium 20/	PAL16L8/A/-2/-4/B-2/-4		PALZOLTO	
20A/20A-2/4/	PAL16R8/A/-2/-4/B-2/-4		PAI.20K10	Waddum 24X
20B-2/-4 Standard	PAL16R6/A/-2/-4/B-2/-4		87,05,175	RO-sylapiox3
Standard	PAL16R4/A/-2/-4/B-2/-4		PAL20X4	
	PAL16L8B/D	303A-V04		
Medium	PAL16R8B/D	POV-MODE	PAL20L16A	
20B/D	PAL16R6B/D		ADTACISLASI	AXAS mulbeM
	PAL16R4B/D		PALSO•(8A	RO-sviewax9
	La-vier-			
Medium	PAL16L8BP			
20BP	PAL16R8BP		Under Development	
Standard	PAL16R6BP			
	PAL16R4BP			omin'i buhasi
Medium 20PA	PAL16P8A	5.4	DA53	A-3
Programmable	PAL16RP8A	1	A DASS	Rox betterned
Polarity	PAL16RP6A			
rolatity	PAL16RP4A		PALSEVXYOR	Lexis 24M. Veried XOR
			March that is	
Large 20	PAL16X4	A000	OFASIOSJAS	Large ZAFIA
Arithmetic	PAL16A4		1	auonouda yaA
Large 20RA Asynchronous	PAL16RA8	0.004800	Under Development	Compleatenal

24-Pin and MegaPAL™ Device Families

Digelec

Series	Part Numbers	FAM 52	Adapter	Adapter Rev.
	PAL12L10	5.4	DA55	Nounter C-1
	PAL14L8	5.4	DA33	415) 365-7029
Small 24	PAL16L6			
Combinatorial	PAL18L4		redmost :	Series Par
	PAL20L2		\$-8H0	194
	PAL20C1	+	\$-18.10	119
Small 24A	PAL6L16A		11.1.5.1	
Decoder	PAL8L14A		Under Developm	ent C-16% Hems
Medium 24A/	PAL20L8A/-2/B	5.4	DA55	C-1
24A-2/B	PAL20R8A/-2/B		DASS	
Standard	PAL20R6A/-2/B		61.27-2	
Standard	PAL20R4A/-2/B		\$417.0	
	PAL20L10		\$1.87A7-2 -47B-27-4	Redium 28/ PALII
Medium 24X	PAL20X10		FISIAL-21-4/8-21-4	2040'20 L-2444 PAL10
Exclusive-OR	PAL20X8		A-IS-BUANDAMARK	208-1-4 PALI
Exclusive-On	PAL20X4		NESS SIAL PLANERS	Standard page
	PAL20L10A		Crearia	
Medium 24XA	PAL20X10A		0.8899	
Exclusive-OR	PAL20X8A		GREED	[143] G 805
	PAL20X4A		Q6) Sq	4
	PAL20S10		161.000	JA mulbeli
Large 24RS	PAL20RS10		Reader	
Shared	PAL20RS8		Reagan	
Product Terms	PAL20RS4		199439	
Large 24A Registered XOR	PAL22RX8A		ABSIBI	THE WART WITH SHIP
			1089984	and the state of t
Large 24/A Varied XOR	PAL32VX10/A		A899ar	F 52 CH 72 C
varied XON			Aarseas	
Large 24RA	PAL20RA10		- AX8:	Larry 20 I IAL
Asynchronous	,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,		AABI	
ECL Combinatorial	PAL10H20P8			A 800 anna 1
MegaPAL TM	PAL32R16			
Devices	PAL64R32	Under Development		

Kontron

1230 Charleston Road Mountain View, CA 94039-7230 (415) 965-7020 System MPP-80S System EPP-80

			bg flemst
Series	Part Number	UPM-B Rev.	Conditionation
	PAL10H8/-2	1.44	
	PAL10L8/-2	PALZOGI	
	PAL12H6/-2		
Small 20/-2 Combinatorial	PAL12L6/-2	PALSLIA	
	PAL14H4/-2	A17 16 A3	
	PAL14L4/-2	B S AVE DO LAS	
	PAL16H2/-2	ENS-VERTOS JAS	
	PAL16L2/-2	PAL20FOAA28	
	PAL16C1/-2	BIS VANEOS IA	
Medium 20/	PAL16L8/A/-2/-4/B-2/-4	PAL20LID	
20A/20A-2/4/	PAL16R8/A/-2/-4/B-2/-4	041.203/10	
20B-2/-4	PAL16R6/A/-2/-4/B-2/-4	SKOC JAC	
Standard	PAL16R4/A/-2/-4/B-2/-4	AKSC. IA	
		hater a second second	
	PAL16L8B/D	A01105 1/4	
Medium	PAL16R8B/D	ADRIKOSJAS	
20B/D	PAL16R6B/D	PALSONIA	
	PAL16R4B/D	As Wester	
Medium	PAL16L8BP	PALZOSID	
20BP	PAL16R8BP		USM egiel
Standard	PAL16R6BP	Under Developmen	t beind
Standard	PAL16R4BP	68605.IAS	Error Toubor9
	PAL16P8A	A1.44	Corres 24461
Medium 20PA	PAL16RP8A	41.44	
Programmable	PAL16RP6A		
Polarity	PAL16RP4A	ADIXVSEJAS	
	TALIOTTAA		
Large 20	PAL16X4	PALZORATO	
Arithmetic	PAL16A4		100 00 100 100 100 100 100 100 100 100
Large 20RA Asynchronous	PAL16RA8	1.47	netarandingo Marandingo

20-Pin Davice Femily

24-Pin and MegaPAL™ Device Families

Kontron

Series	Part Number	UPM-B Rev.
entruspera i F	PAL12L10	1.44 pasA'b-evicenelii 1 0886
	PAL14L8	et 20479040
Small 24	PAL16L6	
Combinatorial	PAL18L4	Serie Part Number
	PAL20L2	PALIGHAL
	PAL20C1	PARTOLINE PARTOLINE
Small 24A	PAL6L16A	THE PART OF THE PA
Decoder	PAL8L14A	1.48
The second of	T ALOCI TA	
Madium 044/	PAL20L8A/-2/B	1.44
Medium 24A/	PAL20R8A/-2/B	b-selective.
24A-2/B Standard	PAL20R6A/-2/B	PALIBITING
Standard	PAL20R4A/-2/B	PALIBOTAL
	PAL20L10	Slociary 20/ PAL ISLAND AND AND AND
	PAL20X10	04/2014 PAL 1038/APA 21-48
Medium 24X	PAL20X8	208-2/-A PALISREAL WAR 2/-A
Exclusive-OR	PAL20X4	BASE SALAR S
	TALLONG	P-15-09-15-14-101-14-11
	PAL20L10A	PALISIBEL
Medium 24XA	PAL20X10A	Wedium Patrickes
Exclusive-OR	PAL20X8A	potato PAL TERSBID
	PAL20X4A	PALIGRABID [
	PAL20S10	
Large 24RS	PAL20RS10	Majorita PALTOLOGIA
Shared	PAL20RS8	PALIGRED FALLERS
Product Terms	PAL20RS4	Standard ENJORD
	FALZUNG4	
Large 24A Registered XOR	PAL22RX8A	Pedium 2014 PAL (SP84
Large 24/A Varied XOR	PAL32VX10/A	1.48
Large 24RA Asynchronous	PAL20RA10	1.44 co abrel
ECL Combinatorial	PAL10H20P8	1.47
MegaPAL™	PAL32R16	Buoncepage
Devices	PAL64R32	Under Development

20-Pin Device Family Micropross

Tel 20479040

Parc d'activite des Pres 5, rue Denis-Papin 59650 Villeneuve-d'Ascq

ROM 5000 Programmer

24-Pin and MegaPAL Cevice Femilies

Series	Part Number	Rev.	Complantavial
	PAL10H8/-2	3.5	
	PAL10L8/-2	3.5	
	PAL12H6/-2	A8 18 A	
Small 20/-2	PAL12L6/-2	PALSLIAA	
Combinatorial	PAL14H4/-2		
	PAL14L4/-2	PARTUS IA	
	PAL16H2/-2	BAS-AA-805 JAS	
	PAL16L2/-2	BIS VALEDO LA FILIPIA	
	PAL16C1/-2	80.14.80.17	
Medium 20/	PAL16L8/A/-2/-4/B-2/-4	0 308349	
20A/20A-2/4/	PAL16R8/A/-2/-4/B-2/-4	6 67 5000 6	
20B-2/-4	PAL16R6/A/-2/-4/B-2/-4	BXB5.D	
Standard	PAL16R4/A/-2/-4/B-2/-4	40405,IA7	
	PAL16L8B/D		
	PAL16R8B/D	A01.201.10S	
Medium		AO XX LAT	
20B/D	PAL16R6B/D	At XOS JA	
	PAL16R4B/D	Lisa Lilian Amisias La	
Medium	PAL16L8BP	DESCRIPTION	
20BP	PAL16R8BP		Large 2185
Standard	PAL16R6BP	Under Development	
Otanuara	PAL16R4BP	MARIO (AO L	white bullout
	PAL16P8A	3.5	
Medium 20PA	PAL16RP8A	3.5	SOX besetzigeR
Programmable	PAL16RP6A	1 430174001447	AV-S epas.
Polarity	PAL16RP4A	PAL38VIOIA	
		OPARCS JAF	
Large 20	PAL16X4		
Arithmetic	PAL16A4		
Large 20RA Asynchronous	PAL16RA8	Under Development	Manager and Salar Sa Manager Salar S

24-Pin and MegaPAL™ Device Families

Micropross

Series	Part Number		Rev.	
m me too 3	PAL12L10	THE PARTY	ALDOLD ALDOLD	Manter v. CA. 1
	PAL14L8		3.5	
Small 24	PAL16L6			
Combinatorial	PAL18L4	Software Rev.	Part Institut	
P.	PAL20L2	3.0	2-18110114611	
	PAL20C1	Land State	FALIGIAR	
Small 24A	PAL6L16A			
Decoder	PAL8L14A		Under Development	
Decodel	FALOL 14A			
80	PAL20L8A/-2/B		\$40,940,345	
Medium 24A/	PAL20R8A/-2/B		3.5	
24A-2/B	PAL20R6A/-2/B		PAL18L2-2	
Standard	PAL20R4A/-2/B		PALIBOUR	
	Language		A CARA LANGER AT	Control of the set
	PAL20L10		2.12.90AAQAMA999 1A9	
Medium 24X	PAL20X10		INTO BIS AND AND THE STATE OF T	
Exclusive-OR	PAL20X8		4-10-49-11-AU-921-14-9	
	PAL20X4			
	Tanana		PACTELSER	
	PAL20L10A		PAC 1678040	
Medium 24XA	PAL20X10A		PALISPERIT	
Exclusive-OR	PAL20X8A		PALISHABA	
	PAL20X4A			
	PAL20S10		PAL161J89F	
Large 24RS	PAL20RS10		PAL IGRADE	
Shared	PAL20RS8		PALISPER	
Product Terms	PAL20RS4		PAL169481	
Large 24A Registered XOR	PAL22RX8A	0.0	PALISPEA	
riegioterea Xerr			APPRILIAN	
Large 24/A	PAL32VX10/A			
Varied XOR	TALSEVATOR		PALIFERRAL	
Large 24RA	BulcoBase			
Asynchronous	PAL20RA10		PALTEXAL	Large 20
	N SOUTH		PA1.18A4	
ECL Combinatorial	PAL10H20P8		•	ACIDE ANNEL
MegaPAL™	PAL32R16			
Devices	PAL64R32		Under Development	

Promac

Adams MacDonald Enterprises, Inc. 2999 Monterey/Salinas Highway Monterey, CA 93940 (408) 373-3607 Promac P3
Programmer

Series	Part Number	Software Rev	. 4.1	PALH	S1/S2
	PAL10H8/-2	3.0	8.40	RELAY J	0/1
	PAL10L8/-2		10	SJAT	0/6
	PAL12H6/-2		348.00		0/2
CII 00/ 0	PAL12L6/-2		Aar	IO JAY'S	0/7
Small 20/-2 Combinatorial	PAL14H4/-2		Abi	Part Time	0/3
	PAL14L4/-2		84-28	PALZE	0/8
	PAL16H2/-2		-BISAASB	15 PAR 21	0/4
	PAL16L2/-2		ELS-VASED	PAL20	0/9
	PAL16C1/-2		EAS-VANE	BE JAS I	0/5
Medium 20/	PAL16L8/A/-2/-4/B-2/-4		01.1	ic las	0/10
20A/20A-2/4/	PAL16R8/A/-2/-4/B-2/-4		013	PALSE	0/11
20B-2/-4	PAL16R6/A/-2/-4/B-2/-4		BX	ne 13-0	0/12
Standard	PAL16R4/A/-2/-4/B-2/-4		15	10 1250	0/13
	PAL16L8B/D				5/0
Medium	PAL16R8B/D		A03.1	2014.0	5/1
20B/D	PAL16R6B/D		AGTN	SC 14 2	5/2
208/0	PAL16R4B/D	1	ABX	SD DAG	5/3
Medium	PAL16L8BP		0180	PALZ	
20BP	PAL16R8BP		etani	ALZO	
Standard	PAL16R6BP		Under Dev	elopment	
	PAL16R4BP		1200	SCHAO	arms Ellesberg
Medium 20PA	PAL16P8A	3.0	ASXA	CLIAC I	A 1/0 - 1218-3
	PAL16RP8A	3.0	SOAT	N. 3.59N	1/3
Programmable	PAL16RP6A				4.10
Polarity	PAL16RP4A		Algrany	PALS	1/1
Large 20	PAL16X4		01/48	ELIA	0/14
Arithmetic	PAL16A4				0/15
Large 20RA Asynchronous	PAL16RA8		8900H	TEACH TO SERVICE STATES	74 14 14 14 14 14 14 14 14 14 14 14 14 14

24-Pin and MegaPAL™ Device Families

Promac

Series	Part Number	Software Rev.	S1/S2
7.00	PAL12L10	3.0	2/2
	PAL14L8	1	2/3
Small 24	PAL16L6		2/4
Combinatorial	PAL18L4	ebo and	2/5
	PAL20L2	08-09	2/6
	PAL20C1	82-8	2/1
		19-19	
Small 24A	PAL6L16A	89-48	3/11
Decoder	PAL8L14A	80.02	3/10
	PAL20L8A/-2/B	10-05	2/8
Medium 24A/	PAL20R8A/-2/B	62-05	2/9
24A-2/B	PAL20R6A/-2/B	86-46	2/10
Standard	PAL20R4A/-2/B	20-24	2/11
	TALZOTHA ZIB		2/11
	PAL20L10	63-02 4-9-84-1	2/7
Medium 24X	PAL20X10	18-92 1 18-814	2/12
Exclusive-OR	PAL20X8	12.42 3-2.50-1	2/13
	PAL20X4	148-2-4	2/14
		69-15	
	PAL20L10A	2 30	2/7
Medium 24XA	PAL20X10A		2/15
Exclusive-OR	PAL20X8A	80.6	3/0
	PAL20X4A		3/1
	PAL20S10		3/5 ctalled 4
Large 24RS	PAL20RS10		3/6
Shared	PAL20RS8		3/7
Product Terms	PAL20RS4		3/8
FIGURE 15 THE ST			
Large 24A Registered XOR	PAL22RX8A	88.48 11.48	ASSELSAS LASUR multiple
Large 24/A Varied XOR	PAL32VX10/A	81-18	Argantas I naigh
Large 24RA Asynchronous	PAL20RA10	65-65 36-82	3.4
ECL Combinatorial	PAL10H20P8		AF S eggs.
MegaPAL™	PAL32R16		
Devices	PAL64R32	Under Dev	relopment

Stag Microsystems

528-5 Weddell Drive Sunnyvale, CA 94089 (408) 745-1991 ZL30 PPZ

100000000000000000000000000000000000000		Name and Advantage of the Parket of the Park	Spanist Service	18734 YY CHRESTER
Series	Part Number	Code	ZL30 Rev.	Zm2200
als	PAL10H8/-2	20-20	30-35	14
	PAL10L8/-2	20-25	PALZING	
	PAL12H6/-2	20-21		
Small 20/-2	PAL12L6/-2	20-26	PALGLYIA	Small SAA
Combinatorial	PAL14H4/-2	20-22	PALBLILA AILJBJAS	1900190
	PAL14L4/-2	20-27	PALPOLIAN 28	
	PAL16H2/-2	20-23	PALZORPAL-2/B	Medico 26A
	PAL16L2/-2	20-28	SIC LAS SIOCIAS	2dA-2/8
FACE	PAL16C1/-2	20-24	PALZORIAN-SIB	Standard
Medium 20/	PAL16L8/A/-2/-4/B-2/-4	20-29	PAL206 0	
20A/20A-2/4/	PAL16R8/A/-2/-4/B-2/-4	20-30	PALEOXIO	
20B-2/-4	PAL16R6/A/-2/-4/B-2/-4	20-31	PALSONS	Madhan 24X
Standard	PAL16R4/A/-2/-4/B-2/-4	20-32	- Weiling	SO-evi-uloxa
	PAL16L8B/D	22-29	30-39	12
Medium 20B/D	PAL16R8B/D	22-30		
	PAL16R6B/D	22-31	P. (20X 0A	Windsom 24X04
200/0	PAL16R4B/D	22-32	PAL20XBA	HO-avia dox3
1 1 1 1 1 1 1 1 1	TALIGRAD			
Medium	PAL16L8BP		PALSOS10	
20BP	PAL16R8BP		Under Developmen	Large 24ffS
Standard	PAL16R6BP		agang Ag	Shared
	PAL16R4BP		22002129	and the ne
Medium 20PA	PAL16P8A	20-38	30-35 SJAG	AIS 12
Programmable	PAL16RP8A	20-11	00 00	ROX paratelpo
Polarity	PAL16RP6A	20-12		Lange 24 A
Folarity	PAL16RP4A	20-13	PALSSVICION	FOX MahreV
				I AN AS AN AS
Large 20	PAL16X4	20-33	P41.20F410	14
Arithmetic	PAL16A4	20-34		
Large 20RA Asynchronous	PAL16RA8	20-19	30-37	12

24-Pin and MegaPAL™ Device Families

Stag Microsystems

Series	Part Number	Code	ZL30 Rev.	ZM2200
	PAL12L10	21-50	30-35	14 374.8
	PAL14L8	21-51	8150	Viesquite FX 7
Small 24	PAL16L6	21-52		12
Combinatorial	PAL18L4	21-53		0415124
	PAL20L2	21-54	Part Mumber	. Returned L
	PAL20C1	21-55		+
Small 24A	PAL6L16A		Para de l'expressor	
			Under Developmen	t
Decoder	PAL8L14A			La rancial de la company
	PAL20L8A/-2/B	21-56	30-35	12
Medium 24A/	PAL20R8A/-2/B	21-57	Legar Ma	1
24A-2/B	PAL20R6A/-2/B	21-58	PAL1812F3	
Standard	PAL20R4A/-2/B	21-59	PALIBOTAS PALIBOTAS	
100	PAL20L10	21-60		
	PAL20X10	21-61	PAL 16L3/A) - (21-A/B-21-1	Modium 20:
Medium 24X	PAL20X8	21-62	PAL16R8/A-2/-4/8-2/-4	10A/20A-2/4/
Exclusive-OR	PAL20X4	21-63	PAL16R6M-8/-4/8-8/-4	P-3-802
	PAL2UA4	21-03	PAL 16 144A - 121- 418-21-4	t stanta
	PAL20L10A	21-60	PALISLEGIO	
Medium 24XA	PAL20X10A	21-61	CALIGRADI	Josef
Exclusive-OR	PAL20X8A	21-62	PALIERER	808
	PAL20X4A	21-63	PAR LARGERY	
	PAL20S10	21-81		
Large 24RS	PAL20RS10	21-80	30-39	Modles
Shared	PAL20RS10	21-79	PALISPAIR	2096
Product Terms	PAL20RS4	21-79	PALISBOIR	Stand: d
Troduct Terms	PALZUN34	21-70	United States of the States of	ber televis
Large 24A Registered XOR	PAL22RX8A		PALISPBA	Ledwo 20PA
Large 24/A Varied XOR	PAL32VX10/A		PAUISPECA	Polyrius Both
Large 24RA Asynchronous	PAL20RA10	21-77	30-37	C sgrad
ECL Combinatorial	PAL10H20P8			alto a dila A.
MegaPAL™	PAL32R16			- strenomismys
Devices	PAL64R32	Under Development		

Storey Systems

3201 North Hwy. 67 Suite H Mesquite, TX 75150 (214) 270-4135 P240 Programmer

Series	Part Number		Rev.	THE REPORT OF THE PARTY OF
	PAL10H8/-2	68-19	- K-Miller	
	PAL10L8/-2		2.0	
	PAL12H6/-2		ARRIBLISS	
Small 20/-2	PAL12L6/-2		AAFJB ING	
Combinatorial	PAL14H4/-2			
	PAL14L4/-2		8'S 48 US 19	
	PAL16H2/-2			
	PAL16L2/-2		88-A8-RIS.M	
	PAL16C1/-2		BYS-AMPRICAL CO.	
Medium 20/	PAL16L8/A/-2/-4/B-2/-4		0 .08.14-	
20A/20A-2/4/	PAL16R8/A/-2/-4/B-2/-4		64K29M46	
20B-2/-4	PAL16R6/A/-2/-4/B-2/-4		10.03.14	
Standard	PAL16R4/A/-2/-4/B-2/-4		VOS.IA*	
	DAL (OLODIO			
	PAL16L8B/D		4.0	
Medium	PAL16R8B/D		A A A STATE OF THE	
20B/D	PAL16R6B/D		A Dres Div	
	PAL16R4B/D			
Medium	PAL16L8BP			teras-ears_
20BP	PAL16R8BP		Under Development	
Standard	PAL16R6BP			
	PAL16R4BP	5721S	A PROSING	1 107 201 1 3 21 12 20 1 7
	PAL16P8A		EUGENEE .	SIGNA TORNAL FILLERS
Medium 20PA	PAL16RP8A		4.0	
Programmable	PAL16RP6A		AST VSE AT	
Polarity	PAL16RP4A		THE STATE OF THE S	
Large 20	PAL16X4		2.0	
Arithmetic	PAL16A4			
Large 20RA Asynchronous	PAL16RA8		4.04	JARapaM
	menideland of admini		6.00 S 14.0	Decireos

24-Pin and MegaPAL™ Device Families

Storey Systems

Series	Part Number		Rev.	
	PAL12L10		2.0	T sign
mesive doot t	PAL14L8		10000	
Small 24	PAL16L6			
Combinatorial	PAL18L4		Part Number	
	PAL20L2		P. (8/80) AQ	
C9.1	PAL20C1	3.1	0.00 101 105	
Small 24A	PAL6L16A		ESSOCIETATION	
Decoder	PAL8L14A		Under Development	
Decoder	PALOL14A			o blank thems
	PAL20L8A/-2/B		2.0	
Medium 24A/	PAL20R8A/-2/B		18-35Har JA4	
24A-2/B	PAL20R6A/-2/B		835,381,349	
Standard	PAL20R4A/-2/B		SALTSCIAR	
	PAL20L10		Maria Jan Jar Jar Jar Jar	
	PAL20X10		540/BW-01-A98871-A9	
Medium 24X	PAL20X8		PALLORGAN DIAMETERS	
Exclusive-OR	PAL20X4		×49-894 (2.149	
	TALLON			
	PAL20L10A		0.68,131,169	
Medium 24XA	PAL20X10A	The second	Q Q (A C) A C)	ergit (codi)
Exclusive-OR	PAL20X8A	Quider Davelop	Under Development	
	PAL20X4A		PALIBRANCE	
	PAL20S10		186 (St. 184	
Large 24RS	PAL20RS10		48899144	lifedium
Shared	PAL20RS8		PALISPISE	
Product Terms	PAL20RS4		MARIOLIAS	
Large 24A Registered XOR	PAL22RX8A		ASPat JA9	ARC: mulask
Large 24/A	T		ASSESSA VI	
Varied XOR	PAL32VX10/A			9-38109
Large 24RA Asynchronous	PAL20RA10		4.04	
Asyliciliolious			(1) (1) (1) (1) (1) (1) (1) (1) (1) (1)	
ECL Combinatorial	PAL10H20P8			
MegaPAL™	PAL32R16			
Devices	PAL64R32		Under Development	

Structured Design

1700 Wyatt Drive Suite 7 Santa Clara, CA 95054 (408) 988-0725 SD 20/24 System SD 1000 System

Series	Part Number	SD 20/24	V. 61 W	SD 1000
	PAL10H8/-2	1.6	Z 627V.	1.05
	PAL10L8/-2		FODSJA"	
	PAL12H6/-2		And night	Smell 26A
	PAL12L6/-2		AM IS IA A	Deceder
Small 20/-2 Combinatorial	PAL14H4/-2			
	PAL14L4/-2		8/S-VA8 I09 JA	
	PAL16H2/-2		PALSOREAL SIB	Medium 24A
	PAL16L2/-2		21 20 86A-2/B	5 S-A4S
	PAL16C1/-2		PIS ANTOSIA	Stendard
Medium 20/	PAL16L8/A/-2/-4/B-2/-4		01.03.14	
20A/20A-2/4/	PAL16R8/A/-2/-4/B-2/-4		PALSONIS	Valle and the same
20B-2/-4	PAL16R6/A/-2/-4/B-2/-4		AL2018	Madium 24X Exclusive-OR
Standard	PAL16R4/A/-2/-4/B-2/-4	+	2003 JAS	MU-INSSEES
Otanaara	FALTON4/A/-2/-4/D-2/-4			
	PAL16L8B/D		PAL20_10A	Action in the same of the same of the same
Medium	PAL16R8B/D	Under Development	PALZOGOA .	Madisan 24XA Exclusive-OR
20B/D	PAL16R6B/D		PALZOKBA	
	PAL16R4B/D		AMOSJAS	*
	L DALLOLODD		PACEOSTU	
Medium	PAL16L8BP			
20BP	PAL16R8BP			
Standard	PAL16R6BP			
	PAL16R4BP			
	PAL16P8A		Under Developmen	
Medium 20PA	PAL16RP8A			
Programmable	PAL16RP6A			
Polarity	PAL16RP4A			
	FALIONF4A			
Large 20	PAL16X4		- VIAITADAN	- Asynchronous -
Arithmetic	PAL16A4	1.6		1.05
Large 20RA			Under Developmen	

24-Pin and MegaPAL™ Device Families

Structured Design

Series	Part Number	SD 20/24	1	A S S	D 1000
Programme	PAL12L10	1.6		DHOM	1.05
	PAL14L8			lountain 20.10, CA 91043	
Small 24	PAL16L6				are a constant
Combinatorial	PAL18L4	168/0		Serion Part Nu	
	PAL20L2			PALTUHSA-2	
	PAL20C1	*		PAL101.84-2	*
Small 24A	PAL6L16A				
Decoder	PAL8L14A		Under D	Development	
Decoder	TALOLITA			0.11321.012.0	
	PAL20L8A/-2/B	1.6		PALIFIAS	1.05
Medium 24A/	PAL20R8A/-2/B	1.6		PAL18H2A	1.05
24A-2/B	PAL20R6A/-2/B			PALTGLE P	
Standard	PAL20R4A/-2/B			PAL16C1	
	PAL20L10			PAL I SLOVA	Media 24
Medium 24X	PAL20X10		1-8-8-6	PALISPBIA	DAZ ADSTAU
Exclusive-OR	PAL20X8			PALIBRIAN.	p- 3-805
Exclusive-On	PAL20X4			PAL18RA/A	b-shnat#
	PAL20L10A			PALTELES	
Medium 24XA	PAL20X10A			PALIGRAR	carboll.
Exclusive-OR	PAL20X8A	1		PALTERSB	3/802
	PAL20X4A	· · · · · · · · · · · · · · · · · · ·	L	PALTER48	
	PAL20S10			asisiat MS	n. sheti
Large 24RS	PAL20RS10		Under [Development	
Shared	PAL20RS8			PALIGRAD	
Product Terms	PAL20RS4			BARBILAS	
Large 24A Registered XOR	PAL22RX8A			PALIBREA	
				PALIERPS	eldan marger
Large 24/A Varied XOR	PAL32VX10/A			PAL18RPE	
				PALISHPA	
Large 24RA Asynchronous	PAL20RA10			PALIGXA	
Asylicinolidus				PALIGA	
ECL Combinatorial	PAL10H20P8				ARCS egra.
MegaPAL™	PAL32R16			PALTERAS	anon-indonys
Devices	PAL64R32			*	

Valley Data Sciences

Charleston Business Park 2426 Charleston Road Mountain View, CA 94043 (415) 968-2900 160 Series Programmer

		the state of the s	DATE BURNINGS
Series	Part Number	Rev. B JA	Combination
	PAL10H8/-2	\$40.53.04.2	
	PAL10L8/-2	1.03	
	PAL12H6/-2		
	PAL12L6/-2	ABIJELIEA	
Small 20/-2 Combinatorial	PAL14H4/-2	ANLOUNT	
Combinatorial	PAL14L4/-2	E Standard Control	
	PAL16H2/-2	A.F. BUS-VARROS LA	
	PAL16L2/-2	88 V42 F0S	
	PAL16C1/-2	2-AL2084AA26G	
Little Control			
Medium 20/	PAL16L8/A/-2/-4/B-2/-4	0.4284.0	
20A/20A-2/4/	PAL16R8/A/-2/-4/B-2/-4	0.000.00	
20B-2/-4	PAL16R6/A/-2/-4/B-2/-4	ALRONE	
Standard	PAL16R4/A/-2/-4/B-2/-4	EPACTORS STORY	4
	L DAL 4 CL OD/D		
	PAL16L8B/D	AOLUSTA	
Medium 20B/D	PAL16R8B/D	AQ XOULT	
	PAL16R6B/D	PALSOXEA	
	PAL16R4B/D	* I Silver I	
Medium	PAL16L8BP	nisos ing l	
20BP Standard	PAL16R8BP		
	PAL16R6BP	Under Development	
	PAL16R4BP		
	FALIONADE		
Medium 20PA	PAL16P8A	1.03	412 ogval
Programmable	PAL16RP8A	and the second	
Polarity	PAL16RP6A	and the state of t	
Folality	PAL16RP4A	AVOY RVISE JAS	
Large 20	PAL16X4	0.5MR02.1/5	
Arithmetic	PAL16A4		
Large 20RA Asynchronous	PAL16RA8	Under Development	Je vo knidero z

24-Pin and MegaPAL™ Device Families

Valley Data Sciences

Series	Part Number	Rev.		
emmergo 9	PAL12L10	37-0777		
	PAL14L8	1.03		
Small 24	PAL16L6			
Combinatorial	PAL18L4	Serie. Part Number		
	PAL20L2	JASHO! JAH		
	PAL20C1	▼ S.Ne.TOLAR J		
Small 24A	PAL6L16A			
Decoder	PAL8L14A	Under Development		
Decoder	PALOL14A	A STATE OF THE STA		
	PAL20L8A/-2/B			
Medium 24A/	PAL20R8A/-2/B	1.03		
24A-2/B	PAL20R6A/-2/B			
Standard	PAL20R4A/-2/B	SALISOTAS		
	T =	384 3041 20V PAL 181.83V 2 - 418 24-4		
	PAL20L10	SOAJOBA STALIGHBLAND & BOSTADS		
Medium 24X	PAL20X10	208 1 4 PALISHSAVS - 48 2-4		
Exclusive-OR	PAL20X8	Standard PALISHAW SHEET SHEET		
	PAL20X4			
	PAL20L10A	DIGEST AR		
	PAL20L10A PAL20X10A	OCCEPTIAS LIBERAL		
Medium 24XA		Outstand Class		
Exclusive-OR	PAL20X8A	CREWFar JAR		
	PAL20X4A			
	PAL20S10	Medit n PALIGIAGE		
Large 24RS	PAL20RS10	SORT PALIGNOR		
Shared	PAL20RS8	963531 JAS 1 to build		
Product Terms	PAL20RS4	594981/A3_1		
Large 24A Registered XOR	PAL22RX8A	ASSAT LAS ASS multisti		
negistered AOH		ASSESTIAS SIDE DATES		
Large 24/A	PAL32VX10/A	Polar IV PRLIBERES		
Varied XOR	I ALGEVATO/A	ALPROPAR		
Large 24RA	DAL 00DA10	Large 20 PAUISX4		
Asynchronous	PAL20RA10	AA21/39 ob mitral		
ECL				
Combinatorial	PAL10H20P8	ABOY Ayes I		
MegaPAL™	PAL32R16	1.04 + 1.1 Adapter		
Devices	PAL64R32	Under Development		

Varix

1210 E. Campbell Road Richardson, TX 75081 (214) 437-0777 OMNI Programmer

		3.191, jr 3	FS. Name 1
Series	Part Number	Rev.811A9	
	PAL10H8/-2	9.109.149	
	PAL10L8/-2	3.18	
	PAL12H6/-2		
	PAL12L6/-2	PAL6L18A	
Small 20/-2 Combinatorial	PAL14H4/-2	PALBLYA	
Combinatorial	PAL14L4/-2	P.A. 20L. A.A.2/8	
	PAL16H2/-2	PALLORDA-ZIE	
	PAL16L2/-2	PALZORIA 28	
	PAL16C1/-2	BIS AMAROS JAR	
Medium 20/	PAL16L8/A/-2/-4/B-2/-4	6 1083 6	
20A/20A-2/4/	PAL16R8/A/-2/-4/B-2/-4	PA1.20X19	
20B-2/-4	PAL16R6/A/-2/-4/B-2/-4	#XQEJA9	
Standard	PAL16R4/A/-2/-4/B-2/-4	NKSS-LA*	
	PAL16L8B/D	PALZOLIOA	
Medium	PAL16R8B/D	ADDXOS IAN	
20B/D	PAL16R6B/D	ASXCLIA	
	PAL16R4B/D		Fich-evisulex3
Medium	PAL16L8BP		
20BP Standard	PAL16R8BP	Under Development	
	PAL16R6BP	SEP SEA	
	PAL16R4BP	ASSOCIATION OF THE PROPERTY OF	ProBuct Tayns
Medium 20PA	PAL16P8A	3.18	LANG SITTEL
Programmable	PAL16RP8A	POSMETICAL	
Polarity	PAL16RP6A	100000000000000000000000000000000000000	Latge 24A
Polarity	PAL16RP4A	AND AVECTA	
	L DALLOVA		
Large 20	PAL16X4	PALLORIUS	
Arithmetic	PAL16A4		
Large 20RA Asynchronous	PAL16RA8	Under Development	leisol smidmo 3

24-Pin and MegaPAL™ Device Families

Varix

Series	Part Number	Rev.
	PAL12L10	3.18
	PAL14L8	0.10
Small 24	PAL16L6	
Combinatorial	PAL18L4	
	PAL20L2	
	PAL20C1	
Small 24A	DALGLICA	
	PAL6L16A	
Decoder	PAL8L14A	
	PAL20L8A/-2/B	
Medium 24A/	PAL20R8A/-2/B	
24A-2/B	PAL20R6A/-2/B	
Standard	PAL20R4A/-2/B	
	DAI 201 10	
	PAL20L10 PAL20X10	
Medium 24X	PAL20X8	
Exclusive-OR	PAL20X4	
	PAL2UA4	
	PAL20L10A	
Medium 24XA	PAL20X10A	
Exclusive-OR	PAL20X8A	
	PAL20X4A	
	PAL20S10	
Large 24RS	PAL20RS10	
Shared	PAL20RS8	Under Development
Product Terms	PAL20RS4	
	1 THE OTHER	
Large 24A Registered XOR	PAL22RX8A	
Large 24/A Varied XOR	PAL32VX10/A	
Large 24RA Asynchronous	PAL20RA10	3.18
ECL Combinatorial	PAL10H20P8	
MegaPAL™	PAL32R16	
Devices	PAL64R32	Under Development

4-Pin and MagaPALT Device Pamilies

Varix

		Saries
		Linge 246 A Asynchronous Asynchronous
· 121		
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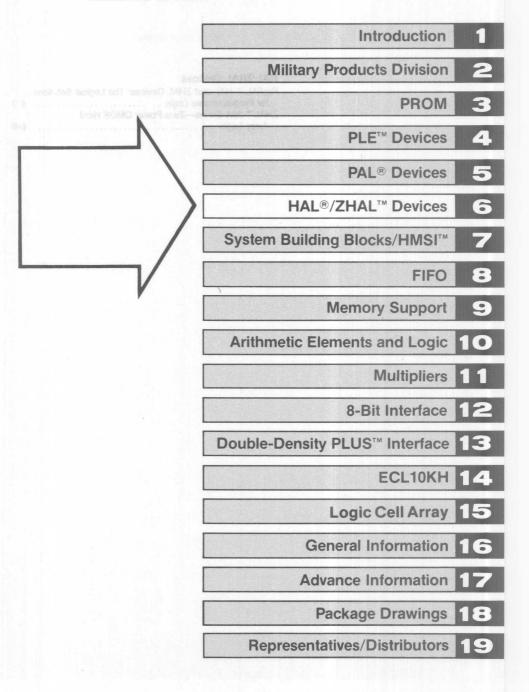


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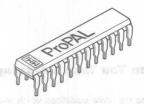
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ProPAL™, HAL®, and ZHAL™ Devices: **The Logical Solutions for Volume Programmable Logic**

So you have discovered the convenience and flexibility of designing with PAL® devices from Monolithic Memories. You have implemented a design using PAL devices, and taken that design into production. Now may be the time to consider ways of reducing the efforts you put into programming, testing, and marking large volumes of PAL devices. Wouldn't it be more convenient if you could be relieved of the duties and costs of volume programming and testing and still reap the benefits afforded by programmable logic?

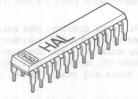
Or perhaps you are considering a semicustom product, but you're a little nervous about going to a gate array. Wouldn't it be preferable if you could find a semicustom product which allows easy, inexpensive prototyping, provides fast prototype turnaround, comes fully tested, can have a custom marking, has low NRE charges, provides design flexibility, and has an assured second source?

Well, Monolithic Memories, the inventor of the PAL device, offers the logical solutions. ProPAL, HAL, and ZHAL devices make the transition from user-programmed devices to customized production-ready devices easy and risk free.



ProPAL Devices

ProPAL (Programmed PAL) devices are simply PAL devices that Monolithic Memories programs and tests for you. You receive a fully functional unit without having to do the programming and testing. But you still have the flexibility to handle design changes easily.



HAL Devices

HAL (Hard Array Logic) devices are to PAL devices as ROMs are to PROMs. Instead of fuses in the logic array, your pattern is implemented using metal links that are masked in during wafer fabrication. So your need to program devices is eliminated. And because the devices have their functionality masked in, Monolithic Memories can provide full functional testing before shipping the product. You can place the devices in your boards with a minimum of handling and the highest level of confidence.

Monolithic Memories offers a HAL device for every PAL device. Any PAL device design you program can be implemented in a HAL version, allowing you to move smoothly into volume production.



ZHAL Devices

Monolithic Memories now provides a third alternative for the programmable logic user: new Zero-Standby-Power CMOS HAL devices.

For the first time there are HAL devices which can implement any pattern from the Series 20 and Series 24 PAL devices with the greatly reduced power consumption only CMOS can offer.

For high complexity designs reaching into the thousands of gates, Zero Power MegaHAL™ devices provide the natural semicustom VLSI alternative to gate arrays. The MegaPAL™ devices provide the flexibility and fast design turn-around you need for prototyping. Once you are ready for production, the CMOS MegaHAL devices provide the same functionality with Zero Power.

All of the ZHAL devices are fully HC/HCT compatible, making them easy to use in TTL and CMOS environments.

Should You Use a PAL, ProPAL, or **HAL Device?**

PAL devices offer the flexibility and convenience needed for prototyping your innovative designs. They provide a means for designing an efficient system by integrating functions and saving you board space. For flexible production, it makes sense to program and test your own PAL devices. This is especially true if you need low volumes per pattern. You always have the option of making last minute design tweaks as you fine tune your system design.

TWX: 910-338-2376





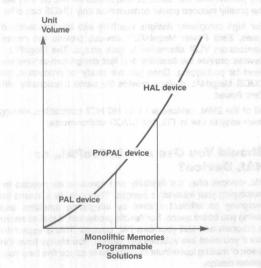
Once your production volumes reach a moderate volume of a few thousand devices per year for each pattern, you may wish to dedicate your production resources to newer designs, instead of programming and testing production volumes. Yet in order to be able to make quick design updates, you might not want to commit to a HAL mask. ProPAL devices provide the ideal solution by eliminating programming and testing needs while retaining enough flexibility to accommodate design changes.

When you feel that your design has stabilized and your volume has ramped up to several thousand devices per year, a HAL device becomes the most cost effective way to purchase our programmable logic. By shifting the burdens to Monolithic Memories, who can handle large volumes easily, you can concentrate your energies on more productive projects.

How Does MMI Do This?

Monolithic Memories takes your proven PAL device design and either arranges to program ProPAL devices in volume, or generates a custom mask for a HAL or ZHAL device. And all without the normal risks inherent in purchasing a semicustom product. Why? Because:

- You can prototype your system and initiate production using standard Monolithic Memories PAL devices. You don't have to worry about making a mistake that could put your design schedule in jeopardy.
- The nominal Non-Recurring Engineering (NRE) charges for ProPAL and HAL devices are far lower than those normally required for a semicustom circuit. And they can even be amortized over your first production quantity.



- You save on the costs of programming devices. This will also shorten your production cycle, since you can plug the devices into the socket with no additional processing.
- All of the devices are tested for full functionality before they leave Monolithic Memories. You save on the costs of testing and generating test programs.
- Monolithic Memories is geared towards providing volumes of high quality devices. No one knows how to test programmable logic as well as Monolithic Memories. Between the thorough, efficient testing and marking capabilities and the option to provide burn-in for extra reliability, you can obtain a higher quality device that if you did the programming and testing yourself.
- MMI can provide custom marking. This saves you the added expense of stripping the mark from standard devices and then remarking them with your own mark.
- HAL devices are secure by design. If you prefer ProPAL devices, they can also be secured for you at the factory.
- ProPAL device lead time is only 1 to 2 weeks longer than that of unprogrammed PAL devices.
- HAL device turn-around time is a mere 6 to 8 weeks or less from acceptance of your design package to receipt of first units.
- If you find yourself with an unexpected demand, you need not turn away business for lack of HAL device stock. You can always use ProPAL devices to make up for any temporary shortfall

How Can You Take Advantage of This?

The following are some guidelines which you can use to help convert your designs to ProPAL, HAL or ZHAL devices.

1. Send in Your Design

You will need to provide your logic equations from either PALASM® PALASM 2 or ABEL™ on magnetic media*.

When Monolithic Memories generates vectors for use in functionally testing your pattern, "seed" vectors are helpful in providing the foundation upon which the final test vectors will be based.

A master PAL device containing your design is needed for Monolithic Memories to verify that the pattern you submitted has been correctly processed. If you cannot provide a Monolithic Memories master PAL device, Monolithic Memories will accept your design inputs and provide ProPAL samples for your approval.

For your convenience, a checklist is included to help you prepare all of the necessary materials to be submitted to Monolithic Memories. This will also help Monolithic Memories process your design, resulting in smoother and faster turn-around. Copies of this form are available from your Sales Representative, or you can simply copy the attached form.

2. MMI Will Verify the Design

Upon receiving your design package, Monolithic Memories will enter your design into their computer and verify that there are no format or syntax problems. A fuse map will be generated, and sample ProPAL devices programmed.

If any questions are encountered at this stage, they will be resolved with you before any further processing takes place.

3. MMI Will Check the Samples

If you have approved immediate production of your devices, Monolithic Memories will make a fuse for fuse comparison between the samples and the master device you provide. If there are no discrepancies, test generation will be started immediately (or upon receipt of your purchase order).

If you prefer to see programmed sample ProPAL devices prior to initiating production, Monolithic Memories can provide them for your approval before proceeding further. Sample approval is also needed when no master devices are provided or when a discrepancy is found during verification.

4. MMI Will Generate Test Vectors

A functional test sequence is generated using TGEN™, a proprietary software package. Any seed vectors you provide will be used to help initiate test generation. TGEN will check for hazards and race conditions, monitor fault coverage and systematically add vectors until test coverage goals are met.

Monolithic Memories has a test quality standard that sets as a minimum goal 90% coverage of all stuck-at faults. Lower coverage patterns can sometimes be processed as HAL devices, or it is possible to handle them as ProPAL devices only, but your approval will be needed. If acceptable coverage cannot be obtained, ways of increasing the testability of the design may have to be considered before Monolithic Memories can process the pattern.

For more detail on exactly how the test coverage is determined, refer to the article "PAL Design Function and Test Vectors" in the Monolithic Memories Programmable Logic Handbook.

When suitable test coverage is obtained, as is normally the case, there is no need for you to be involved with vector generation. If, however, you wish to approve the test vectors before production units are generated, the vectors will be made available to you.

5. MMI Will Generate Production Units

After an acceptable test sequence has been generated, Monolithic Memories will generate the appropriate HAL or ZHAL mask and build the devices. Or, in the case of a ProPAL device, Monolithic Memories will arrange to program and test blank units.

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ABEL is a trademark of Data I/O Corp.

DEC, RSX, VAX, and VMS are registered trademarks of Digital Equipment Corp. IBM PC is a trademark of International Business Machines, Inc.

Having Your Devices Marked

The standard Monolithic Memories mark consists of the device type, the package type, the date code, and the Monolithic Memories logo.

If you wish, you can have the standard marking replaced by a custom marking. The logo and date code are standard, but any other markings can be as you desire. The character and line limitations for the most common packages are in Table 1.

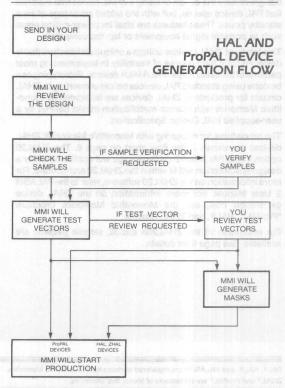
If the package you want is not listed, your local representative can help you determine the guidelines you need.

Whom to Contact

When you are ready to put the power of the Monolithic Memories factory to work for you, just contact your local Monolithic Memories sales representative. And let Monolithic Memories take care of your production programming, testing, and marking needs.

Table 1.

PLASTIC	20 pin (300 mil)	2 lines/13 characters per line
	24 pin (300 mil)	2 lines/17 characters per line
CERDIP	20 pin (300 mil)	2 lines/16 characters per line
	24 pin (300 mil)	2 lines/17 characters per line
PLCC	20 lead	4 lines/11 characters per line
	28 lead	5 lines/12 characters per line



Zero Power CMOS Hard Array Logic ZHAL™ 20A Series

Patent Pending

Features/Benefits

- · Zero standby power
- 25-ns maximum propagation delay
- HC and HCT compatible
- Space saving PLCC available
- Low power alternative for Small and Medium 20-pin PAL® devices, including 16L8/16R8/16R6/16R4

Description

The Zero Power Hard Array Logic (ZHAL) devices are ideal in low-power applications that require high-speed operation. These attributes are achieved through the use of Monolithic Memories' advanced high-speed CMOS process. Now system designers have the option of using a ZHAL device that matches fast PAL device speeds, but with the added advantage of zero standby power. These features are ideal for power-critical areas such as portable digital equipment or lap-top computers.

This family of ZHAL devices utilizes a unique architecture that is designed for a high degree of flexibility in implementing most patterns of the listed 20-pin PAL/HAL® devices. Prototyping can be done using standard PAL devices before converting to ZHAL circuits for production. ZHAL devices are fabricated by Monolithic Memories with custom metallization masks defined by a user-supplied HAL Design Specification.

The procedures for designing with Monolithic Memories' ZHAL devices are shown in the flow chart on page 8. The ZHAL20 option in the PALASM®2 CAD package will confirm whether a design specification will fit within the ZHAL20 architecture. For more information on the ZHAL20 software, refer to the PALASM 2 User Manual. For more information on the ZHAL device generation flow, see the Monolithic Memories brochure "ProPAL™, HAL®, and ZHAL Devices."

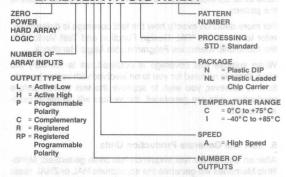
For evaluation of the ZHAL20A circuit, sample patterns are available. See page 6 for details.

Ordering Information

DADT NUMBER	DACKAGE	ARRAY	OUTPUTS		
PART NUMBER	PACKAGE	AGE 10 8 12 6 14 4 16 2 10 8 12 6 14 4 16 2 16 8 16 9 16 9 16 9 16 9 16 9 16 9 16 9	REG		
ZHAL10H8A	ut it it said a sol	10	8		
ZHAL12H6A		91 12 8	6	ett ec e	
ZHAL14H4A		14	4 30	ab au	
ZHAL16H2A		16	2	0000	
ZHAL16C1A	N, NL	16	2	ang u o	
ZHAL10L8A		10	8	gr ille si	
ZHAL12L6A		12	6	qq <u>s</u> —n	
ZHAL14L4A					
ZHAL16L2A		16	2	160 <u>81</u> 0	
ZHAL16L8A		16	8	_	
ZHAL16R8A	Vacifics	16	ens e tir	8	
ZHAL16R6A	N, NL	16	2	6	
ZHAL16R4A		16 9	18 v 40 a v	4	
ZHAL16P8A	non I mag	16	8	(1580).	
ZHAL16RP8A	N, NL	16	ev tros v	8	
ZHAL16RP6A		16	2	6	
ZHAL16RP4A		16	4	4	

ZHAL16L8A I N STD H01234

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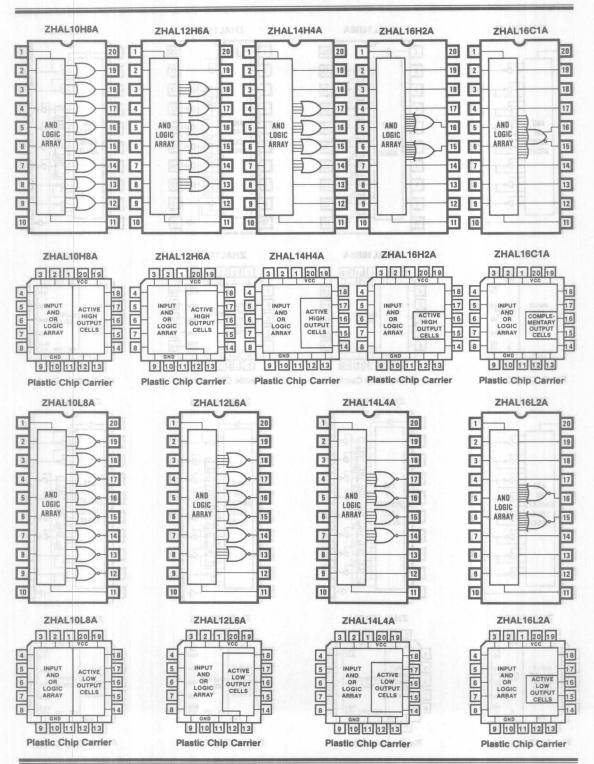


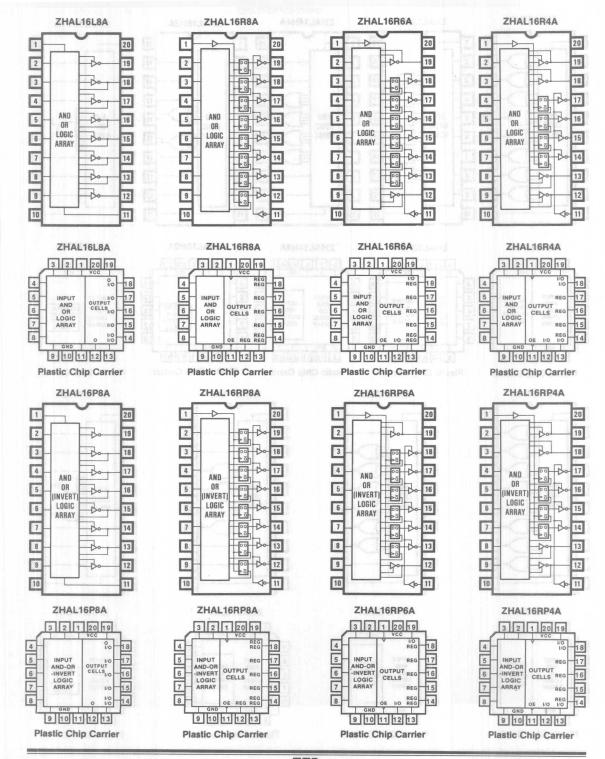
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ZHAL™ and ProPAL™ are trademarks of Monolithic Memories.

2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2374

Monolithic Management Memories





Operating Conditions

SYMBOL	PARAMETER			INDUSTRIAL MIN TYP MAX		MIN	UNIT		
Vcc	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
t _w	Width of clock	and the second second second second	15	10	of the po	15	10	30 tg 10	ns
t _{su}	Setup time from input or feedback to clock	16R4A, 16R6A, 16R8A, 16RP4A, 16RP6A, 16RP8A	20	13		20	13	mus op	ns
th	Hold time	The state of the s	0	-10		0,40	-10	120 1900	ns
TA	Operating free-air temperature		-40	25	85	0	25	75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAI	METER	TES	T CONDITIONS	MIN	TYP	MAX	UNIT		
V _{IL} ¹	Low-level inpu	t voltage	No.		0	3.62.0	0.8	V		
V _{IH} ¹	High-level inpu	ut voltage	J 7889 UQ		2		VCC	V		
IIL	Low-level inpu	t current	V _{CC} = MAX	V _I = GND	1909	T.	-1	μΑ		
IIH High-level input curren		Pin 8 ²	V _{CC} = MAX	V _I = V _{CC}	7	1	10	μΑ		
	input current A	All other pins	VCC - WAX		Take.	1	μΑ			
V _{OL} Low-le	Low-level outp	uit voltage	V _{CC} = MIN	I _{OL} = 8 mA	一学 。	0.1	0.4	V		
	Low-level outp	out voltage	V _{CC} = 5 V	I _{OL} = 1 μA	L		0.05			
Vall	Lich level event veltere		V _{CC} = MIN	I _{OH} = -6 mA	3.763	4.1		V		
VOH	High-level out	High-level output voltage		I _{OH} = -1 μA	4.95			7		
lozL ³	V _{CC} = 5 V		VO = GND	ban s	0	-10	μΑ			
^I OZH ³	Off-state outpu	at current	V _{CC} = MAX		1 3,000	0	10	μΑ		
Standby supply curre		y current ⁴	I _O = 0 mA, V _I = GNI	D or V _{CC}	Ordina .	0	100	μΑ		
lcc	Operating supply current		f = 1 MHz, I _O = 0 mA, V _I = GND or V _{CC}			2	55	mA		

Switching Characteristics Over Operating Conditions

SYMBOL	PARA	AMETER	TEST CONDITIONS (See Test Load)		USTR		COM	MER	CIAL	UNIT	
t _{PD}	16C1A, 10L8A	, 14H4A, 16H2A, , 12L6A, 14L4A 16R6A, 16R4A,	$R_L = 1 K\Omega$ $C_L = 50 pF$		15	25	Notice of the	15	25	ns	
tCLK	Clock to output of 16R4A, 16R6A 16RP4A, 16RP	, 16R8A,			entic aff	10	15	at :080-	10	15	ns
t _{PZX}	Input to output enable	16L8A, 16R4A, 16R6A, 16P8A,		jiye i	12	25	(S) 816:	12	25	ns	
t _{PXZ} 6	Input to output disable	16RP4A, 16RP6A		80	14	25	Suga	14	25	ns	
t _{PXZ} 6 t _{PZX}	Pin 11 to output disable/enable	16R4A, 16R6A, 16R8A, 16RP4A,	and control	asing tile	12	15	B. (v.S. i He m	12	15	ns	
fMAX	Maximum frequency	16RP6A, 16RP8A		28.5	40	om ela orginio	28.5	40	Civ sof	MHz	

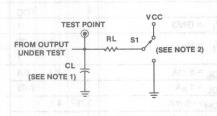
Notes: Apply to electrical and switching characteristics.

- These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test
 these values without suitable equipment.
- 2. Pin 8 (PRELOAD pin). Applies to all devices whether registered or non-registered. 3. JEDEC standard no. 7 for high-speed CMOS devices.
- 4. Disable output pins = VCC or GND. 5. Add 3 mA per additional 1.0 MHz of operation over 1 MHz. 6. CL = 5 pF.

Absolute Maximum Ratings

Supply voltage, VCC	0.5 V to 7 V
DC input voltage, VI	
DC output voltage, VO	-0.5 V to V _{CC} +0.5 V
DC output source/sink current per output pin, IO	±35 mA
DC VCC or ground current, ICC or IGND	±100 mA
Input diode current, I _{IK} :	ASSIST ASSISTANCE -20 mA
V <0	20 mA
VI>VCC	+20 mA
Output diode current, IOK:	
V _O <0	-20 mA
VO>VCC · · · · · · · · · · · · · · · · · ·	
Storage temperature	65° C to 150° C

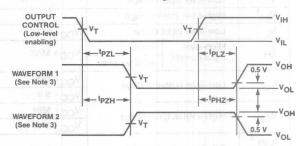
Switching Test Load



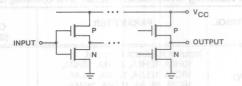
Notes: 1. CL includes probe and jig capacitance.

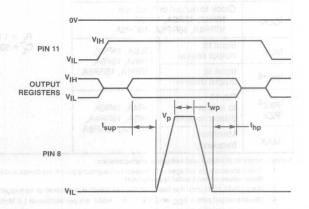
- When measuring tpLZ and tpZL, S1 is tied to VCC.
 When measuring tpHZand tpZH, S1 is tied to ground.
 tpZX is measured with CL = 50 pF. tpXZ is measured with CL = 5 pF.
 When measuring propagation delay times of 3-state outputs, S1 is open, i.e., not connected to VCC or ground.
- Waveform 1 is for an output with internal conditions such that the output is Low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is High except when disabled by the output control.

Enable/Disable Delay



Schematic of Inputs and Outputs





Output Register PRELOAD†

The PRELOAD function allows the register to be loaded from data placed on the output pins. This feature aids functional testing of state sequencer designs by allowing direct setting of output states for improved test coverage. The procedure for PRELOAD is as follows:

- 1. Raise VCC to 4.5 V.
- Disable output registers by setting pin 11 to V_{IH}. Set pin 1 to 0 V.
- 3. Apply VIL/VIH to all registered output pins.
- 4. Pulse pin 8 to Vp (12 V), then back to 0 V.
- 5. Remove VIL/VIH from all registered output pins.
- 6. Lower pin 11 to VIL to enable the output registers.
- 7. Verify for VOI /VOH at all registered output pins.
- Note: Only applies to parts with output registers.

Typical t_{sup} = 50 ns t_{wp} = 100 ns

thp = 50 ns

 $I_{IH} = 30 \,\mu\text{A} \,(\text{Pin 8})$

-

Features/Benefits

- Demonstrates all features of ZHAL20A product
- · 4-bit up/down counter with reset
- · 3-bit shifter
- 25-ns maximum propagation delay
- Zero standby power

Description

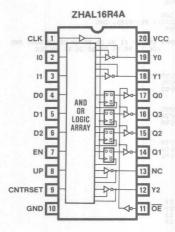
The ZHAL20A Evaluation Pattern is provided as an example of the features and characteristics of the ZHAL20A Series products.

This design consists of two functionally independent patterns: a 4-bit up/down counter and a 3-bit shifter. The 4-bit counter can count up or count down and has reset capability. These features are controlled by two control signals: UP and CNTRSET (Count Reset). When UP is high, the counter counts up. When UP is low, the counter counts down. CNTRSET overrides the count function and resets the counter to all ones, synchronous with the clock

The 3-bit shifter shifts data bits by 0, 1 or 2 positions. The three bits of the shifter are enabled when EN (enable) is high, and are disabled (high-Z) when EN is low.

The PALASM®2 software file and simulation results are shown on the next page. Below are the function tables that summarize the functions of the counter and the shifter.

Logic Symbol



Shifter Function Table

EN	11	10	Y2	Y1	Y0	OPERATION
L	X	X	Z	Z	Z	High-Z
Н	L	L	D2	D1	D0	No operation
Н	L	Н	D0	D2	D1	Shift by one
Н	Н	L	D1	DO	D2	Shift by two

Counter Function Table

ŌĒ	UP	CNTRSET	CLK	Q3-Q0	OPERATION
Н	X	X	Х	Z	High-Z
L	Н	L	1	Q plus 1	Increment
L	L	L	1	Q minus 1	Decrement
L	X	Н	1	High	Reset

H = HIGH voltage level

L = LOW voltage level

X = Don't care

Z = High impedance (off) state

= LOW-to-HIGH clock transition

PALASM Design Specification

Simulation Results

PALASM SIMULATION HISTORY LISTING

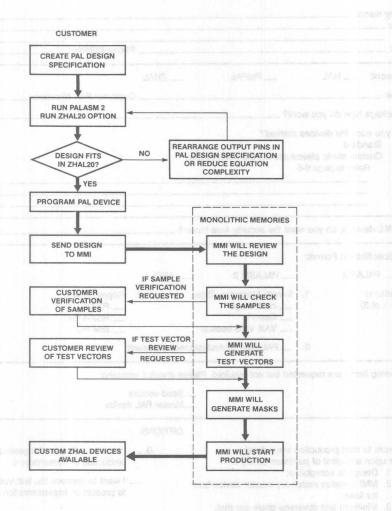
ZZZ Page : :	to the l			
	g g cg cg		cgcgcgcgcg	
CLK	LLLLHLLHLL	HLLHLHLHLH	THTHTHTH	THTHTHTH
IO	XXLLLLLLLH	HHLLLLLLLL	LLLLLLLLL	LLLLLLLL
Il	XXLLLLLLL	LLHHHHHHHH	нинининин	нининини
D0	XXLLLLLLLH	HHLLLLLLL	LLLLLLLLL	LLLLLLLL
D1	XXLLLLLLLL	LLHHHHHHHH	нинининин	нининини
D2	XXLLLLLLLH	HHLLLLLLL	LLLLLLLLL	LLLLLLLL
EN	LLHHHHHHHHH	нинининин	нинининин	нининини
UP	XXXXXXHHHH	нинининин	нинининин	нининини
CNTRSET	XXHHHHLLLL	LLLLLLLLL	LLLLLLLLL	LLLLLLLL
GND	LLLLLLLLL	LLLLLLLLL	LLLLLLLLL	LLLLLLLL
/OE	HHLLLLLLL	LLLLLLLLL	LLLLLLLLL	LLLLLLLL
Y2	XZHHHHHHHL	LLLLLLLLL	LLLLLLLLL	LLLLLLLL
Ql	ZZXXXHHHLL	LLLLHHHHLL	LLHHHHLLLL	HHHHLLLLH
Q2	ZZXXXHHHLL	LLLLLLLHH	HHHHHLLLL	LLLLHHHHH
Q3	ZZXXXHHHLL	LLLLLLLLL	LLLLLHHHH	нининини
00	ZZXXXHHHLL	LHHHLLHHLL	HHLLHHLLHH	LLHHLLHHL
Yl	XZHHHHHHHL	LLHHHHHHHH	нинининин	нининини
YO	ххниннинн	нинининин	нинининин	нининини
VCC	нинининин	нинининин	нинининин	нининини

Simulation File

SIMULATION				
TRACE_ON CLK IO I1 DO D1 D2 EN U	P CNTRSE	T /OE Y2 Q1 Q	2 Q3 Q	0 Y1 Y0
SETF /CLK /OE /EN				
SETF OE EN /I1 /IO /D2 /D1 /DO Y CLOCKF CLK				
CHECK Q3 Q2 Q1 Q0				
SETF /I1 /I0 /D2 /D1 /D0 Y2 Y1 Y CLOCKF CLK	0 /CNTRS	ET UP		
CHECK /Q3 /Q2 /Q1 /Q0				
SETF /I1 IO D2 /D1 D0 /Y2 /Y1 YC CLOCKF CLK				
CHECK /Q3 /Q2 /Q1 Q0				
SETF I1 /I0 /D2 D1 /D0 /Y2 Y1 YC CLOCKF CLK				
CHECK /Q3 /Q2 Q1 /Q0				
SETF OE /CNTRSET UP CLOCKF CLK				
CHECK /Q3 /Q2 Q1 Q0				
SETF OE /CNTRSET UP CLOCKF CLK				
SETF OE /CNTRSET UP				
CHECK /Q3 Q2 /Q1 Q0				
SETF OE /CNTRSET UP CLOCKF CLK				
CHECK /Q3 Q2 Q1 /Q0				
SETF OE /CNTRSET UP CLOCKF CLK				
CHECK /Q3 Q2 Q1 Q0				
SETF OE /CNTRSET UP CLOCKF CLK				
CHECK Q3 /Q2 /Q1 /Q0				
SETF OE /CNTRSET UP CLOCKF CLK				
CHECK Q3 /Q2 /Q1 Q0				
SETF OE /CNTRSET UP CLOCKF CLK				
CHECK Q3 /Q2 Q1 /Q0				
SETF OE /CNTRSET UP CLOCKF CLK				
CHECK Q3 /Q2 Q1 Q0				
SETF OE /CNTRSET UP CLOCKF CLK				
CHECK Q3 Q2 /Q1 /Q0				
SETF OE /CNTRSET UP CLOCKF CLK				
CHECK Q3 Q2 /Q1 Q0				
SETF OE /CNTRSET UP CLOCKF CLK				
CHECK Q3 Q2 Q1 /Q0				
TRACE_OFF				

6

ZHAL 20A Device Generation Flow



HAL/ProPAL CHECKLIST

			第289CF (4CC)
Contact:		PI	none Number:
Do you want: HAL	ProPAL	ZHAL	755
Part Type:		C	ustomer Part Number:
What package type do you wa	nt?		RUN PARASSEZ AUD ZHAR DA DAFRAN
How do you want the devices in — Standard — Custom mark: pleas	marked? e specify the mark below.		TECTORISTO SECURITION OF THE S
			PRODUKT BENICE
For ProPAL devices, do you wa	ant the security fuse blow	n?	
Design Specification Format:	MEDICAL THE INTEREST OF THE PROPERTY OF THE PR	and an arthur and the	PANA OT
PALASM	PALASM 2	ABEL	
Input medium: 1. (Choose 1 of 3)	9-track Magnetic_Tape card image files-11 VAX VMS backup	могазивату стевород2.	Floppy_Disk — RT-11 — RSX-11M — IBM PC
3.	PALASM printout (sign	ned and dated	Wawas raworeus anothar veri so
The following items are reques	ted but not required. Plea	se check if pr	ovided:
	GENERATE WALLS	_Seed vectors _Master PAL o	
		OPTIONS	
A I want to start production (or upon submittal of pur 1. Design is acceptab 2. MMI samples matched for fuse; 3. Minimum test cove (Master device must be)	rchase order) if: le; h my master device fuse rage goals are met.		I want to verify the MMI generated sample devices prior to production implementation. I want to approve the test vectors prior to production implementation.
			mories, and include it in your design package. Date:

	Introduction	1
	Military Products Division	2
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	PAL® Devices	5
	HAL®/ZHAL™ Devices	6
S	ystem Building Blocks/HMSI™	7
	FIFO	8
	Memory Support	9
	Arithmetic Elements and Logic	10
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System Building Blocks/HMSI Selection Guide

FUNCTION	PART NUMBER	
8-Bit Counter	SN54/74LS461A	
8-Bit Up/Down Counter	SN54/74LS469A	
10-Bit Counter	SN54/74LS491A	
16:1 Mux	SN54/74LS450	
Dual 8:1 Mux	SN54/74LS451	sinvesting markets sometimes in a win at A (865.2) and
Quad 4:1 Mux	SN54/74LS453	and ow? All cages afon his was
Increment and Skip Counter	671492	rovida one of four coereticos vinistes de de clock (CK).
2-Digit BCD Counter	671493	The LCAD exercise Joses the Incide
8-Bit Priority Encoder with Register	5/671/0/	ngfeller (QA-QA), T. e. CLEAR o'ns agester to all LOW. The MOLE doe

7

8-Bit Counter SN54/74LS461A

Features/Benefits

- · 8-bit counter for microprogram-counter, DMA-controller and general-purpose counting applications
- 8 bits match byte boundaries
- Bus-structured pinout
- 24-pin SKINNYDIP® saves space
- Three-state outputs drive bus lines
- Low-current PNP inputs reduce loading
- · Expandable in 8-bit increments

Description

The 'LS461A is an 8-bit synchronous counter with parallel load, clear, and hold capability. Two function select inputs (I0, I1) provide one of four operations which occur synchronously on the rising edge of the clock (CK).

The LOAD operation loads the inputs (D7-D0) into the output register (Q7-Q0). The CLEAR operation resets the output register to all LOWs. The HOLD operation holds the previous value regardless of clock transitions. The INCREMENT operation adds one to the output register when the carry-in input is TRUE (CI = LOW), otherwise the operation is a HOLD. The carry-out (CO) is TRUE (CO = LOW) when the output register (Q₇-Q₀) is all HIGHs, otherwise FALSE (CO = HIGH).

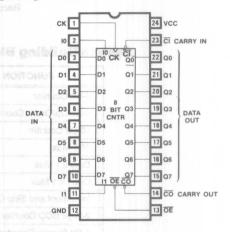
The data output pins are enabled when $\overline{\text{OE}}$ is LOW, and disabled (HI-Z) when OE is HIGH. The output drivers will sink the 24 mA required for many bus interface standards.

Two or more 'LS461A 8-bit counters may be cascaded to provide larger counters. The operation codes were chosen such that when I1 is HIGH, I0 may be used to select between LOAD and INCREMENT as in a program counter (JUMP/INCREMENT).

Ordering Information

PART NUMBER	PACKAGE	TEMPERATUR		
SN54LS461A	JS, W, 28L	Mil		
SN74LS461A	ER NS, JS	Com		

Logic Symbol



Function Table

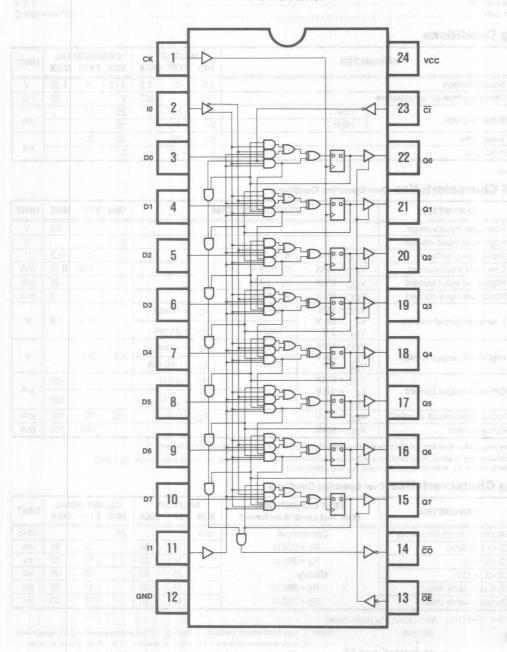
ŌĒ	СК	11	10	CI	D7-D0	Q7-Q0	OPERATION
Н	*	*	*	*	*	Z	HI-Z*
L	t	L	L	X	Х	L	CLEAR
L	1	L	Н	Х	Х	Q	HOLD
L	1	Н	L	Х	D	D	LOAD
L	t	Н	Н	Н	Х	Q	HOLD
L	t	Н	Н	L	X	Q plus 1	INCREMENT

^{*} When OE is HIGH, the three-state outputs are disabled to the high-impedance states; however, sequential operation of the counter is not affected.

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Logic Diagram

8-Bit Counter



Absolute Maximum Ratings

Supply voltage V _{CC}	7 V
Input voltage	5.5 V
Off-state output voltage 5	5.5 V
Storage temperature -65° to +15'	0°C

Operating Conditions

SYMBOL	PARA	METER		ILITARY TYP† I	MAX		MMER(UNIT
Vcc	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
TA	Operating free-air temperature		-55	1	125*	0	PHI	75	°C
		Low	35	15	b. (3)	25	15		
tw	Width of clock	High	20	7	5 1 7 7	15	7		ns
t _{su}	Setup time		40	20		30	20		
th	Hold time	4 10 - 1 - 1	0	-15	1	0	-15		ns

^{*} Case temperature

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS	S	B		MIN	TYP†	MAX	UNIT
VIL**	Low-level input voltage			7					0.8	V
VIH**	High-level input voltage		J-Chall	0 1	Cla Terpo-		2			V
VIC	Input clamp voltage	VCC = MIN	I _I = -18 mA	1	i i	530		-0.8	-1.5	V
IIL	Low-level input current	VCC = MAX	V _I = 0.4 V	1 1	encome of			-0.02	0.25	mA
IH	High-level input current	V _{CC} = MAX	V _I = 2.4 V	LI					25	μΑ
l _l	Maximum input current	VCC = MAX	V _I = 5.5 V	V = 1					1	mA
VOL Low-level output voltage	V _{CC} = MIN V _{II} = 0.8 V	Mil	IOL =	= 12 mA			0.3	0.5	V	
· OL	Low lover output voltage	V _{IH} = 2 V	Com	IOL =	24 mA	1		0.0	0.0	
14	VCC = MIN		Mil	IOH =	IOH = -2 mA		2.4	0.0		
VOH	High-level output voltage	gh-level output voltage VIL = 0.8 V VIH = 2 V		IOH =	I _{OH} = -3.2 mA			2.8		V
lozL	O" - I - I - I - I - I - I - I - I - I -	VCC = MAX		Vo =	0.4 V				-100	Α.
lozh	Off-state output current	V _{IL} = 0.8 V V _{IH} = 2 V		Vo =	2.4 V	10			100	μΑ
los	Output short-circuit current*	V _{CC} = 5.0 V		VO =	0 V		-30	-70	-130	mA
ICC	Supply current	VCC = MAX		L				140	180	mA

^{*} No more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

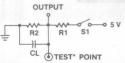
Switching Characteristics Over Operating Conditions

SYMBOL PARAMETER		TEST CONDITIONS (See Test Load/Waveforms)	MILITARY MIN TYP† MAX	COMMERCIAL MIN TYP† MAX	UNIT
fMAX	Maximum clock frequency*	Commercial	16.6	25	MHz
tPD	CI to CO delay	$R_1 = 200 \Omega$	15 35	15 25	ns
tCLK	Clock to Q	R ₂ = 390 Ω	10 25	10 15	ns
tPD	Clock to CO	Military	25 60	25 40	ns
tPZX	Output enable delay	$R_1 = 390 \Omega$	11 25	11 20	ns
tpxz	Output disable delay	$R_2 = 750 \Omega$	10 25	10 20	ns

^{*} f_{MAX} is derived from: 1/MAX [($t_{SU} + t_h$), t_W (Low) + t_W (High), t_{CLK}].

Test Load

* The "Test Point" is driven by the outputs under test, and observed by instrumentation



Notes: 1. tpD is tested with switch S₁ closed, C_L = 50 pF and measured at 1.5 V output level. 2. tpZX is measured at the 1.5 V output level with C_L = 50 pF. S₁ is open for high

impedance to "1" test, and closed for high impedance to "0" test.

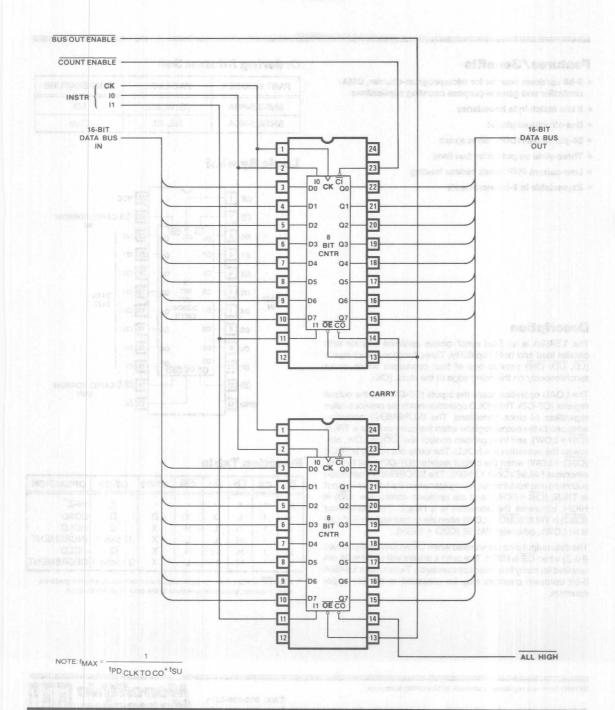
3. tpxz is tested with C_L = 5 pF. S₁ is open for "1" to high impedance test, measured at V_{OH} -0.5 V output level; S₁ is closed for "0" to high impedance test measured at VOL +0.5 V output level.

^{**}V_{IL} and V_{IH} parameters are, in effect, input conditions of D.C. and functional output † All typical values are at V_{CC} = 5 V, T_A = 25°C. tests are not directly tested. V_{IL} is specified at ≤0.8 V and V_{IH} is specified at ≥2.0 V.

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Application

16-Bit Counter



8-Bit Up/Down Counter SN54/74LS469A

Features/Benefits

- · 8-bit up/down counter for microprogram-counter, DMAcontroller and general-purpose counting applications
- · 8 bits match byte boundaries
- Bus-structured pinout
- 24-pin SKINNYDIP® saves space
- Three-state outputs drive bus lines
- Low-current PNP inputs reduce loading
- Expandable in 8-bit increments

Description

The 'LS469A is an 8-bit synchronous up/down counter with parallel load and hold capability. Three function-select inputs (LD, UD, CBI) provide one of four operations which occur synchronously on the rising edge of the clock (CK).

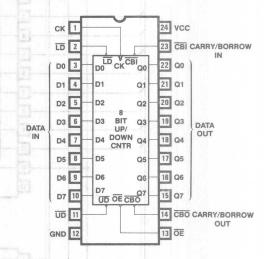
The LOAD operation loads the inputs (D7-D0) into the output register (Q7-Q0). The HOLD operation holds the previous value regardless of clock transitions. The INCREMENT operation adds one to the output register when the carry-in input is TRUE (CBI = LOW), and the up/down control line (UD) is LOW, otherwise the operation is a HOLD. The carry-out (CBO) is TRUE (CBO = LOW) when the output register (Q7-Q0) is all HIGHs, otherwise FALSE (CBO = HIGH). The DECREMENT operation subtracts one from the output register when the borrow-in input is TRUE (CBI = LOW), and the up/down control line (UD) is HIGH, otherwise the operation is a HOLD. The borrow-out (CBO) is TRUE (CBO = LOW) when the output register (Q7-Q0) is all LOWs, otherwise FALSE (CBO = HIGH).

The data output pins are enabled when OE is LOW, and disabled (HI-Z) when OE is HIGH. The output drivers will sink the 24 mA required for many bus-interface standards. Two or more 'LS469A 8-bit up/down counters may be cascaded to provide larger

Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE		
SN54LS469A	JS, W, 28L	Mil		
SN74LS469A	NS, JS	Com		

Logic Symbol



Function Table

OE	СК	LD	ŪD	CBI	D7-D0	Q7-Q0	OPERATION
н	*	*	*.	*	*	Z	HI-Z*
L	1	L	X	X	D	D	LOAD
L	1	Н	L	Н	X	Q	HOLD
L	1	Н	L	L	X	Q plus 1	INCREMENT
L	1	Н	Н	Н	X	Q	HOLD
L	1	Н	Н	L	X	Q minus 1	DECREMEN'

* When OE is HIGH, the three-state outputs are disabled to the high-impedance state; however, sequential operation of the counter is not affected

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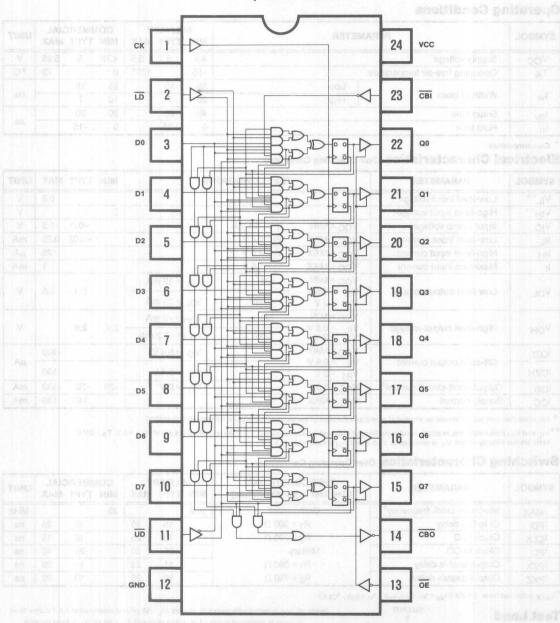
TWX: 910-338-2376

2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2374



Logic Diagram

8-Bit Up/Down Counter



Supply voltage VCC	7.0 V
Input voltage	
Off-state output voltage	5.5 V
Storage temperature65° to +1	150° C

Operating Conditions

SYMBOL	PARAM	METER		TYP†	RY MAX		MMER(UNIT
VCC	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
TA	Operating free-air temperature		-55		125*	0		75	°C
		Low	35	15	No.	25	15		
t _W	Width of clock	High	20	7	1 00	15	7		ns
t _{su}	Setup time		40	20	n:ll [30	20		
th	Hold time	Law and the same of	0	-15		0	-15		ns

^{*} Case temperature

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIO	NS	MIN	TYP†	MAX	UNIT	
VIL**	Low-level input voltage						0.8	V	
VIH**	High-level input voltage	Sec. 1		Station of the state of the sta	2			V	
VIC	Input clamp voltage	VCC = MIN	I _I = -18 mA	The Landerson		-0.8	-1.5	V	
IIL	Low-level input current	V _{CC} = MAX	V _I = 0.4 V	MY 3 185		-0.02	0.25	mA	
IH	High-level input current	VCC = MAX	V _I = 2.4 V				25	μΑ	
11	Maximum input current	VCC = MAX	V _I = 5.5 V				1	mA	
VOL	Low-lovel output voltage	Low-level output voltage VCC = MIN V _{II} = 0.8 V		Mil	IOL = 12 mA		0.3	0.5	V
VOL	Low-level output voltage	V _{IH} = 2 V	Com	I _{OL} = 24 mA		0.5	0.5	V	
Vari	High lavel output voltage	VCC = MIN	Mil	I _{OH} = -2 mA	2.4	2.8			
VOH	High-level output voltage	V _{IL} = 0.8 V V _{IH} = 2 V	Com	I _{OH} = -3.2 mA	2.4	2.0		V	
lozL	0"-1-1	VCC = MAX		V _O = 0.4 V			-100	^	
lozh	Off-state output current	V _{IL} = 0.8 V V _{IH} = 2 V	PHILIT	VO = 2.4 V			100	μΑ	
los	Output short-circuit current*	V _C C = 5.0 V		V _O = 0 V	-30	-70	-130	mA	
Icc	Supply current	V _{CC} = MAX		T. Lawrence F. C.		140	180	mA	

^{*} No more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

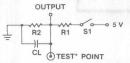
Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load/Waveforms)	MILITARY MIN TYP† M.	AX	COMMERC MIN TYP†		UNIT
fMAX	Maximum clock frequency*	Commercial	16.6		25		MHz
tpD	CI to CO delay	R ₁ = 200 Ω	15	35	15	25	ns
tCLK	Clock to Q	$R_2 = 390 \Omega$	10	25	10	15	ns
tPD	Clock to CO	Military	25	60	25	40	ns
tPZX	Output enable delay	$R_1 = 390 \Omega$	11	25	11	20	ns
tPXZ	Output disable delay	$R_2 = 750 \Omega$	10	25	10	20	ns

 $[*]f_{MAX}$ is derived from: 1/MAX [($t_{SU} + t_h$), t_W (Low) $+t_W$ (High), t_{CLK}].

Test Load

* The "Test Point" is driven by the outputs under test, and observed by instrumentation



Notes: 1. tpD is tested with switch S₁ closed. C_L = 50 pF and measured at 1.5 V output level.

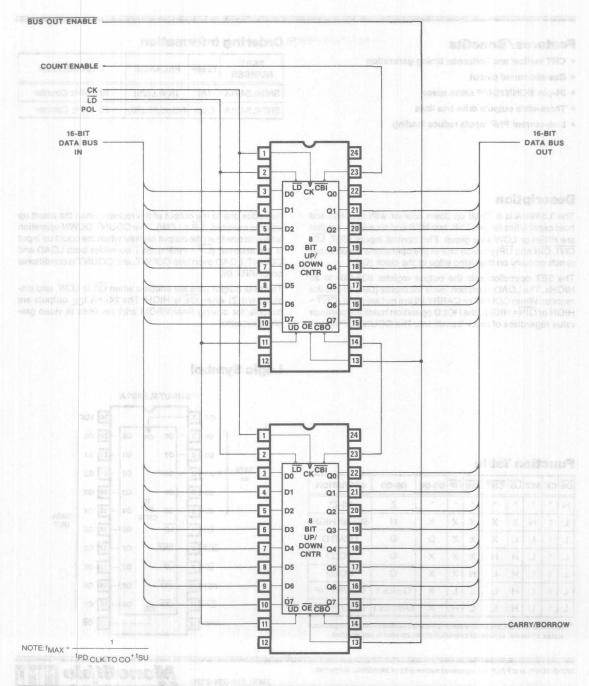
 tpZX is measured at the 1.5 V output level with C_L = 50 pF. S₁ is open for high impedance to "1" test, and closed for high impedance to "0" test.

3. t_{PXZ} is tested with C_L = 5 pF. S_1 is open for "1" to high impedance test, measured at V_{OH} -0.5 V output level; S_1 is closed for "0" to high impedance test measured at V_{OL} +0.5 V output level.

^{**}V_{IL} and V_{IH} parameters are, in effect, input conditions of D.C. and functional output † All typical tests are not directly tested. V_{IL} is specified at ≤0.8 V and V_{IH} is specified at ≥2.0 V.

Application

16-Bit Up/Down Counter



7

10-Bit Counter SN54/74LS491A

16-Pin Up/Down Counter

Features/Benefits

- · CRT vertical and horizontal timing generation
- Bus-structured pinout
- 24-pin SKINNYDIP® saves space
- . Three-state outputs drive bus lines
- . Low-current PNP inputs reduce loading

Ordering Information

PART NUMBER	TEMP	PACKAGE	DESCRIPTION
SN54LS491A	Mil	JS,W,L(28)	10.5 MHz Counter
SN74LS491A	Com	NS,JS,NL(28)	25 MHz Counter

Description

The 'LS491/A is a 10-bit up/down counter with set, load and hold capabilities for two LSB, two MSB and six middle bits that are HIGH or LOW as a group. Five control inputs (SET, LD, CNT, CIN and UP) provide one of five operations which occur synchronously on the rising edge of the clock (CK).

The SET operation sets the output register (Q9–Q0) to all HIGHs. The LOAD operation loads the inputs (D9–D0) into the register. When COUNT or CARRY IN are not asserted (CNT = HIGH or CIN = HIGH), the HOLD operation holds the previous value regardless of clock transitions. The COUNT UP opera-

tion adds one to the output of the register when the count up input is asserted (\overline{UP} = LOW). The COUNT DOWN operation subtracts one from the output register when the count up input is not asserted (\overline{UP} = HIGH). SET overrides both LOAD and COUNT, LOAD overrides COUNT, and COUNT is conditional on CARRY IN.

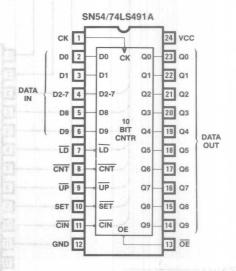
The data output pins are enabled when $\overline{\text{OE}}$ is LOW, and disabled (HI-Z) when $\overline{\text{OE}}$ is HIGH. The 24-mA I_{OL} outputs are suitable for driving RAM/PROM address lines in video graphics systems.

Logic Symbol

Function Table

ŌĒ	СК	SET	LD	CNT	CIN	UP	D9-D0	Q9-Q0	OPERATION
Н	*	*	*	*	*	*	*	Z	HI-Z*
L	1	Н	X	X	X	X	Х	Н	SET all HIGH
L	1	L	L	X	X	X	D	D	LOAD D
L	1	L	Н	Н	X	X	X	Q	HOLD
L	1	L	Н	L	Н	X	X	Q	HOLD
L	1	L	Н	L	L	L	X	Q plus 1	COUNT UP
L	1	L	Н	L	L	Н	X	Q minus 1	COUNT DN

^{*} When OE is HIGH, the three-state outputs are disabled to the high-inpedance states; however, sequential operation of the counter is not affected.



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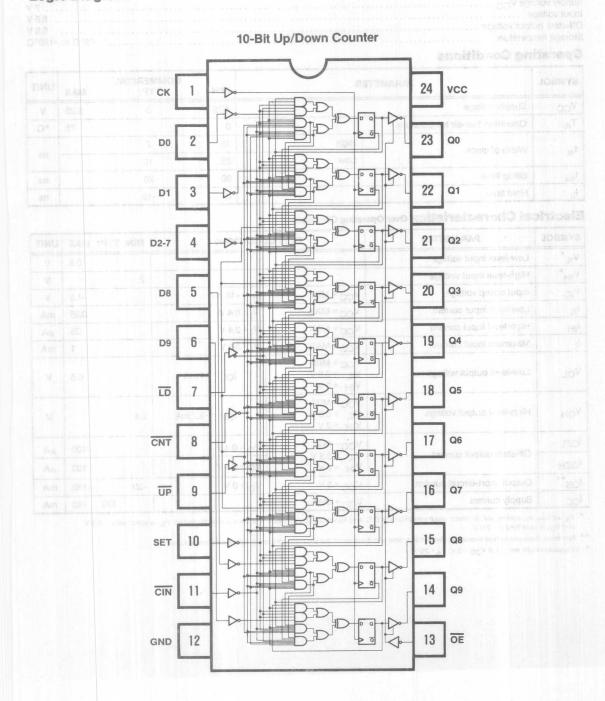
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7

Logic Diagram



Absolute Maximum Ratings

Supply voltage VCC	/
Input voltage	
Off-state output voltage 5.5 \	/
Storage temperature -65° C to +150° C	5

Operating Conditions

SYMBOL	PARAMETER		MIN	COMMERCIAL TYP†	MAX	UNIT
VCC	Supply voltage		4.75	5	5.25	V
TA	Operating free-air temperature		0	err - ay	75	°C
	NAC JAN - 4 - 1 - 1	High	15	\$ 00 7		
t _W	Width of clock	Low	25	15		ns
t _{su}	Setup time		30	20		ns
th	Hold time	THE THE PERSON	0	-15		ns

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TES	T CONDITIONS	MIN	TYP†	MAX	UNIT
V _{IL} *	Low-level input voltage					0.8	V
V _{IH} *	High-level input voltage		Control of the state of the sta	2			V
VIC	Input clamp voltage	V _{CC} = MIN	I ₁ = -18 mA			-1.5	V
I _I L	Low-level input current	V _{CC} = MAX	V _I = 0.4 V			0.25	mA
lін	High-level input current	V _{CC} = MAX	V _I = 2.4 V			25	μΑ
կ	Maximum input current	V _{CC} = MAX	V _I = 5.5 V			1	mA
V _{OL}	Low-level output voltage	V _{CC} = MIN V _{IL} = 0.8 V V _{IH} = 2 V	I _{OL} = 24 mA			0.5	V
V _{OH}	High-level output voltage	V _{CC} = MIN V _{IL} = 0.8 V V _{IH} = 2 V	I _{OH} = -3.2 mA	2.4			V
lozL	11 1 ao 1 11 L	V _{CC} = MAX	V _O = 0.4 V	140		-100	μΑ
lozh	Off-state output current	V _{IL} = 0.8 V V _{IH} = 2 V	V _O = 2.4 V			100	μА
los**	Output short-circuit current	V _{CC} = 5 V	V _O = 0 V	-30		-130	mA
Icc	Supply current	V _{CC} = MAX			120	180	mA

^{*} V_{IL} ad V_{IH} parameters are, in effect, input conditions of D.C. and Functional output tests and are not directly tested. V_{IL} is specified at 2.0 V.

^{**} Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

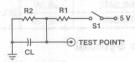
 $[\]dagger$ All typical values are set at V_{CC} = 5 V. T_A = 25° C.

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load)	MILITAR MIN TYP†	William Would	COM MIN 1			UNIT
fMAX	Maximum counting frequency**	Commercial	15.3		25	E		MHz
^t CLK	Clock to Q	$R_1 = 200 \Omega$ $R_2 = 390 \Omega$	10	25		10	15	ns
t _{PZX}	Output enable delay	Mil R ₁ = 390 Ω	11	25	file	11	20	ns
t _{PXZ}	Output disable delay	R ₂ = 750 Ω	10	25	over a first	10	20	ns

^{**} f_{MAX} is derived from: 1/MAX [($t_{SU} + t_h$), t_W (High) + t_W (Low), t_{CLK}].

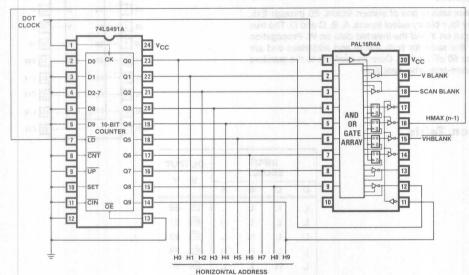
Test Load



- * The "Test Point" is driven by the outputs under test, and observed by instrumentation.
- Notes: 1. tpD is tested with switch S₁ closed. C_L = 50 pF and measured at 1.5 V output level.
 - 2. tp.7x is measured at the 1.5 V output level with C₁ 50 pF. S₁ is open for high impedance to "1" test, and closed for high impedance to "0" test.
 - 3. tpxZ is tested with CL = 5 pF. S₁ is open for "1" to high impedance test, measured at V_{OH} =0.5 V output level: S₁ is closed for "0" to high impedance test measured at V_{OL} ±0.5 V output level.

Application

Video Horizontal Timing and Blanking



Timing Analysis:

Path 1 — Outputs of 74LS491A setting up at PAL16R4A inputs

^tPDCK-Q/74LS491A + ^tSUPAL16R4A = 15 ns + 25 ns = 40 ns

Path 2 — Outputs of PAL16R4A setting up at 74LS491A inputs

tPDCK-Q/PAL16A + tSU74LS491A = 25 ns + 30 ns = 55 ns

Accordingly, the worst-case timing of the two paths is 55-ns, which results in a maximum video dot clock frequency of 18.18 MHz. Strict interpretation of the 60 Hz field rate NTSC Standard suggests that up to 52.1 $\mu \rm sec$ of time is available for active-raster-line duration. In practice however, most CRT monitors

overscan the screen to correct horizontal sweep nonlinearities. As a consequence, the horizontal blanking time is increased, and the active video time decreased, typically to about 40 $\mu \rm sec.$ For the application circuit shown above, over 512 dots (pixels) for one line can be displayed:

$$\frac{40 \ \mu \text{sec per line}}{55 \text{ ns per pixel per line}} = 727 \text{ pixels}$$

Normally, at least a 10-bit counter is required to provide a video timing chain for such resolutions. The 74LS491A combined with a high-speed PAL® (PAL16R4A) is capable of generating a complete set of video timing signals. Note that in the application circuit, the maximum horizontal count [H MAX (n-1)] is decoded one clock early, due to the 1-level pipelining used to obtain circuit speed.

16:1 Mux SN54/74LS450

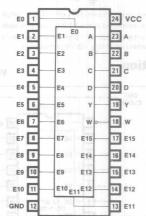
Features/Benefits

- 24-pin SKINNYDIP® saves space
- Similar to SN5/74150
- Low-current PNP inputs reduce loading

Ordering Information

PART NUMBER	PACKA	GE	TEMPERATURE
SN54LS450	JS, W	28L	Mil
SN74LS450	NS, JS	ZOL	Com

Logic Symbol



Description

The 16:1 Mux selects one of sixteen inputs, E0 through E15, specified by four binary select inputs, A, B, C and D. The true data is output on Y and the inverted data on W. Propagation delays are the same for both inputs and addresses and are specified for 50 pF loading. Outputs conform to the standard 8 mA LS totem-pole drive standard.

Function Table

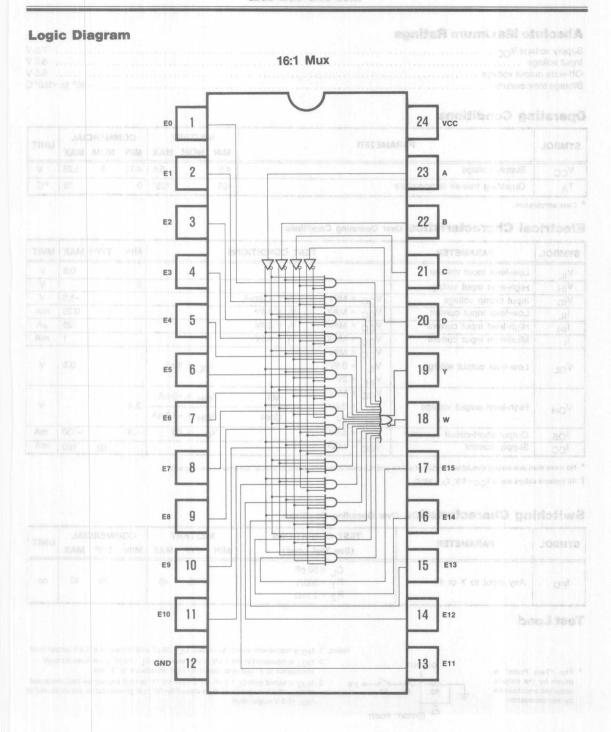
	INI	PUT ECT		OUT	PUT
D	С	В	Α		Ė
L	L	L	L	E0	E0
L	L	L	Н	E1	E1
L	L	Н	L	E2	E2
L	L	Н	Н	E3	E3
L	Н	L	L	E4	E4
L	Н	L	Н	E5	E5
L	Н	Н	L	E6	E6
L	Н	Н	Н	E7	E7
Н	on Em	10 L	L	E8	E8
Н	nil gro	L	Н	E9	E9
Н	L	Н	L	E10	E10
Н	n dE	Н	Н	E11	E11
Н	Н	OL	L	E12	E12
Н	н	L	н	E13	E13
Н	Н	Н	L	E14	E14
Н	Н	Н	Н	E15	E15

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Supply voltage vCC	1.U V
Input voltage	5.5 V
Off-state output voltage	5.5 V
Storage temperature -65° to +	150°C

Operating Conditions

SYMBOL	PARAMETER	, A	MILITARY		COMMERCIAL			
	PARAMETER	MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
TA	Operating free-air temperature	-55	STORAGE LY	125*	0		75	°C

^{*} Case temperature.

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	T	EST CONDITIONS	S	MIN	TYP† MAX	UNIT		
VIL	Low-level input voltage		14 4 4	Land A lead		0.8	V		
VIH	High-level input voltage			Marie III	2	Trial Control	V		
VIC	Input clamp voltage	V _{CC} = MIN	I _I = -18mA			-1.5	V		
I _{IL}	Low-level input current	V _{CC} = MAX	V _I = 0.4V			0.25	mA		
I _{IH}	High-level input current	V _{CC} = MAX	V _I = 2.4V	171 9 19	013	25	μΑ		
1	Maximum input current	V _{CC} = MAX	V _I = 5.5V	percent		1	mA		
VOL	Low-level output voltage	V _{CC} = MIN V _{IL} = 0.8V V _{IH} = 2V		I _{OL} = 8mA		0.5	V		
V	High-level output voltage	$V_{CC} = MIN$ $V_{IL} = 0.8V$	Mil	I _{OH} = -2mA	2.4	24	2.4	2.4	
VOH	riigh-level output voltage	V _{IH} = 2V	Com	$I_{OH} = -3.2 \text{mA}$	2.4		V		
los	Output short-circuit current*	V _{CC} = 5.0V	Marine Territoria	V _O = 0V	-30	-130	mA		
Icc	Supply current	V _{CC} = MAX		Manager 1		60 100	mA		

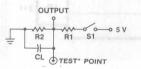
^{*} No more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load)	TYP		MIN	MMER(MAX	UNIT
t _{PD}	Any input to Y or W	$C_L = 50 \text{ pF}$ $R_1 = 560\Omega$ $R_2 = 1.1 \text{k}\Omega$	25	45		25	40	ns

Test Load

* The "Test Point" is driven by the outputs undertest, and observed by instrumentation



Notes: 1. tpD is tested with switch S₁ closed. C_L = 50 pF and measured at 1.5 V output level.

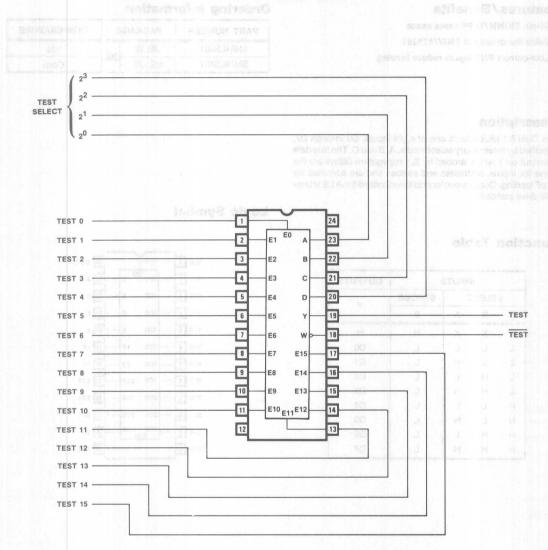
 tpZX is measured at the 1.5 V output level with C_L = 50 pF. S₁ is open for high impedance to "1" test, and closed for high impedance to "0" test.

3. t_{PXZ} is tested with C_L = 5 pF. S_1 is open for "1" to high impedance test, measured at v_{OH} =0.5 V output level; S_1 is closed for "0" to high impedance test measured at v_{OL} +0.5 V output level.

[†] All typicals values are at V_{CC} = 5 V, T_A = 25°C.

Application





7/

Dual 8:1 Mux SN54/74LS451

Features/Benefits

- 24-pin SKINNYDIP® saves space
- Twice the density of SN5/741S151
- . Low-current PNP inputs reduce loading

Ordering Information

PART NUMBER	BER PACKAGE		TEMPERATURE
SN54LS451	JS, W	1001	Mil
SN74LS451	NS, JS	-28L	Com

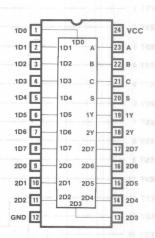
Description

The Dual 8:1 Mux selects one of eight inputs, D0 through D7, specified by three binary select inputs, A, B and C. The true data is output on Y when strobed by S. Propagation delays are the same for inputs, addresses and strobes and are specified for 50 pF loading. Outputs conform to the standard 8 mA LS totempole drive standard.

Logic Symbol

Function Table

	- 1	OUTPUTS		
SELECT		STROBE	V	
C	B A S		· ·	
X	X	X	Н	Н
L	L	L	L	D0
L	L	Н	L	D1
L	Н	L	L	D2
L	Н	Н	L	D3
Н	L	L	L	D4
Н	L	Н	L	D5
Н	H	L	L	D6
Н	Н	Н	L	D7



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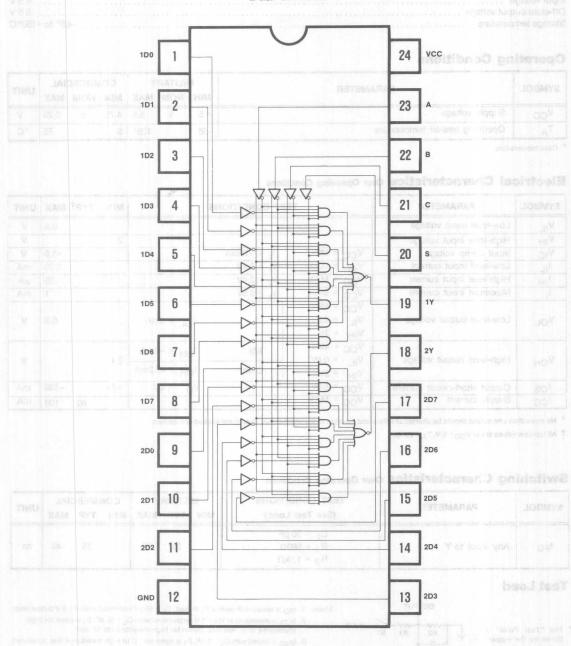
TWX: 910-338-2376

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Logic Diagram

Dual 8:1 Mux



Supply voltage V _{CC}	7.0 V
Input voltage	
Off-state output voltage	5.5 V
Storage temperature -65° t	o +150°C

Operating Conditions

SYMBOL	PARAMETER		MILITAR	Y	co	MMERC	CIAL	
SYMBOL	PANAMETER	MIN	NOM	MAX	MIN	NOM	MAX	UNIT
VCC	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
TA	Operating free-air temperature	-55		125*	0		75	°C

^{*} Case temperature.

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TE	ST CONDITIONS			MIN	TYP	MAX	UNIT
VIL	Low-level input voltage			Paren I	P .			0.8	V
VIH	High-level input voltage			1000		2			V
VIC	Input clamp voltage	V _{CC} = MIN	I _I = -18mA	The G	edt			-1.5	V
IL	Low-level input current	V _{CC} = MAX	$V_1 = 0.4V$	L	1			0.25	mA
1н	High-level input current	V _{CC} = MAX	$V_1 = 2.4V$)			25	μΑ
1	Maximum input current	V _{CC} = MAX	V _I = 5.5V					1	mA
VOL	Low-level output voltage	V _{CC} = MIN V _{IL} = 0.8V V _{IH} = 2V		I _{OL} = 8	BmA			0.5	V
V _{OH}	High-level output voltage	$V_{CC} = MIN$ $V_{IL} = 0.8V$	Mil	I _{OH} = -	-2mA	2.4			V
*OH	riigiriovoi oatput voitage	V _{IH} = 2V	Com	IOH = -	3.2mA	2.4			
los	Output short-circuit current*	V _{CC} = 5.0V		V _O = (V	-30	M	-130	mA
lcc	Supply current	V _{CC} = MAX		18 8	101		60	100	mA

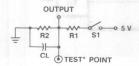
^{*} No more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS	N	ILITA	RY	COI	MMER	CIAL	UNIT
STWIDOL	PANAMETER	(See Test Load)	MIN	TYP	MAX	MIN	TYP	MAX	OIVII
	parameter [1]	C ₁ = 50 pF	F 1 1 1	Parties 1					
tpD	Any input to Y	$R_1 = 560\Omega$		25	45		25	40	ns
		$R_2 = 1.1k\Omega$							

Test Load

* The "Test Point" is driven by the outputs under test, and observed by instrumentation

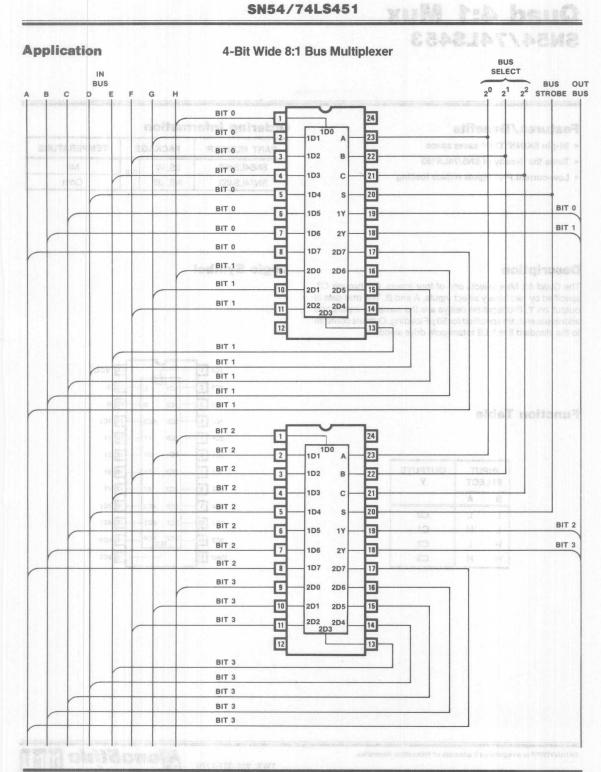


Notes: 1. t_{PD} is tested with switch S_1 closed, C_L = 50 pF and measured at 1.5 V output level.

 tpZX is measured at the 1.5 V output level with C_L = 50 pF. S₁ is open for high impedance to "1" test, and closed for high impedance to "0" test.

3. t_{PXZ} is tested with C_L = 5 pF. S_1 is open for "1" to high impedance test, measured at V_{OH} =0.5 V output level: S_1 is closed for "0" to high impedance test measured at V_{OL} +0.5 V output level.

[†] All typicals values are at V_{CC} = 5 V, T_A = 25°C.



Quad 4:1 Mux SN54/74LS453

Features/Benefits

- 24-pin SKINNYDIP® saves space
- Twice the density of SN5/74LS153
- . Low-current PNP inputs reduce loading

Ordering Information

PART NUMBER	PACKA	GE	TEMPERATURE
SN54LS453	JS, W	28L	Mil
SN74LS453	NS, JS	- ZOL	Com

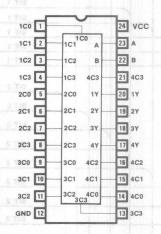
Description

The Quad 4:1 Mux selects one of four inputs, C0 through C3, specified by two binary select inputs, A and B. The true data is output on Y. Propagation delays are the same for inputs and addresses and are specified for 50 pF loading. Outputs conform to the standard 8 mA LS totem-pole drive standard.

Logic Symbol

Function Table

INPUT SELECT		OUTPUTS Y
В	Α	
L	L	CO
L	Н	C1
Н	L	C2
Н	Н	C3



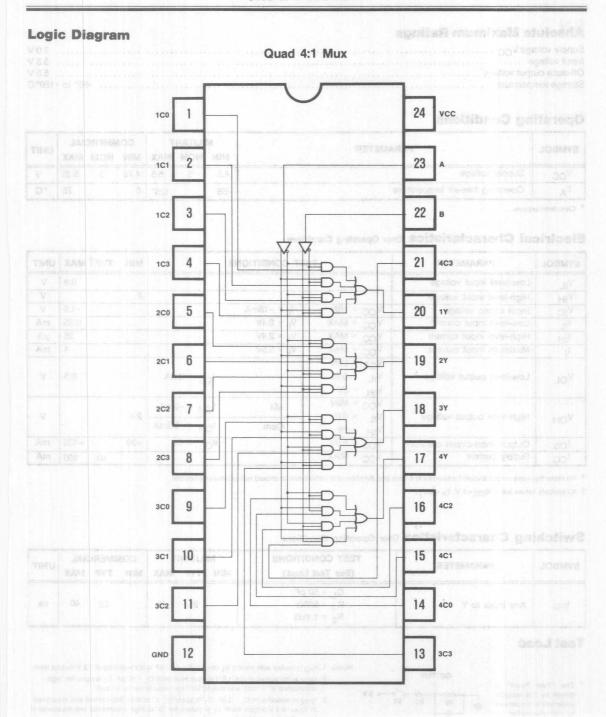
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7-24

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Supply voltage V _{CC}	7.0 V
Input voltage	5.5 V
Off-state output voltage	5.5 V
Storage temperature -65° to +	150°C

Logic Diagram

Operating Conditions

SYMBOL	PARAMETER	MIN	MILITAR MIN NOM				IMERCIAL NOM MAX	
Vcc	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
TA	Operating free-air temperature	-55		125*	0		75	°C

^{*} Case temperature.

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	-CI	EST CONDITIONS	Total A	MIN	TYP† MAX	UNIT
VIL	Low-level input voltage	I LE-OE		function of		0.8	V
VIH	High-level input voltage	THE PLANT		School dec	2		V
VIC	Input clamp voltage	VCC = MIN	I _I = -18mA	-		-1.5	V
I _{IL}	Low-level input current	V _{CC} = MAX	V _I = 0.4V	Later Committee		0.25	mA
1 _{IH}	High-level input current	V _{CC} = MAX	V _I = 2.4V	9		25	μΑ
4	Maximum input current	V _{CC} = MAX	V _I = 5.5V			1	mA
VOL	Low-level output voltage	V _{CC} = MIN V _{IL} = 0.8V V _{IH} = 2V		I _{OL} = 8mA		0.5	V
V _{OH}	High-level output voltage	V _{CC} = MIN V _{IL} = 0.8V	Mil	I _{OH} = -2mA	2.4		V
VOH	riigiriovor odipat voltage	V _{IH} = 2V	Com	$I_{OH} = -3.2 \text{mA}$			
los	Output short-circuit current*	V _{CC} = 5.0V		V _O = 0V	-30	-130	mA
lcc	Supply current	V _{CC} = MAX		L. 3 Jeas	1111	60 100	mA

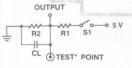
^{*} No more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load)	MILITARY MIN TYP MAX	COMMERCIAL MIN TYP MAX	UNIT
t _{PD}	Any input to Y	C _L = 50 pF R ₁ = 560Ω	25 45	25 40	ns
10	Topos Charge.	$R_2 = 1.1k\Omega$	Secretor of N		

Test Load

* The "Test Point" is driven by the outputs under test, and observed by instrumentation

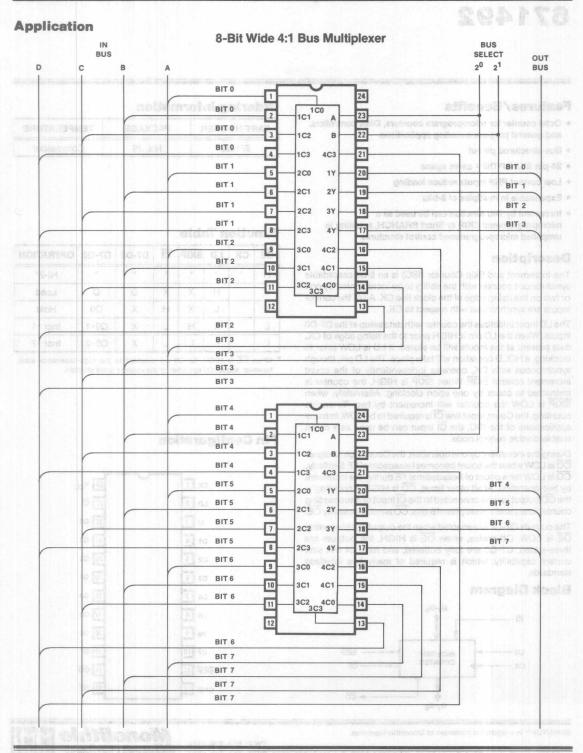


Notes: 1. tpD is tested with switch S₁ closed, C_L = 50 pF and measured at 1.5 V output level.

 1pZX is measured at the 1.5 V output level with C_L = 50 pF. S₁ is open for high impedance to "1" test, and closed for high impedance to "0" test.

3. tpxz is tested with C_L - 5 pF. S₁ is open for "1" to high impedance test, measured at V_{OH} -0.5 V output level: S₁ is closed for "0" to high impedance test measured at V_{OL} +0.5 V output level.

[†] All typicals values are at V_{CC} = 5 V, T_A = 25°C.



- · Octal counter for microprogram counters, DMA controllers, and general purpose counting applications
- Bus-structured pinout
- 24-pin SKINNYDIP® saves space
- Low current PNP inputs reduce loading
- · Expandable in multiples of 8-bits
- · Increment by two function can be used as a microprogrammed SKIP or Short BRANCH, resulting in simplified microprogrammed control structures

Description

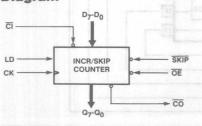
The Increment and Skip Counter (ISC) is an 8-bit cascadable synchronous counter with the ability to be incremented by one or two on the rising edge of the clock line CK. All of the control inputs are synchronous with respect to CK.

The LD input initializes the counter with data setup at the D7-D0 inputs. When the LD pin is HIGH prior to the rising edge of CK, data present at the inputs will be stored. If LD is LOW prior to clocking, a HOLD operation will take place. The LD pin, though synchronous with CK, operates independently of the count increment control SKIP. When SKIP is HIGH, the counter is instructed to count by one upon clocking. Alternately, when SKIP is LOW the counter will increment by two. To enable counting, the Count Input line CI is required to be LOW. In many applications of the ISC, the CI input can be used as a count enable/disable control node.

During the increment by one operation, the Count Output signal CO is LOW when the count becomes hexadecimal FF. Similarly, CO is LOW for a count of hexadecimal FE during the increment by two operation. At all other times, CO is HIGH. Accordingly, the CO output can be connected to the CI input of a succeeding counter to expand in multiples of 8-bits. CO is not affected by OE.

The outputs Q7-Q0 are enabled when the output enable control OE is LOW. Otherwise, when OE is HIGH, the outputs are three-stated. Q7-Q0 are fully buffered, and have 24 mA sink current capability, which is required of many bus interface standards.

Block Diagram



Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
671492	NS, JS	Commercial

Function Table

OE	СК	LD	SKIP	CI	D7-D0	Q7-Q0	OPERATION
Н	*	*	*	*		*	HI-Z*
L		Н	X	X	D	D	Load
L		L	X	Н	X	Q0	Hold
L	8	TIL.	Н	L	X	Q0+1	Incr +1
L		L	L	L	X	Q0+2	Incr +2

When OE is HIGH, Q7-Q0 are disabled to the high-impedance state; however, sequential operation of the counter is not affected.

Pin Configuration



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TWX: 910-338-2376



Supply voltage VCC	/ V
Input voltage	5.5 V
Off-state output voltage	5.5 V
Storage temperature ——6	55°C to +150°C

Operating Conditions

SYMBOL	PARAMETE	R	MIN	COMMERCIAL TYP	MAX	UNIT
V _{CC}	Supply voltage	AND DESCRIPTION OF THE PARTY STATES OF THE	4.75	5	5.25	V
TA	Operating free air temperature	0		75	°C	
		Low	35	hso.lindi	branh	rare 18
r _W	Clock width	High	25			ns
t _{su}	Setup time	50			ns	
th	Hold time	0	-15		ns	

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CO	ONDITIONS	MIN	COMMERCIAL TYP†	MAX	UNIT
V _{IL} *	Low-level input voltage					0.8	V
V _{IH} *	High-level input voltage	Jissini tur	Upp V d.f te basi esset t	2	D. Belletin yê rîch veri w t	attal chash	V
VIC	Input clamp voltage	V _{CC} = MIN	I _I = -18 mA	O Was Sta	s ed at the 1,5 V cutout le	-1.5	V
IIL	Low-level input current	V _{CC} = MAX	V _I = 0.4 V	10.10	rahtugue V 2.0+ 10 V r. m	-0.25	mA
^I IH	High-level input current	V _{CC} = MAX	V _I = 2.4 V			25	μА
l _l	Maximum input current	V _{CC} = MAX	V _I = 5.5 V			1	mA
V _{OL}	Low-level output voltage	V _{CC} = MIN V _{IL} = 0.8 V V _{IH} = 2 V	I _{OL} = 24 mA			0.5	V
V _{OH}	High-level output voltage	V _{CC} = MIN V _{IL} = 0.8 V V _{IH} = 2 V	I _{OH} = -3.2 mA	2.4			V
lozL	Off state output ourrant	VCC = MAX	V _O = 0.4 V			-100	_
lozh	Off-state output current	V _{IL} = 0.8 V V _{IH} = 2 V	V _O = 2.4 V			100	μΑ
los**	Output short-circuit current**	V _{CC} = 5.0 V	V _O = 0 V	-30		-130	mA
Icc	Supply current	V _{CC} = MAX			120	180	mA

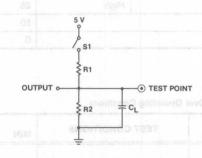
^{*} V_{IL} and V_{IH} are input conditions of output tests and are not, themselves, directly tested. As conditions of tests, $V_{IL} \le 0.8$ V and $V_{IH} \ge 2.0$ V. ** Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

[†] Typicals at V_{CC} = 5 V, T_A = 25° C.

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS (See test load)	MIN	COMMERCIAL	MAX	UNIT
fMAX	Maximum clock frequency		12.5		deraperati	MHz
t _{PD3}	CI to CO delay	Commercial		35	50	ns
t _{PD1}	Clock to Q	C _L = 50 pF		20	30	ns
t _{PD2}	Clock to CO	$R_1 = 200 \Omega$ $R_2 = 390 \Omega$		55	80	ns
t _{PZX}	Output enable delay	The state of the s	PARAMET	35	45	ns
t _{PXZ}	Output disable delay			35	45	ns

Standard Test Load

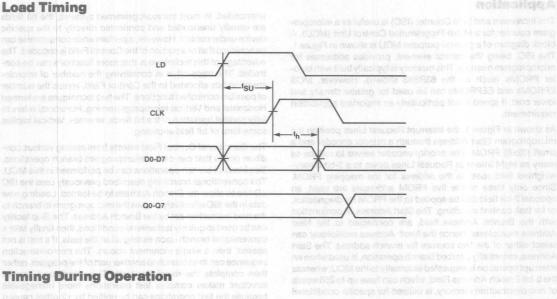


Notes: 1. tpD is tested with switch S₁ closed. C_L = 50 pF and measured at 1.5 V output level.

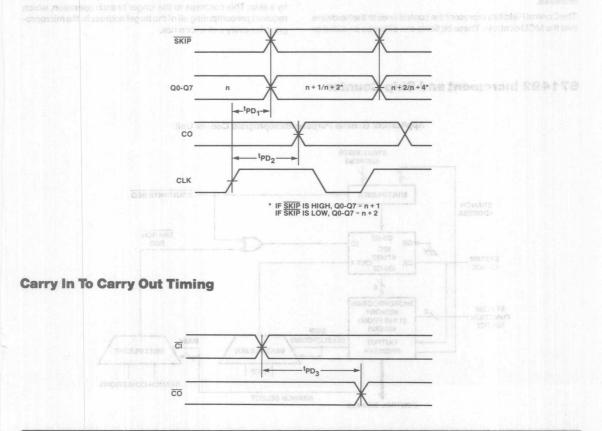
2. tpzx is measured at the 1.5 V output level with CL = 50 pF, S1 is open for high impedance to "1" test, and closed for high impedance to "0" test.

tpXZ is tested with C_L = 5 pF. S₁ is open for "1" to high impedance test, measured at V_{OH} -0.5 V output level; S₁ is closed for "0" to high impedance test measured at V_{OH} +0.5 V output level.









Application

The Increment and Skip Counter (ISC) is useful as a microprogram counter for a Micro-Programmed Control Unit (MCU). A block diagram of a general-purpose MCU is shown in Figure 1. The ISC, being the central element, provides addresses for microprogram memory. This memory is typically built with bipolar PROMs (such as the 63RS88 shown). However, MOS EPROMs and EEPROMs can be used for greater density and lower cost, if speed is not particularly an important application requirement.

As shown in Figure 1, the Interrupt Request Lines position the microprogram Start Address through a priority encoder and a small (32x8) PROM. The priority encoder serves to reduce as many as eight Interrupt Request Lines down to a 3-bit binaryweighted field used as the address for the mapping PROM. Since only three of the five PROM addresses are used, an optional 2-bit field can be applied to the PROM for diagnostics, or for task context switching. The Start Address, in conjunction with the Branch Address field, are connected to the Next Address multiplexer. Hence the Next Address multiplexer can select either of the two sources for branch address. The Start Address, essentially a forced branch operation, is used when an interrupt operation is requested externally to the MCU; whereas the 8-bit Branch Address Field, which can have up to 256 words of microinstruction memory, is utilized for specific conditional branches

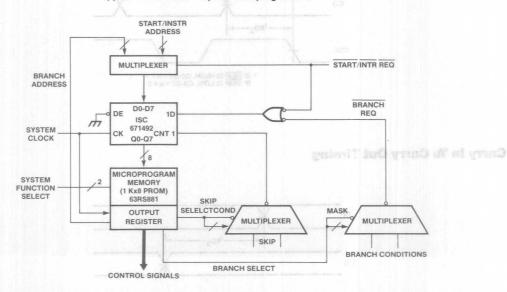
The Control Field bits represent the control lines to the hardware that the MCU controls. These bit fields can either be encoded or

unencoded. In most microprogrammed systems, the bit fields are usually unencoded and connected directly to the specific device under control. However, a performance compromise can be achieved if all or a portion of the Control Field is encoded. The advantage of this technique is that more functions can be controlled. The trade-off is in conserving the number of microinstruction bits allocated to the Control Field, versus the number of possible controlled functions. The two techniques are termed Horizontal and Vertical microprogramming. Horizontal refers to fully parallel operation of the bit fields; whereas, Vertical implies some form of bit field encoding.

The Conditional Control Field selects from among various condition codes that can cause microprogram branch operations. Two kinds of branch operations can be performed in this MCU. The conventional branching described previously uses the ISC LD line to allow the Branch Address to be loaded. Loading new data in the ISC effectively causes the microprogram to branch to the next instruction set by the Branch Address. The Skip facility can be used to quickly test several conditions, then finally take a conventional branch upon exiting all of the tests. If a test is not passed, then a single increment occurs. The microinstruction sequence can then branch to another part of the program, rather than complete the remaining tests. This conditional control structure makes complex test operations more manageable because the test operations can be unified by +2 offset caused by a skip. This contrasts to the longer branch operation, which required precomputing all of the target address in the microprogram for every exit a loop has.

671492 Increment and Skip Counter

Application: General Purpose Microprogram Control Unit



7

2-Digit BCD Counter 671493

Features/Benefits

- Drive numeric displays
- Expansion in 2-digit increments
- 24-pin SKINNYDIP® saves space
- · Bus structured pinout
- . Low current PNP inputs reduce loading
- . Three-state output drive bus lines

Description

The 2-digit BCD (Binary Coded Decimal) Counter is a synchronous counter with complementary count enables (CE1, CE2), parallel load (LD), and carry out (CO). Three control inputs (LD, CE1, CE2) provide one of three operations which occur synchronously on the rising edge of the clock (CK).

The load operation loads the inputs (D1 and D2) into the output register (Q1 and Q2) when load is LOW. Note that the load line overrides the increment.

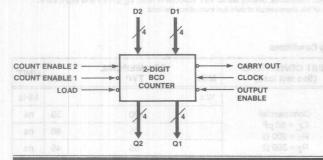
When $\overline{\text{LD}}$ is not active, the counter will increment in a Binary-Coded-Decimal sequence if both count enables are asserted $\overline{(\text{CE1} = \text{L and CE2} = \text{H})}$, otherwise it holds.

Two or more BCD Counters can be cascaded to implement larger BCD counters by connecting carry out (\overline{CO}) of the first stage to count enable $(\overline{CE1})$ of the second stage. This signal is not affected by \overline{OE} .

Parallel loading allows programmability of the BCD Counter and numeric indicator.

This BCD Counter is ideal in an industrial control application where an event counter is needed to drive numeric displays. The device can receive one count enable in the form of strobes from a motor or other device. The second count enable can receive the period signal. With connections in this manner, the counter counts events during a period. The device will provide two active high BCD outputs (Q1 and Q2) to drive two numeric indicators, which feature an on-board decoder/driver.

Block Diagram



Ordering Information

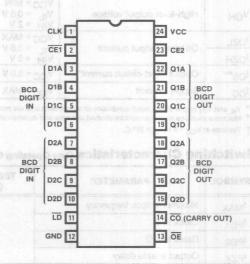
PART NUMBER	PACKAGE	TEMPERATURE
671493	NS, JS	Com

Function Table

ŌĒ	СК	LD	CE1	CE2	D1A-D1D/ D2A-D2D	Q1A-Q1D/ Q2A-Q2D	OPERATION
Н	(*)	01 * ()	0 10	0 *0:	placinal:	Z	HI-Z*
L	1	L	X	X	D	D	Load
L	1	Н	Н	X	X	Q	Hold (CE1=H)
L	1	Н	X	L	X	Q	Hold (CE2=L)
L	1	Н	L	Н	X	Q plus 1	Increment

^{*} When OE is HIGH, Q1 and Q2 are disabled to the high-impedance state; however, sequential operation of the counter is not affected.

Pin Configuration



SKINNYDIP® is a registered trademark of Monolithic Memories.

TWX: 910-338-2376

Monolithic Memories



Supply voltage VCC	7 V
Input voltage	5.5 V
Off-state output voltage	5.5 V
Storage temperature	65°C to +150°C

Operating Conditions

SYMBOL	BOARDAY PARAMETER	MIN	COMMERCIAL MAX	UNIT	
V _{CC}	Supply voltage	4.75	5.25	V	
TA	Operating free air temperature	0	Aconia bene 75 d	°C	
	Olevelywideh	Low	35	sument PNP inputs reduce lands	
t _w	Clock width	High	25	estate output drive Lus line i	ns
t _{su}	Setup time	Punct	50	noifair	ns
th	Hold time	-ordany	0 0	aning t-15 ₀ 0 visale d08 lipi	ns

Electrical Characteristics Over Operating Conditions we recool during enough to end shiving (\$30, 130

SYMBOL	PARAMETER	PARAMETER TEST CONDITIONS		PAMETER TEST CONDITIONS		COMMERCIAL MIN TYP† MAX	UNIT
V _{IL} *	V _{IL} * Low-level input voltage			3.0 ₉ increment.	V		
V _{IH} *	High-level input voltage	THIT	in a Binary-	is not active, the counter will increme!	TINV		
VIC	Input clamp voltage	V _{CC} = MIN	I _I = -18 mA	esidena siudo ritod il soneupae larriga-	٧		
I _I L	Low-level input current	V _{CC} = MAX	V _I = 0.4 V	-0.25	mA		
lн	High-level input current	V _{CC} = MAX	V _I = 2.4 V	O) tuo yner paitosaago yd metnuoc 25	Proc.		
I ₁	Maximum input current	V _{CC} = MAX	V ₁ = 5.5 V	ount enable (CES) of the second siego,	mA		
V _{OL}	Low-level output voltage	V _{CC} = MIN V _{IL} = 0.8 V V _{IH} = 2 V	I _{OL} = 24 mA	2.0 ling allows programme litting of the condicators.	Paryle I		
Vон	High-level output voltage	V _{CC} = MIN V _{IL} = 0.8 V V _{IH} = 2 V	I _{OH} = -3.2 mA	Counter is idea; in an industrial contra event counter a headed to drive but 2.2 in receive one; ount enalt. In the form of			
lozL	Off state suitant surrent	VCC = MAX	V _O = 0.4 V	100 mer device. The securic count enable			
lozh	Off-state output current	V _{IL} = 0.8 V V _{IH} = 2 V	V _O = 2.4 V	one during a period, The device will provi	μΑ		
los**	Output short-circuit current**	V _{CC} = 5.0 V	V _O = 0 V	3_30 own sync or (NO end 10) and 130	mA		
Icc .	Supply current	V _{CC} = MAX		120 180	mA		

^{*} V_{IL} and V_{IH} are, in effect, input conditions of output tests and are not, themselves, directly tested. As conditions of tests, V_{IL} ≤ 0.8 V and V_{IH} ≥ 2.0 V.
** Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	[E] 060	TEST CONDITIONS (See test load)	MIN	COMMERCIAL	MAX	UNIT
fMAX	Maximum clock frequency	The section of	218AH3	12.5		URUL	MHz
t _{PD1}	Clock to Q	TATE OF	Commercial		20	30	ns
t _{PD2}	Clock to CO	Tri one	C _L = 50 pF R ₁ = 200 Ω		55	80	ns
^t PZX	Output enable delay		$R_2 = 390 \Omega$		35	45	ns
tPXZ	Output disable delay	20.00E-0.00		egan vegen	35	45	ns

[†] Typicals at V_{CC} = 5 V, T_A = 25°C.

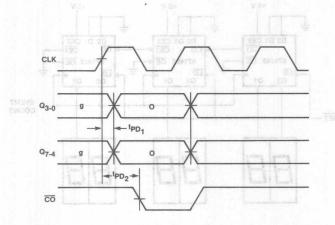
Standard Test Load

Counters. The 2-big 1 BCD Counters control the deplay for the explain BCD Counters count the deplay for the pairs of LEC displays. The 2-big 8-big 8-b

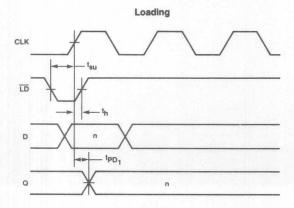
Notes: 1. t_{PD} is tested with switch S_1 closed. C_L = 50 pF and measured at 1.5 V output level.

- 2. tpZX is measured at the 1.5 V output level with CL = 50 pF. S₁ is open for high impedance to "1" test, and closed for high impedance to "0" test.
- 3. tpXZ is tested with C_L = 5 pF. S₁ is open for "1" to high impedance test, measured at V_{OH} -0.5 V output level; S₁ is closed for "0" to high impedance test measured at V_{OL} +0.5 V output level.

Output Timing



Input Timing



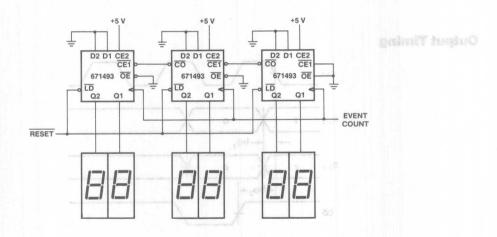
7

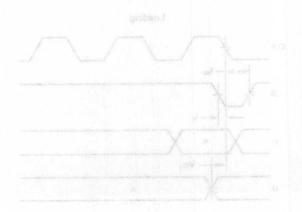
The Event Counter can be implemented using the 2-Digit BCD Counters. The 2-Digit BCD Counters control the display for three pairs of LED displays. The 2-Digit BCD Counters count the events.

The displays are controlled by the output enable. These counters display the count in 10s, 100s and 1000s respectively. These simply count the occurrence of an external event.

671493 2-Digit BCD Counter

Application: Event Counter





- · Encodes eight data lines in priority
- · Output enable capability
- · Three-state outputs drive bus lines

Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
671494	N, J epation	Vague Com SoV

Description

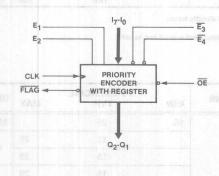
The 8-Bit Registered Priority Encoder accepts data from eight inputs (17-10) and provides a binary representation on the three outputs (Q2-Q0). A priority is assigned to each input (with I0 having the highest priority line, and I7 the lowest), so that when two or more inputs are simultaneously active, the input with the highest priority is loaded into the output registers. Pin 14 serves as the interrupt flag (FLAG) and goes LOW when there is an interrupt present and remains HIGH when there is not interrupt present. The Priority Encoder registers are updated on the rising edge of the clock. The device also features four priority interrupt enable lines: E1, E2, E3, E4, which enable or disable the FLAG output. These enable lines have no effect on the priority outputs Q2-Q0. All outputs are HIGH-Z when the output control line (OE) is HIGH, and OE operates independently of all other inputs.

Function Table

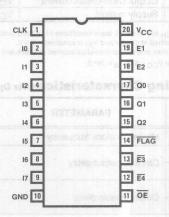
17	16	15	14	13	12	11	10	CLK	OE	FLAG*	Q2	Q1	Q0
E.	X	X	X	X	X	X	Н	13/20	E L	sado bo	Н	Н	Н
L	X	X	X	X	X	Н	L	1	L	L	Н	Н	L
L	X	X	X	X	Н	L	L	1	L	L	Н	L	Н
L	X	X	X	Н	L	L	L	1	L	E SELENCT	Н	L	L
L	X	X	Н	L	L	L	L	nol n	L	L	L	Н	Н
L	X	Н	L	L	L	L	L	aut i	aL.	k vel L ro.i	L	Н	L
L	Н	L	L	L	L	L	L	t	L	eval-fort	L	L	Н
Н	L	L	L	L	L	L	L	1	L	L	L	L	L
L	L	L	L	L	L	L	L	ov po	L	e e Hro.	Н	Н	Н
X	X	X	X	X	X	X	X	X	Н	Z	Z	Z	Z

Presumes E1, E2 = HIGH and $\overline{E3}$, $\overline{E4}$ = LOW. If the states of these four lines are different, the FLAG output will be disabled (HIGH), regardless of 10-17.

Block Diagram



Pin Configuration



TWX: 910-338-2376



7-37

Supply voltage VCC	7 V
Input voltage	7 V
Off-state output voltage	.5 V
Storage temperature -65°C to +150), C

Operating Conditions

SYMBOL	PARAMETE	MIN	COMMERCIAL TYP	MAX	UNIT	
VCC	Supply voltage	4.75	5	5.25	V	
TA	Operating free-air temperature		STREET ON SWITTERING	75	°C	
TC	Operating case temperature				°C	
	Ol- 1 - 1 III	Low	25	10		
tw	Clock width	High	25	10		ns
tsu	Setup time	35	15	osti i veta	ns	
th	Hold time	いって かんさ 日本学 一別	0		Chicago Tagas	ns

Electrical Characteristics Over Operating Conditions (1994) Jugar dage of designed at visions A (1904-SD) angluo

SYMBOL	PARAMETER	TEST CO	NDITIONS	MIN ger fl	COMMERCIA TYP†	L MAX	UNIT
V _I L*	Low-level input voltage	L V V V I	na al e anti-	BILLY WITH	eop ons text	0.8	V
VIH*	High-level input voltage		ACCUMENT ACT	2	VI OIT aniena	n toria anezenq	V
VIC	Input clamp voltage	VCC = MIN	I _I = -18 mA	bing west as o	-0.73	-1.5	V
HL H. J	Low-level input current	VCC = MAX	V _I = 0.4 V	tinte or disain	-0.02	-0.25	mA
I _H	High-level input current	V _{CC} = MAX	V _I = 2.4 V	hq sdi no i	otte om evanteen	il aldana a 25	μΑ
1	Maximum input current	V _{CC} = MAX	V _I = 5.5 V	aglico arti n	o MOH-S in ca	na aruqtuo 10	mA
VOL	Low-level output voltage	VCC = MIN VIL = 0.8 V VIH = 2 V	I _{OL} = 24 mA	He to whitelin	0.3	0.5	V
Vон	High-level output voltage	V _C C = MIN V _{IL} = 0.8 V V _{IH} = 2 V	I _{OH} = -3.2 mA	2.4			V
lozL	O# state subsub sussess	V _{CC} = MAX	V _O = 0.4 V			-100	
lozh	Off-state output current	V _{IL} = 0.8 V V _{IH} = 2 V	V _O = 2.4 V		2)	100	μΑ
los	Output short-circuit current**	VCC = MAX	V _O = 0 V	-30	-70	-130	mA
Icc	Supply current	VCC = MAX, Ou	itputs open		120	180	mA

† Typicals at V_{CC} = 5 V, T_A = 25°C.

Switching Characteristics Over Operating Conditions

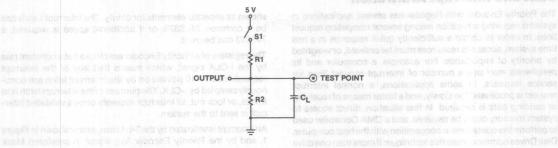
SYMBOL	PARAMETER	je Ta	TEST CONDITIONS	MIN	COMMERCIAL	MAX	UNIT
f _{MAX}	Maximum clock frequency	21		16	25		MHz
t _{PLH}	Clock to output dolor	7			15	25	
^t PHL		1	Commercial		15	25	ns
t _{PZL}			$C_L = 50 \text{ pF}$ $R_1 = 200 \Omega$		15	25	
^t PZH	Output enable delay	ock to output delay utput enable delay	$R_2 = 390 \Omega$		15	25	ns
^t PLZ	Output disable delay				15	25	
t _{PHZ}	Output disable delay			0.0000000000000000000000000000000000000	15	25	ns

 ^{*} V_{IL} and V_{IH} are, in effect, input conditions of DC and functional output tests and are not directly tested.
 V_{IL} is specified at ≤ 0.8 V and V_{IH} is specified ≥ 2.0 V.

 ** Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

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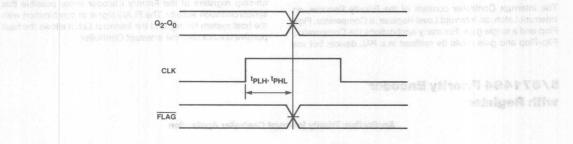
Standard Test Load



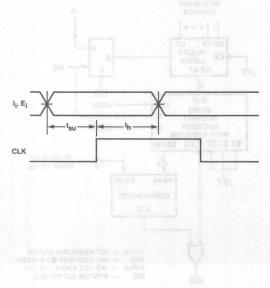
Notes: 1. tpD is tested with switch S1 closed. CL = 50 pF and measured at 1.5 V output level.

- 2. tpzx is measured at the 1.5 V output level with CL = 50 pF. S1 is open for high impedance to "1" test, and closed for high impedance to "0" test.
- 3. tpXZ is tested with C_L = 5 pF. S₁ is open for "1" to high impedance test, measured at V_{OH} -0.5 V output level; S₁ is closed for "0" to high impedance test measured at V_{OL} +0.5 V output level.

Output Timing says ledged an 1970 to the end to source of the company of the comp



Input Timing



Application: DMA and Interrupt Arbitration

The Priority Encoder with Register has several applications in systems requiring arbitration among several competing request lines. In order to obtain a sufficiently quick response in a real time system, access to resources must be ordered, or weighted by priority of importance. For example, a computer and its peripherals may use a number of interrupt request lines for service requests. In some applications, a normal interrupt request is processed too slowly, and a faster means of receiving or sending data is required. In this situation, direct access to system memory could be required, and a DMA Controller used to perform the operations in cooperation with the host computer. Disk Drives commonly use this technique; if more than one drive is in a system, a flexible means of arbitrating DMA requests would be required.

Figure 1 details how a Priority Encoder can be used to construct a Priority Interrupt Controller. Note that in this application, the inputs can either be DMA or Interrupt requests to the Host Computer. In fact, two circuits can be combined in one system to accommodate both types of requests. The expansion possibilities of Figure 1 will be covered after the basic operation of the circuit is explained.

The Interrupt Controller consists of the Priority Encoder, an Interrupt Latch, an Interrupt Level Register, a Comparator, Flip-Flop and a single gate. For many applications the Comparator, Flip-Flop and gate could be realized in a PAL device, but are

shown as separate elements for clarity. The Interrupt Latch can be a common 74LS373, or if additional speed is required, a 74S373 can be used.

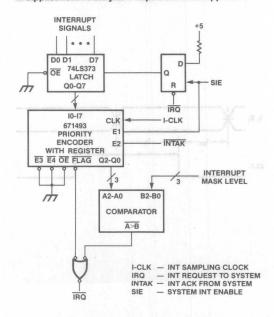
The registers of a Priority Encoder are clocked at a constant rate by the I-CLK signal, which means that any of the interrupt request lines 17-10 passed on by the interrupt latch are continously sampled by I-CLK. The purpose of the interrupt latch is to freeze, or lock out, all interrupt requests once a validated interrupt is sent to the system.

An interrupt is validated by the 3-bit comparator shown in Figure 1, and by the Priority Encoder flag signal. A prestored Mask Value from the Interrupt Level Register is compared with the current value of Q2-Q0, and if the priority code is greater, and if FLAG is LOW, the system is informed that an interrupt is needed. FLAG normally goes low when any of the 17-10 lines are asserted High, if simultaneously all of the Priority Encoder enables (E1, E2, E3 and E4) are asserted.

Because of the fact that in a typical system interrupts can occur at irregular intervals, the Interrupt Controller must be capable of synchronizing to the cycle timing of the host machine. The on-chip registers of the Priority Encoder make possible this synchronization activity. The FLAG signal in combination with the host system timing, and the Interrupt Latch allows the host positive control over the Interrupt Controller.

5/671494 Priority Encoder with Register

Application: Priority Interrupt Controller Application



(Single Burst Error Recovery IC)

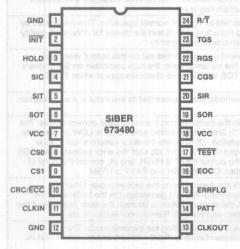
Features/Benefits

- 15 MHz data rate
- Selectable CRC or ECC polynomials
- Standard 16-bit CRC-CCITT polynomial detects errors
- · Computer-generated 32-bit ECC polynomial exceeds the performance of Fire code polynomials
- Double-burst error detection and single-burst error correction with ECC polynomial
- . Programmable correction span of 5, 8 or 11 bits
- Hardware or software correction modes
- Separate receiver and transmitter ports
- · HOLD pin for idle operation
- . Maximum of 1024 bytes of data
- Inverted checkbits and selective initialization to a HIGH state improve reliability

Description

The SiBER (Single Burst Error Recovery) is a LSI error detection and correction circuit used to insure data integrity between two serial ports. An industry standard 16-bit CRC polynomial and a 32-bit computer-generated ECC polynomial are both implemented on this chip. Both polynomials have error detection capabilities, but only the ECC polynomial is used for error correction. The ECC polynomial has a maximum correction span of 11 bits in series and a maximum record length of 1024

Pin Configuration



Ordering Information

100	PART NUMBER	PACKAGE	TEMPERATURE		
10	673480	J	Com		

bytes of data. The 16-bit CRC polynomial is the industry standard CCITT polynomial:

The 32-bit computer-generated ECC polynomial is selected for its error detection span, and the high probability of detecting short double-burst errors:

$$x^{32} + x^{28} + x^{26} + x^{19} + x^{17} + x^{10} + x^{6} + x^{2} + 1$$

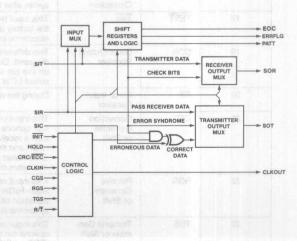
The SiBER implements the transmit, receive, search, and correct algorithms, which are basically serial division operations. By simply asserting the appropriate control signals, spelled out in the "modes of operation" section of this data sheet, the user can:

- 1) Append checkbits to the data under transmission.
- 2) Generate the syndrome from received data.
- 3) Correct erroneous data bits with the information embedded in the syndrome.

Selective inversion of checkbits and selective initialization of the internal registers to an all-one-state insure randomness in the encoded checkbits and, consequently, improve reliability.

Typical applications of the SiBER include mass storage environments and data communication channels.

Block Diagram



TWX: 910-338-2376

SiBER Pin Description

PIN NUMBER	SYMBOL	PIN NAME	FUNCTION
1, 12	GND	Ground	Electrical Ground
2	ĪNIT	Initialize	An active LOW asynchronous input pulse is used to reset all internal registers and output flags before transmitting or receiving any data.
3	HOLD	Hold	Raising this input HIGH puts the device in idle operation by holding its present state. The data present on SIT is sent to SOT. A LOW presented on this pin resumes normal operation.
meC	SIC	Serial Input Correction	During hardware correction, the buffered data is presented to this input one bit at a time in reverse order. If the data bit is erroneous it is corrected and placed on SOT. See block diagram for data flow.
5	SIT	Serial Input Transmitter	During the transmit mode, data to be transmitted is presented to this input in a serial fashion.
6 Introdes a tarrec	SOT	Serial Output Transmitter	Four different types of data are shifted out on this output (see block diagram). Data on SIR appears on this pin during receive mode; corrected data appears during hardware correction, error syndrome appears during software correction; and error pattern appears during hardware/software correction.
7, 18	VCC	VCC	+5 volt supply.
8,9 d., consumate some consumer consumer consumer consumer consumer consumer streets.	CS ₀ , CS ₁	Correction Span Select	Correction spans that can be selected by specifying CS ₀ and CS ₁ are: a 5-bit correction span (CS ₀ = LOW, CS ₁ = LOW), an 8-bit correction span (CS ₀ = LOW, CS ₁ = HIGH), and an 11-bit correction span (CS ₀ = HIGH, CS ₁ = HIGH). The fourth state (CS ₀ = HIGH, CS ₁ = LOW) is restricted and must never be entered. It is used by the factory during manufacturing to test the device for enhanced quality assurance and guaranteed functionality.
102 102 153	CRC/ECC	CRC/ECC Select	This input control line is used to select the desired polynomial. The 32-b computer-generated ECC polynomial is selected when CRC/ECC is LOV and the 16-bit standard CRC-CCITT polynomial when CRC/ECC is HIGH
BOU HTO IT OF	CLKIN	Clock Input	This is the clock input, and the rising edge is used to strobe the data during the transmit, receive, and correction modes of operation.
on 13 a bnis	CLKOUT	Clock Output	The Clock output is a delayed clock input. It is generally used for synchronization of all output signals from the SiBER.
Admid14 on ever	PATT	Pattern Flag	This output is set HIGH (and remains set until initialized) when the error pattern is found by the SiBER.
15	ERRFLG	Error Flag	This output is set HIGH (and remains set until initialized) when the syndrome is nonzero. A nonzero syndrome at the end of the receive cycle means that the data read is in error.
16	EOC	End of Correction	This output is set HIGH (and remains set until initialized) eleven clock cycles after the pattern flag is set.
17	TEST	Test	This input must be tied to V _{CC} for normal operation. This pin is used by the factory during manufacturing to test the device for enhanced quality assurance and guaranteed functionality.
19	SOR	Serial Output Receiver	Two different types of data are shifted out on this output (see block diagram). During the transmit mode, the data presented on SIT appears on this pin when TGS is HIGH, and checkbits appear when TGS is pulled LOW.
20	SIR	Serial Input Receiver	During the receive mode, data is presented to this input in a serial fashion
21	CGS	Correction Generate or Shift	This input controls the device during the search and correct modes. The four options are: (1) Shift the syndrome when CGS is LOW immediately after a receive operation, (2) generate the error pattern when CGS is HIGH and the output PATT is LOW, (3) shift the error pattern when CGS is LOWered and the output PATT is HIGH, and (4) correct the burst of erroneous data when CGS is HIGH and PATT is HIGH.
22	RGS	Receive Generate or Shift	This input controls the device during the receive mode. When RGS=HIGH the syndrome is being generated. On the HIGH-to LOW transition of RGS, the error condition is latched; the error flag is set if the syndrome is nonzero and the SiBER enters correction mode.
23	TGS	Transmit Gen- erate or Shift	This input controls the device during the transmit mode. The two options are to generate checkbits (TGS = HIGH) and to shift checkbits (TGS = LOW).
24	R/T	Receive/ Transmit	This input pin controls the mode of operation. A LOW enables the transmit mode, and a HIGH enables the receive mode.

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Modes of Operation

Prior to performing any operation, the appropriate correction span and polynomial type must be selected. The settings of the

control signals for each of the four options are summarized below:

SIGI	NALS	geoministry.	DESCRIPTION
CRC/ECC			DESCRIPTION
0	0	0	5-bit correction span, ECC polynomial
AST WENA	0	тмояск	8-bit correction span, ECC polynomial
0	1_		11-bit correction span, ECC polynomial
1	×	X	No correction, CRC polynomial generation
X	1	0	Illegal state. It is only used by the factory for testing the devices.

[&]quot;X" Designates "Don't Care"

The four different modes of operation are tabulated below. Note that the CRC polynomial cannot go into the search/correct

mode, but the other modes and functions are common to both the CRC and ECC polynomials.

the case of a non-zero	CONTROL SIGNALS			DATA PATH		e SiBEH generates a syndrome. To initialize the devic	
(HOTH MODE FIS) one	R/T	TGS	RGS	cgs	IN	OUT	setted winto A/T is DESCRIPTION as legisters and the set in the receive mode.
TRANSMIT	000	ne opntro oxrection	X	X	SIT	SOR	Generate checkbits from the data placed on SIT. This data appears on SOR.
	0	0	X	n e X	an X	SOR	Shift the checkbits serially on SOR.
RECEIVE	003 -# 038413-4	X	1	X	SIR	SOT	The data on SIR appears on SOT. Simultaneously the syndrome is generated in the 32-bit feedback shift register.
	1	X	ţ	X	X	X	Set the error flag if the syndrome is nonzero.
SEARCH	1	X	0	- Arac	X	X	Search for the error pattern.
(ERRFLG = H, PATT = L)	202-4	X	0	0 81	B = X = 0	SOT	Shift the syndrome serially on SOT. (software correction)
CORRECT (ERRFLG = H.	1	X	0	- 1 - 4700	SIC	SOT	Data placed on SIC is corrected and placed on SOT. (hardware correction) ¹
PATT = H)	1	X	O THATE HAR	0	RCBAYS RO	SOT	Shift the error pattern. (software/hardware correction)

NOTE: 1. In this mode, data placed on SIC is transmitted to SOT. This feature allows the user to implement a read-modify-write operation on buffered data without paying attention to the pattern flag PATT.

Transmit Mode

In this mode, the SiBER generates the unique checkbits for the data being transmitted. These checkbits are appended to the end of the data stream. To initialize the device $\overline{\text{INIT}}$ is asserted while R/\overline{T} is LOW. The internal registers and the output flags are reset and the device is in the transmit mode. If TGS is LOW the SiBER will remain initialized until TGS is pulled HIGH. This feature is implemented to allow relaxed initialization timing. Once TGS is

HIGH the device starts to generate checkbits for the data present on SIT. The data on SIT also appears on the SOR output. When the last data bit is transmitted, LOWer TGS and the 32 checkbits for the ECC polynomial or the 16 checkbits for the CRC polynomial are serially shifted out on SOR. Figure 1 shows the data flow during the transmit mode. TGS must remain low for at least 32 clock cycles for the ECC polynomial or 16 clock cycles for the CRC polynomial to allow all the checkbits to be shifted out.

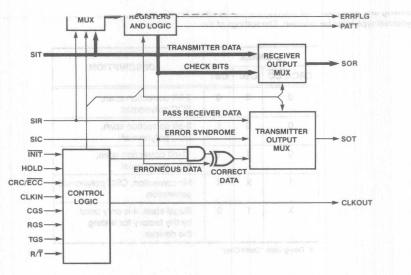


Figure 1. Data Flow During the Transmit Mode

Receive Mode

In this mode, data and checkbits are read from the SIR pin and the SiBER generates a syndrome. To initialize the device $\overline{\text{INIT}}$ is asserted while R/ $\overline{\text{T}}$ is HIGH. The internal registers and the output flags are reset and the device is in the receive mode. If RGS is LOW the SiBER will remain initialized until RGS is pulled HIGH. The feature is implemented to allow relaxed initialization timing. Once RGS is HIGH, the device starts to generate the syndrome for the data present on SIR. The data on SIR also appears on the

SOT output. When the last data bit, which is really the last checkbit that was appended to the block of data, is presented on SIR, the error flag ERRFLG is latched on the HIGH-to-LOW transition of RGS; the error flag is set for the case of a non-zero syndrome. When the syndrome is non-zero (ERRFLG = HIGH) and the ECC polynomial is asserted, then the search mode is invoked. The state of the control pin CGS determines the operation performed. The correction cycle is not invoked when the CRC polynomial is asserted. Figure 2 shows the data flow during the receive mode.

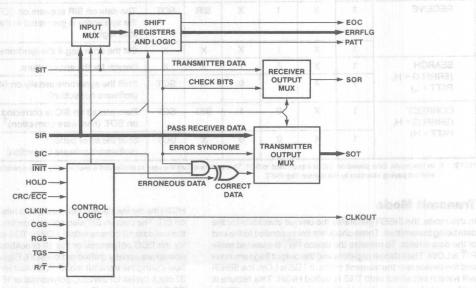


Figure 2. Data Flow During the Receive Mode

7

Search/Correct Mode

The search/correct mode is used to find the error pattern required to correct the erroneous data record that has just been received. The error pattern can be found by shifting the 32-bit syndrome (left by the receive operation) backwards until a correctable pattern is found, or the search is exhausted by clocking beyond the length of the data record (which indicates the error is uncorrectable). Note that the search/correct mode pertains only to ECC operations and not to CRC operations.

When an error occurs, and correction of the error is desired, there are three methods of finding the error and correcting it, as follows:

- Pass the syndrome on to the host processor for software correction
- Perform a correction pattern search inside the SiBER and pass the error pattern on to the host processor for correction (hardware/software correction).
- 3) Pass the data record to be corrected through the SiBER (in reverse order) while the SiBER performs the pattern search AND corrects the data record 'on the fly' as it passes through the SiBER chip.

Typically, after the last bit of the ECC field of the data record being read is clocked into the SiBER, RGS is deactivated and HOLD is activated. One clock later, the ERRFLG signal will reflect the final state of the ECC/CRC shift register. It is at this time the system must decide whether to perform a correction or not. Typically, in magnetic media implementations, the system may perform one or more retries on the data record before attempting the correction (some systems will retry until subsequent received ECC fields or syndromes generated by receive operations, are found to be identical).

The Syndrome can be clocked out of the SiBER by simply deactivating the HOLD signal, allowing the syndrome to be shifted out of the SiBER on the SOT line. If the SiBER is to be used to perform all or part of the correction function (as in method 2 or 3), the CGS signal is activated and the HOLD signal is deactivated and the search operation begins.

The first clock cycle of the search operation is used to prepare the syndrome for reverse polynomial shifting. From then on, the SiBER looks for error burst patterns to appear in the ECC shift register. The exact type of pattern searched for is dependent on the correction span selection input signals, CS0 and CS1 (5-, 8-, or 11-bit maximum burst lengths). When an error pattern that fits the qualifications of the correction span inputs is found in the proper position of the ECC shift register, the PATT signal is activated by the SiBER. If method 2 is being used, then the error pattern is shifted out of the SiBER (by lowering the CSG input) when the PATT signal has become active (the HOLD signal can be used to aid in controlling the transition between searching and error pattern shifting, for system timing constraints). Note: the error pattern being shifted out of the SiBER will be generated in the reverse order with respect to the original data received. It may also be noted that the error pattern extracted will be CS bits long (where CS represents the selected correction span) regardless of the actual error burst length. When an error burst whose length is less than the correction span selected is found, the first N bits of the error pattern from the SiBER will be zeros (where N correction span - actual error burst length). For example, if a single-bit error burst occurs and correction is performed with an 8-bit correction span selected, then when the error pattern is found, the first seven bits of the error pattern out of the SiBER will be zeros, and the eighth bit will be a one.

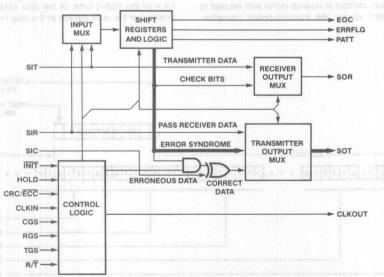


Figure 3. Data Flow During the Search/Correct Mode for Method 1 and Method 2.

The Error Syndrome or Pattern is Shifted Out on SOT

Once the pattern is found, the number of clock cycles required to find it, NCC, is used to calculate the position of the error. The calculation is made with respect to the end of the data record *including* the 32-bit ECC field. The calculation is as follows: ED = NCC-1 (where ED is the Error Displacement in bits, NCC is the Number of Clock Cycles required to find the pattern, and 1 for the search preparation). Therefore, if the pattern is found in one clock, the error displacement, ED, will be zero, indicating the error pattern was found at the end of the ECC field of the data record.

Since the ECC field is used only for error detection and correction, many systems do not store this field if dedicated hardware is used for correction. Therefore the Error Displacement equation can be modified to calculate the distance with respect to the end of the data field, instead of the ECC field. The calculation would then be: ED = NCC -33. Note that the Error Displacement can, in this case, be a negative number. This simply indicates that the error burst is partially, if not entirely, contained in the ECC field. Careful consideration for boundary conditions are required in these cases.

The maximum number of clock cycles, MNC, to find a correctable error pattern with the SiBER is calculated as: MNC = DL + 33 - CS (where DL is the number of bits in the data field, and CS the selected correction span), which corresponds to an error burst at the beginning of the data field. The search operation should be terminated if the PATT signal has not been activated within the number of clock cycles calculated in the above equation for MNC. If the error pattern cannot be found within MNC clock cycles, then the error is considered uncorrectable and no further action can be taken.

Method 3 is implemented with the SiBER by retransmitting the data record through the SiBER during the pattern search. Note: The data record is transmitted in reverse order with respect to the receive operation, during the search/correct operation.

When the SiBER finds the error pattern, the data being presented at the SIC input is XORed with the error pattern and retransmitted, via the SOT output, as corrected data. During other periods of the search/correct operation, the data presented at the SIC input is retransmitted to the SOT output, unchanged.

After a receive operation with an error condition present, the SiBER starts the search/correct operation, just as described for method 2, by asserting the CGS input line. For proper positioning of the retransmitted data with respect to the error pattern to be found, the SiBER must be clocked once (if the data record retransmission includes the 32-bit ECC field) or thirty-three times (if the data record retransmission does not include the 32-bit ECC field) before data bits are presented at the SIC input and captured at the SOT output.

If the PATT output does not become active within MNC clock cycles, as calculated above, then the error is uncorrectable.

Example: and armonec. - 1813 and reliable (nebro exteren

Data Field = 512 bytes = 4096 bits

Correction Span = 11 bits

MNC = (4096 + 33 - 11) = 4118 clock cycles

Therefore, with this format, all correctable error patterns must be found within 4118 clock cycles from when the search/correct operation began, otherwise the error is uncorrectable.

If a search operation finds the error pattern in 1787 clock cycles, then the 11-bit error burst starts (in reverse order) 1786 bits from the end of the ECC field or 1754 bits from the end of the data field. This can be recalculated for forward displacement as (4096-1754-11) bits = 2331 bits from the beginning of, or starting with bit 4 of the 292nd byte, of the data field. Figure 4 shows the position of the error pattern in the data field.

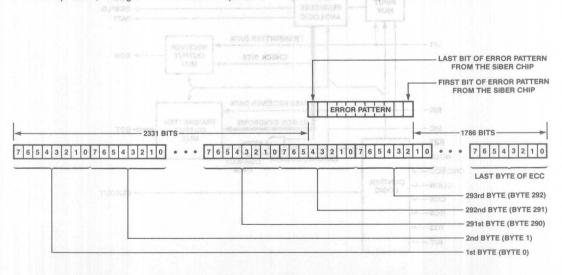
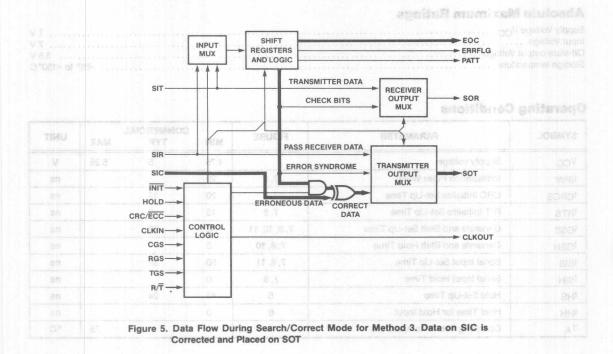


Figure 4. Example



Multiple Burst Errors

When there is an error, the error flag ERRFLG goes HIGH. If this error is within the correcting capability of the code, then PATT goes HIGH when the error pattern is found. If there is a multiple error of two or more bursts and the capability of the code is

exceeded, then the pattern flag PATT remains LOW during the search mode. The SiBER is recommended for detecting and correcting bursts of errors in 1K bytes of data or a total of 8K bits in a serial stream. It can be used for even larger streams, but the probability of miscorrection is increased.

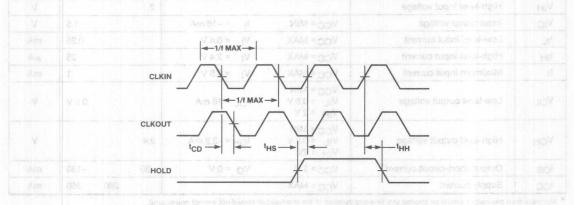


Figure 6. Clock and Hold Timing

upply Voltage V _{CC}	7 V
put Voltage	7 V
ff-state output Voltage	.5 V
orage temperature -65° to +150)°C

Operating Conditions

SYMBOL	PARAMETER	FIGURE	MIN	COMMERCIAL TYP	MAX	UNIT
Vcc	Supply voltage	ohan Å	4.75	5	5.25	V
tIPW	Initialization Pulse Width	7, 8	20	2000		ns
tCRCS	CRC Initialize Set-Up Time	7, 8	20	12		ns
trs trs	R/T Initialize Set-Up Time	7, 8	15	8		ns
tGSS	Generate and Shift Set-Up Time	7, 8, 10, 11	50	27		ns
tGSH	Generate and Shift Hold Time	7, 8, 10	0	= -820		ns
tsis	Serial Input Set-Up Time	7, 8, 11	50	32		ns
tSIH	Serial Input Hold Time	7, 8	0	8.01		ns
tHS	Hold Set-Up Time	6	45	24		ns
tHH	Hold Time for Hold Input	6	0			ns
TA	Operating free-air temperature	ing Search/Clar	0	Figure 5. Date	75	°C

Electrical Characteristics Over Operating Conditions

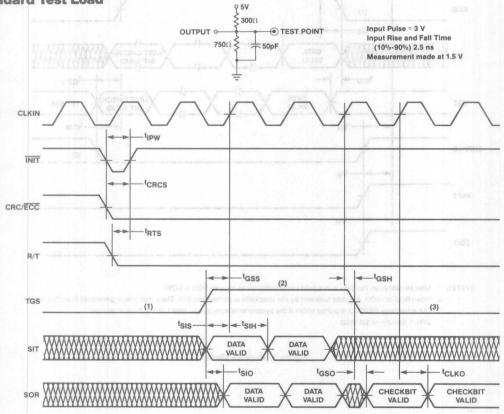
SYMBOL	PARAMETER	d gnipsence TEST	CONDITION	MIN	P MAX	UNIT
VIL	Low-level input voltage	Selfa nethale in the self- shi to voltachariones — à	i pason a anerena a como a paso entro de viniciana	oter regulacijis. Sp.: Sma etak	0.8	V
VIH	High-level input voltage			2		V
VIC	Input clamp voltage	VCC = MIN	I _I = -18 mA		-1.5	V
IIL	Low-level input current	V _{CC} = MAX	V _I = 0.4 V		0.25	mA
lн	High-level input current	V _{CC} = MAX	V _I = 2.4 V		25	μΑ
l ₁	Maximum input current	VCC = MAX	V _I = 5.5 V	reduce.	1	mA
VoL	Low level output voltage	V _{CC} = MIN V _{IL} = 0.8 V V _{IH} = 2 V	I _{OL} = 16 mA		0.5 V	V
Vон	High level output voltage	V _{CC} = MIN V _{IL} = 0.8 V V _{IH} = 2V	I _{OH} = -3.2 mA	2.4		٧
los	Output short-circuit current*	V _{CC} = 5 V	VO = 0 V	-30	-130	mA
ICC	Supply current	VCC = MAX		28	360	mA

^{*} Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	FIGURE	MIN	MERCIAL TYP	MAX	UNIT
fMAX	Maximum Clock Frequency	6	laborate de la labora	land stage	15	MHz
tsio	Serial Input to Output Delay	7, 8, 11		25	35	ns
tGSO	Generate to Serial Output Delay	7-11		25	35	ns
tCLKO	Clock to Output Delay	7, 9, 10	92	49	60	ns
tERR	RGS to ERR Delay	8, 9, 10		20	30	ns
tPAT	Clock to PATT Delay	10, 11		33	42	ns
tEOC	Clock to EOC delay	10, 11	and the	33	40	ns
tFR	Initialize to Flags Reset Delay	8		27	35	ns
tCD	CLKIN to CLKOUT Delay	6		12	18	ns

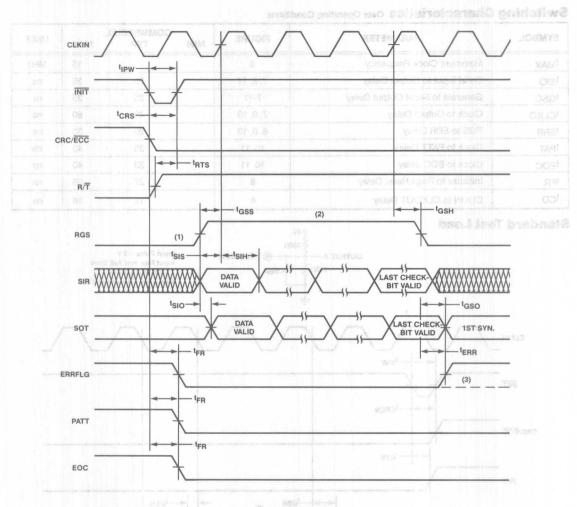




NOTES: 1. After Initialization the chip is in a hold mode (idle) for as long as TGS is LOW.

- 2. When TGS is HIGH, the data to be encoded is shifted into SIT. The maximum data length is 1K bytes.
- 3. When TGS is lowered in the transmit mode the checkbits are shifted out on SOR. There are 32 checkbits for the ECC polynomial and 16 for the CRC polynomial.

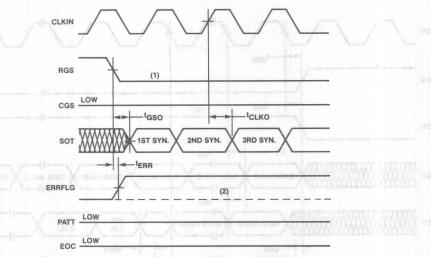
Figure 7. Transmit Mode



- NOTES: 1. After Initialization the chip is in a hold mode (idle) for as long as RGS is LOW.
 - 2. When RGS is HIGH, the data followed by the checkbits is shifted into SIR. The syndrome is generated from this data.
 - The error flage ERRFLG is pulled HIGH if the syndrome is non-zero or kept LOW if there is no error.
 SYN. = Syndrome Bit Valid

Figure 8. Receive Mode





NOTES: 1. When RGS is pulled LOW in the receive mode and CGS and PATT are LOW, the 16-bit syndrome for the CRC polynomial or the 32-bit syndrome for the ECC polynomial is shifted out on SOT. This is called the search mode.

Figure 9. Search Mode for Software Correction

The error flag ERRFLG remains LOW when there is no error.
 SYN. = Syndrome Bit Valid

CLKIN tgss RGS (1) ← t_{GSH} t_{GSS} CGS (4) tCLKO tgso 2ND E.P. E.P. TERR **ERRFLG** (2) <--tPAT PATT (3)

- NOTES: 1. When CGS is HIGH, the SiBER is clocked until PATT is flagged. This is the search mode in which the location of the error pattern is determined.
 - 2. The error flag ERRFLG remains LOW if there is no error.
 - 3. A multiple error is indicated when ERRFLG is HIGH and PATT remains LOW.
 - 4. When CGS is LOWered after PATT goes HIGH, the error pattern is shifted out on SOT. This is called the correction mode.
 - 5. 11 clock cycles after PATT is flagged, EOC goes HIGH.

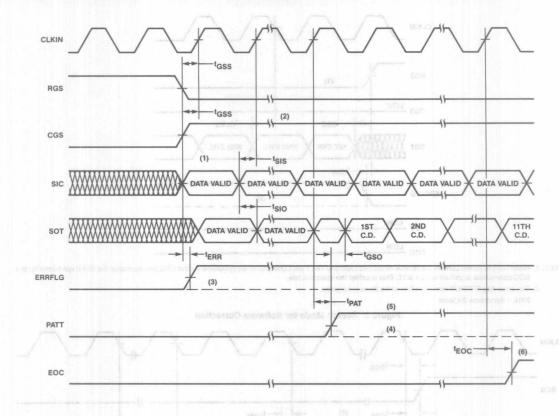
E.P. = Error Pattern Bit Valid

EOC

Figure 10. Search and Correct Modes for Software/Hardware Correction

tEOC

(5)



- NOTES: 1. Data placed on SIC is transmitted to SOT. This feature allows the user to implement a ready-modify-write operation on buffered data without paying attention to the pattern flag PATT.
 - 2. When CGS is HIGH the SiBER is clocked until PATT is flagged. This is the search mode in which the location of the error pattern is determined.
 - 3. The error flag ERRFLG remains LOW if there is no error.
 - 4. A multiple error is indicated when ERRFLG is HIGH and PATT remains LOW.
 - 5. When PATT is HIGH, the data across SIC is inverted, if erroneous, and shifted out on SOT.
- 11 clock cycles after PATT is flagged, EOC goes HIGH.
 C.D. = Corrected Data Bit Valid

Figure 11. Search and Correct Modes for Hardware Correction

Application

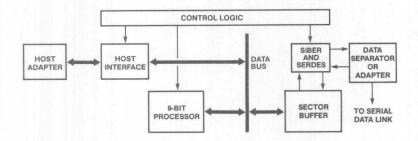


Figure 12. System Block Diagram

The SiBER and the Serializer/Deserializer (SERDES) block, shown in more detail in Figure 13, reside in the front end of a typical system. This block will append the checkbits to the data under transmission and it will generate the syndrome from the

received data. Correction can be performed in case of an error. Four operations take place under external control provided by the control logic block.

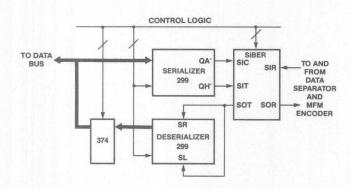
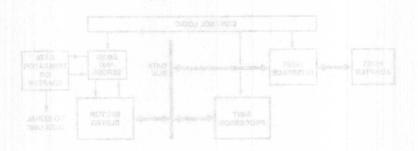


Figure 13. Detailed SiBER and Serializer/Deserializer (SERDES) Block



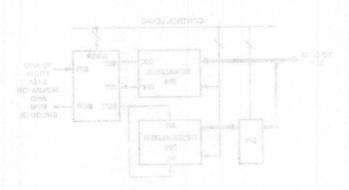
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Regula 12. Bystem Block Diagram

The SiBER and the Settable of Description (SERDES) block, shown in more (Seat to Figure 1. recide in the front and at a 1, out it system. This block will as end the checkfitts to the data under transmission and it will generate the swintroms from the

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Pyrine 13. Detailed SHRER and Serializer/Description (SERDES) (North



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6	HAL®/ZHAL™ Devices		
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10	Arithmetic Elements and Logic		
11	Multipliers	1	
12	8-Bit Interface		
13	Double-Density PLUS™ Interface		
14	ECL10KH		
15	Logic Cell Array		
16	General Information		
17	Advance Information		
18	Package Drawings		
19	Representatives/Distributors		

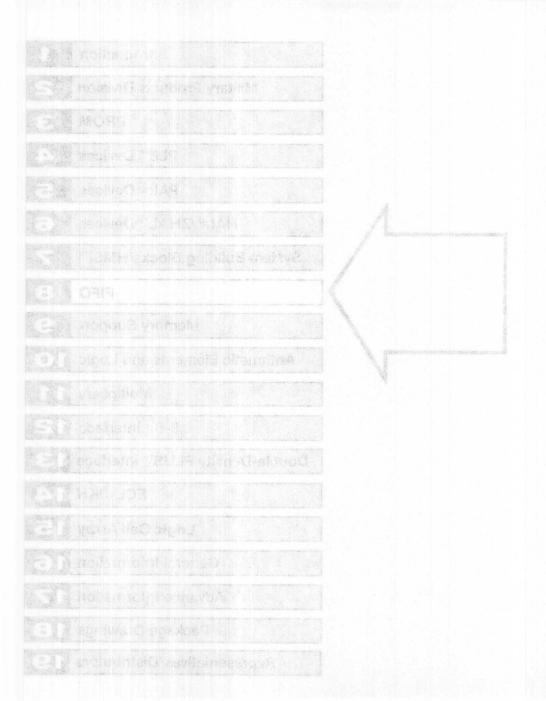


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PACKAGES	enura#	CHGAWZATION	MAXIMUM	STANDALONE
			25 MHz	
	Iou = 24 mA. Three-State Status Flags			87413A

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	\$4,143		
			C67402
		ENORS	

8

FIRST-IN FIRST-OUT BUFFER MEMORIES

Product Selection and Application Reference Guide

Low-Power FIFOs

	CASCADABLE/ STANDALONE	MAXIMUM DATA RATE	ORG.	MAXIMUM	FEATURES	PACKAGES	PINS
19-8 19-8	67L401*	5 MHz	64x4	100 mA	E1-8 bidso	N,J,NL (20)	16
18-E	67L402*	5 MHz	64x5	130 mA	81.8 8-19	N,J,NL (20)	18
18-8 17-8	C67L401D*	15 MHz	64x4	100 mA	IOL = 24 mA	N,J,NL (20)	16
7-8	C67L402D	15 MHz	64x5	100 mA	I _{OL} = 24 mA	N,J,NL (20)	18
100	C67L4033D	15 MHz	64x5	115 mA	IOL = 24 mA, Three-State, Status Flags	N,J,NL (20)	20
or-s	C67L4013D	15 MHz	64x4	100 mA	IOL = 24 mA, Three-State	N,J,NL (20)	16

^{*} Standalone only.

High-Performance FIFOs

STANDALONE	MAXIMUM DATA RATE	ORGANIZATION	FEATURES	PACKAGES	PINS
67411A	35 MHz	64×4	I _{OL} = 24 mA	J	16
67412A	35 MHz	64x5	I _{OL} = 24 mA	J	18
67413A	35 MHz	64x5	IOL = 24 mA, Three-State, Status Flags	J	20
67411	25 MHz	64x4	I _{OL} = 24 mA	J	16
67412	25 MHz	64x5	I _{OL} = 24 mA	J	18
67413	25 MHz	64x5	IOL = 24 mA, Three-State, Status Flags	J	20

Standard FIFOs

CASCADABLE	STANDALONE	MAXIMUM DATA RATE	ORGANIZATION	PACKAGES	PINS
C67401	67401	10 MHz	64x4	N, J, NL (20)	16
C67402	67402	10 MHz	64x5	N, J, NL (20)	18
C67401A	67401A	15 MHz	64x4	N, J, NL (20)	16
C67402A	67402A	15 MHz	64x5	N, J, NL (20)	18
C67401B	67401B	16.7 MHz	64x4	N, J	16
C67402B	67402B	16.7 MHz	64x5	N, J	18

System FIFOs

DEVICE	DESCRIPTION	ORGANIZATION	PACKAGES	PINS	MAXIMUM FREQUENCY
67417	Serializing FIFO Memory Serial data buffering with optional Serial-to- Parallel or Parallel-to-Serial data conversion	64x8/9	J	24	28 MHz Serial 10 MHz Parallel
674219	FIFO RAM Controller Provides control for SRAM to act as a FIFO buffer	Up to 64K words		1	24 MHz Clock

FIFO Applications

APPLICATION	KEY REQUIR	EMENTS residing bettereby theye	FIFO PRODUCTS
Microprocessor/CPU Buffering	Data rate of processor System architecture (word width)	or individual dribs and dribs of e" may be a sound principle by lat a time or even "one byte at a	74S225/A C/67401/2A/B 67411/2/3A
Peripherals	High data rate or low power Status flag	sich to make your microprocessor sible service from it. sibled "FIFCs" which let you keen.	C/67401/2A/B 67L401/2 C67L401/2/3D
Data/Telecom	High data rate or low power Status flags Word depth (high storage capacity) Data format (serial or parallel)	and let each portion of your bill wants to see end yet let you cot your software by constantly saos, or even by intermittently	001 1011200
Data Acquisition	High data rate	reemary for a short time. FIFOs torage" devices - "logical rubber	67411/2/3A 74S225A

FIFO Application Notes From Monolithic Memories "System Design Handbook"

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AN-149	FIFOs: Operations and Applications	5-11
AN-150	Second Generation FIFOs Simplify System Design and Open New Application Areas	5-23
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AN-100	PROMs, PALs, FIFO, and Multipliers Team Up to Implement Single-Board High-Performance Audio Spectrum Analyzer	12-3
CP-116	System Solutions for a High-Speed Processor Using Innovative ICs	7-3

Monolithic Memories FIFO Technical Support Hotline 1-800-247-6527 ex. 6197 or 6239

to Hold Your System Together

Chuck Hastings

Introduction

Data-rate matching problems are a very basic part of the life of a builder of digital systems. Some important electromechanical devices such as disk drives produce or absorb data at totally inflexible rates governed by media recording densities and by the speeds at which small electric motors are naturally willing to rotate. Other devices such as letter-quality printers have maximum data rates beyond which they cannot be hurried up, and which are relatively slow compared to the rates of other devices in the system.

Microprocessors and their associated main memories are generally faster and more flexible than other system components, but often operate with severly degraded efficiency if they must be diverted from their main tasks every few milliseconds to handle data-ready interrupts for individual dribs and drabs of data. While "one day at a time" may be a sound principle by which to live your life, "one bit at a time" or even "one byte at a time" is not a philosophy by which to make your microprocessor live if you want the best possible service from it.

Today there are components called "FIFOs" which let you keep your hardware design simple, and let each portion of your system see the data rate which it wants to see, and yet let you avoid hobbling the performance of your software by constantly interrupting your microprocessor, or even by intermittently halting it in order to let DMA (Direct Memory Access) circuits take over control of the main memory for a short time. FIFOs may be thought of as "elastic storage" devices — "logical rubber bands" between the different parts of your system, which stretch and go slack so that data rates between different subsystems do not need to match up on a short-term microsecond-bymicrosecond basis, but only need to average out to be the same over a much longer period of time.

This tutorial paper both describes what FIFOs are in general, and introduces the 64x4 and 64x5 Monolithic Memories FIFOs in particular.

What is a FIFO?

FIFO is one of those made-up words, or acronyms, formed from the initials of a phrase — in this case, "First-In, First-Out." Originally, the phrase "First-In, First-Out" came from the field of operations research, where it describes a queue discipline which may be applied to the processing of the elements of any queue or waiting line. There is also a LIFO, or "Last-In, First-Out" queue discipline. The terms FIFO and LIFO have also been used for many years by accountants to describe formal procedures for allocating the costs of items withdrawn from an inventory, where these items have been bought over a period of time at varying prices.

You can probably think of some simple, everyday objects which in some manner behave according to the FIFO queue discipline. For instance, little two-seater cable-drawn boats are drawn through an amusement park tunnel of love one by one, and must emerge from the other end in the same order in which they entered the tunnel — "First-In, First-Out." The old-time coin dispensers used by the attendants at such amusement park features, or by city bus drivers, are "buffer storage" devices for coins which handle the coins in this same manner. (See Figure 1.)

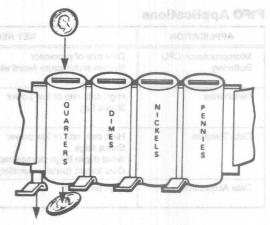


Figure 1. Primitive Mechanical FIFO Device

Notice also that the input of a coin into one of the tubes of such a coin dispenser through the slot at the top, and the output of a coin at the bottom of that tube when the lever for that tube is pushed, are completely independent events which do not have to be synchronized in any way, as long as the tube is neither totally empty nor totally full. However, if the tube fills up completely, a coin inserted into the slot will not go into the tube. Likewise, if the tube empties out completely, no coin is released from the tube at the bottom when the lever is pressed. The coin tube thus behaves as an asynchronous FIFO. Keep this homely example in mind.

In computer technology, both the FIFO queue discipline and the LIFO queue discipline are frequently used to control the insertion and withdrawal of information from a buffer memory, or from a dedicated buffer region of some larger memory. In input/output programming practice, a FIFO memory region is sometimes referred to as a *circular buffer*, and in programming for computer-controlled telephone systems it is called a *hopper*. A LIFO memory region is usually referred to as a *stack*.

67401 was originally designed as a faster bipolar upgrade of a

MOS part, the Fairchild 3341, which needs a second power-

The reason for having a 5-bit model as well as a 4-bit model of

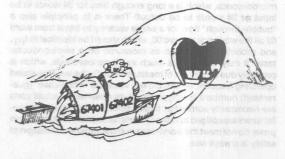
next to a 67401 makes a 9-bit FIFO, and two 67402s make a 10-bit FIFO. But I'm getting ahead of myself.

Pinouts are indicated in the data sheet.

FIFOs: Rubber-Band Memories to Hold Your System Together

A logic HIGH signal on the Input Ready line indicates that there is at least one vacant memory location within the FIFO into which a new data word may be inserted. Likewise, a logic HIGH on the Output Ready line indicates that there is at least one data word currently stored within the FIFO and available for reading at the outputs. The operation of the FIFO is such that, once a data word has been inserted at the Data In lines (the top of the FIFO, as it were), this word automatically sinks all the way to the bottom (assuming that the FIFO was previously empty) and forthwith appears at the Output lines. (Remember the synonym hopper?) in keeping with the FIFO queue discipline, the first word which was inserted is the first one available at the outputs, and additional words may be withdrawn only in the order in which they were originally inserted.

There is no provision for random access in these FIFOs, since their internal implementation uses one particular variation of shift-register technology. Each FIFO word consists of 4 (for the 67401) or 5 (for the 67402) data bits, plus a control or "presence" bit which indicates whether or not the word contains significant information. There are thus 4 or 5 data "tracks" and one presence "track" if you look at a FIFO from a magnetic-tape perspective. What the Master Reset input does is to clear all of the bits in the presence track, and in addition to clear the very last data word (at the "bottom") which controls the Output lines. The other 63 data words are not cleared, but it doesn't really matter; their status is like unto that of operating-system files whose Directory entries have been deleted, in that they can no longer be read out and will get written over as soon as new information comes in.



WHICH MAY BE APPLIED TO THE PROCESSING OF THE ELEMENTS OF ANY QUEUE ..."

Both FIFO and LIFO memories have frequently been implemented as special-purpose digital systems or subsystems, but as of the present time only FIFO memories are commonly implemented as individual, self-contained semiconductor devices.

Representative FIFOs

To give you the flavor of what these semiconductor devices are like, I'll describe the type 67401 64x4 FIFO and type 67402 64x5 FIFO which have been available for several years from Monolithic Memories. ("64x4" here means containing 64 words of 4 bits each.) These parts have a basic, easy-to-understand architecture and control philosophy. They also happen to be the fastest FIFOs available through normal commercial channels as of this writing, and they are in widespread use for applications ranging from microcomputers up to IBM-lookalike mainframes and large special-purpose military radar processors. A 67401 is internally organized as follows:

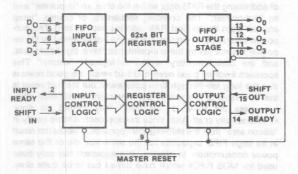


Figure 2. Architecture of the 67401 FIFO

The list of signals/pins for the 67401 is:

TYPE	HOW MANY	(CUM.)	I/O/V
Data In	4	4	an soid
Output	4	8-108	0
Control:		ficq-awr y ava	Delle si M
Shift In	1099 L	9	tions small
Shift Out			
Master Reset	From y time hour	but notes per	amit rijtus
Status:		SING TO THE	GILLO DAM
Input Ready	18048	12	0
Output Ready	se combut particular	13	0
Not Connected	ORIA regeat	14	90° LL - 11
Voltage:	CHO OF DELLOYS, I	919 El SI SI	REL BYC-3
V _{CC} (+5V)	1	15	V
Ground	gri of 1 stances		V

The corresponding list for the 67402 differs only in that there are five Data in lines rather than four, and five Output lines rather than four. The reason that there is an unused pin is that the

We now return to what happens when a new data word gets inserted at the "top" of the FIFO. A mark (call it a "one") is made in the presence bit for word 00, the first word. Assume now that word 01 is vacant, so that there is a "zero" in its presence bit. The internal logic of the FIFO then operates so that the data from word 00 is automatically written into word 01, the presence bit for word 01 is automatically set to "one," and the presence bit for word 00 is automatically reset to "zero." If word 02 is likewise vacant, the process gets repeated, and so forth until the same piece of data has settled into the lowest vacant word in the FIFO — the next lower word, and all the rest, have "ones" in their presence bits, blocking further changes.

Conversely, now assume that at the moment no data word is being input, but that one has just been output. Then the bottom word in the FIFO - word 63 - has a "zero" in its presence bit, but there are a number of other words above it which have "ones" in their presence bits. The data in word 62 then moves into word 63 in the same manner described above, and the data in word 61 moves into word 62, and so forth, until there is no longer any word in the FIFO having a "one" in its presence bit which is above a word having a "zero" in its presence bit. The effect is that of empty locations bubbling up to the top of the FIFO. Or, in case you are one of those elite individuals who has been exposed to the concepts and jargon of modern semiconductor theory, you may prefer to think of the FIFO operation as one in which data ("electrons") flow from the top of the FIFO to the bottom, and vacancies ("holes") flow from the bottom of the FIFO to the top. In the general case, of course, new data words are being input at the top and old ones are being output at the bottom at random times, and there is a dynamic and continually changing situation within the FIFO as the new data words drop towards the bottom and the vacancies bubble up towards the top, and they intermix along the way.

An obvious consequences of this manner of operation in shiftregister-technology FIFOs is that it takes guite a bit longer for a data word to pass all the way through the FIFO than the minimum time between successive input or output operations. There are various versions of the 67401 and 67402, rated at 5, 7, 10, 15, 16.7 or 35 MHz over commercial (0°C to +75°C) or military (-55°C to +125°C) temperature ranges. Thus, for instance, a 16.7-MHz FIFO can input data words at the top and/or output data words at the bottom at a sustained rate of a word every 60 nanoseconds. However, the "fall-through" time, tpT for these same FIFOs is stated in the data sheet as 1.3 microseconds, which is a long enough time for 24 words to be input or 24 words to be output! There is in principle also a "bubble-through" time for a single vacancy to travel from word 63 all the way back to word 00, which should be identical to tpt, and probably is although as measured on a semiconductor tester it may differ by as much as 50 nanoseconds, which is probably due to artifacts of measurement. By the way, the stated operating frequencies and the tpT value are "worst-case" (guaranteed) numbers; the "typical" values observed in actual parts are necessarily somewhat better, since semiconductor manufacturers are obliged to take any parts back which customers can prove do not meet the worst-case numbers, and some margin of safety is always nice.

Besides Monolithic Memories, other manufacturers of highspeed FIFOs include Fairchild Semiconductor, Mostek, National Semiconductor, RCA, Texas Instruments, and TRW LSI Products. MOS (slow) FIFOs are available from Advanced Micro Devices, Fairchild Semiconductor, Texas Instruments, Western Digital, Zilog, and probably other firms. FIFOs in development or available at just about all of these vendors also offer new bells and whistles which I haven't discussed, such as three-state outputs, serial (one-bit-at-a-time) as well as parallel data ports, and additional status flags. For instance, Monolithic Memories now has the 67413 FIFO which has a "half-full" flag which tells when half of the FIFO's words contain data, and also a second flag which indicates that the FIFO is either "almost full" (within 8 words of full) or: "almost empty" (within 8 words of empty), reminiscent of the "yellow warning interrupt" in Digital Equipment Corporation PDP-11 computers. This "almost-full/empty flag" can be used as an interrupt to a microprocessor to indicate that some action must be taken, and the microprocessor can then examine the "half-full flag" to see what it actually has to do.

There are also other design approaches to the insides of a FIFO besides the one based on shift-register technology which has been described here. For instance, a FIFO may be organized as a random-access memory ("RAM") with two counters capable of addressing the RAM right within the chip, an "in-pointer" and an "out-pointer." The counting sequences, of course, "wrap around" from the highest RAM address back to zero. The outpointer chases the in-pointer, the region just traversed by the inpointer but not yet by the out-pointer contains significant data, and the complementary region is logically "empty." This approach involves good news and bad news: the good news is that the long fall-through time goes away, but the bad news is that now reading and writing typically interfere with each other - unless the RAM is "two-port," they cannot be done simultaneously at all. Also, since this approach is more costly in "silicon area" than the shift-register approach, it would not result in as large FIFO capacities for the same size die or the same power consumption. In practice, this approach has only been used for MOS FIFOs which have turned out to be guite slow.

Another design approach is somewhat intermediate between the pure RAM approach as just described and the shift-register approach. It uses "ring counters" on the chip instead of full-blown binary counters. What this means in practice is that there are now two extra "tracks" along with the data tracks within the FIFO, plus also an input data bus and an output data bus. Single "one" bits move along the in-pointer track and the out-pointer track, and the out-pointer chases the in-pointer as before. The RAM is effectively two-port, and the two parallel buses both go to each and every word. Texas Instruments has announced some small (16x4) bipolar FIFOs based on this technical approach. Like the pure RAM approach, it gets rid of the fall-through time but needs proportionally more silicon area to store a given number of bits.

Designing with FIFOs

Returning now to the Monolithic Memories 67401 and 67402, if what you really need is a "deeper" FIFO, say 128x4 instead of just 64x4, these parts are designed to cascade using a simple "handshaking" procedure, without any external logic at all! If FIFO B follows FIFO A in the cascading sequence, the Shift In control input of FIFO B is connected to the Output Ready status output of FIFO A, and likewise the Shift Out control input of FIFO A is connected to the Input Ready status output of FIFO B, and the Master Reset control inputs are all tied together. (See Figure 3.) That's all there is to it. Any number of FIFOs may be cascaded in this manner.



"...THE MONOLITHIC MEMORIES C67401 AND C67402...ARE
DESIGNED TO CASCADE USING A SIMPLE 'HANDSHAKING'
PROCEDURE..."

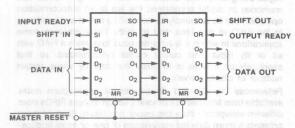


Figure 3. Cascading FIFOs to Form 128x4 FIFO

If what you really need is a "wider" FIFO, then you simply arrange 64x4 or 64x5 FIFOs side-by-side up to the required width. Then, you use an external AND gate such as a 74508 or 74S11 to AND the Input Ready signals of the first rank of FIFOs if there is more than one rank, or of the only rank of FIFOs if there isn't. (See Figure 12 in the FIFO data sheet.) Likewise, a similar AND gate is also needed to AND the Output Ready signals of the last rank of FIFOs. If you didn't provide these AND gates and just took the Input Ready signal of one FIFO as representative of when the whole array was ready, you would be taking the rather large gamble that you had correctly chosen the slowest row in this array — and if you chose wrongly, 4-bit or 5-bit chunks of your input word might not get read correctly into the FIFO where they were supposed to go. Ditto on the output side. So like use the AND gates.

Although a humungus number of 67401s and 67402s are in use world-wide giving hassle-free service, it should be kept in mind that these devices are asynchronous sequential circuits. (One definition of "asynchronous sequential circuit" is "a fortuitous collection of race conditions," but that definition is unduly sardonic for very carefully designed parts such as these.) If your board is subject to noise, or if certain data sheet setuptime and hold-time conditions are occasionally not met, errors may occur. It is prudent system-design practice to every so often allow an array of FIFOs to empty out completely, and then issue a Master Reset. (I'm assuming, of course, to start with that you're not the kind of turkey who has to be told to issue a Master Reset as part of your power-up sequence.) In the event that you still get what appear to be occasional errors. very small (say from 22 to 68 picofarads) capacitors from both the Shift In control input and the Shift Out input of a FIFO to

ground will often eliminate these. But by all means start with a good circuit board — these are high-speed-Schottky-technology circuits, and like to see a lot of ground-plane metal on the board, along with other reputable interconnection practices such as 0.1-microfarad disk capacitors between V_{CC} and ground for each chip to bypass switching noise.

The sequence of events which occurs during the operation of shifting a new data word into the "top" of a FIFO is shown in Figure 3 in the FIFO data sheet, and the corresponding sequence of events for shifting out the bottom word is shown in Figure 7 in the FIFO data sheet. In both of these figures, it has been assumed that the external logic — whether it be the rest of your system, or just another FIFO — refrains from raising the respective Shift line to HIGH until the respective Ready line has gone HIGH. If the Shift line is raised any earlier, it simply gets ignored.

When two FIFOs are cascaded as shown in Figure 3, the sequences of events shown in data-sheet Figures 3 and 7 are subject to the additional ground rule that the Output Ready line of the FIFO on the left in Figure 3 (call it "FIFO A") is identically the Shift In line of the FIFO on the right (call it "FIFO B"). And likewise, the Input Ready line of FIFO B is identically the Shift Out line of FIFO A. In the terminology we have been using. FIFO A is the "upper" FIFO and FIFO B is the "lower" FIFO. Although you do not normally need to be concerned about what happens when two FIFOs are hooked together for cascaded operation in this manner, since the "handshake" occurs quite automatically without the rest of your logic having to do anything to make it happen, it is an illuminating exercise to consider data-sheet Figures 3 and 7 together in this light and see why the cascading works.

In the general case, both FIFO A and FIFO B are neither completely full nor completely empty. Thus, from the description already given of FIFO internal operation, after some period of time there will be a significant piece of data in word 63 or FIFO A and a "one" in the presence bit for that word. Since the word-63 presence bit is what controls the Output Ready signal, the latter will at some point in time go HIGH and at that same point in time the data word in FIFO A word 63 is present at the output lines. Likewise, after some period of time there will be a vacancy in word 00 of FIFO B, and a "zero" in the presence bit for that word which in turn results in the Input Ready signal going HIGH. Remembering now that each of these Ready signals is in fact the respectively-opposite Shift signal for the other FIFO, it may be seen from data-sheet Figure 3 that the conditions for inputting a word into FIFO B have now been met, and from data-sheet Figure 7 that the conditions for outputting a word from FIFO A and allowing the next available piece of data from somewhere further "up" in FIFO A to enter FIFO A word 63 have also been met. The time delays shown in both data-sheet Figure 3 and data-sheet Figure 7 from the event at 2 to the event at 3, and from the event at 4 to the event at 5A, are asynchronous internallogic-determined times of the order of four or five gate delays, where the gates in question are high-speed-Schottky LSI internal gates and have significantly less propagation delay than the SSI gates you can read about in data sheets.

Returning now to applying the timing analysis shown in datasheet Figures 3 and 7 to the case of FIFO A and FIFO B operating in cascaded mode, notice that each movement (rising or falling) of the Ready signal for one FIFO is activated by the movement in

..... une outer part. The two signals, Onzvoid (meaning Output Ready A" which is the same signal as "Shift In B") and IRB/SOA, cannot both remain HIGH at the same time for more than a few nanoseconds, since if they are both HIGH a data word will pass between the two FIFOs as already described. So, at the point when both the sequence of events shown in data-sheet Figure 3 and the sequence of events shown in data-sheet Figure 7 have been completed, and consequently ORA/SIB and IRB/-SOA have both gone HIGH again, another similar sequence of events occurs for both FIFOs and another word is passed, and so forth. This process continues apace until either ORA/SIB sticks LOW, which can happen if FIFO A gets completely emptied out of data words and has "zeroes" everywhere in its presence track; or until IRB/SOA sticks LOW, which can likewise happen if FIFO B gets completely filled and has "ones" everywhere in its presence track. When such a deadlock situation occurs, it lasts until a new data word has been input into FIFO A and has had time to "fall all the way through" and settle into FIFO A word 63, or until the data word in word 63 of FIFO B has been read out and the resulting vacancy has had time to "bubble all the way back up" into FIFO B word 00, as the case may be.

Various Uses for FIFOs

The classical FIFO application, as already mentioned at the beginning of this paper, is that of matching the instantaneous data rates of two digital systems in a simple, economical way. One of the two systems may, for reasons of design economics or even of utter necessity, want to emit or absorb data words in ultra-high-speed bursts, whereas the other one may prefer to operate at a slow-but-steady data rate or even at an erratic rate which varies between ultra-slow and slow or even between slow and fast. No matter — it's all the same to an asynchronous FIFO such as the 67401 or 67402, as long as the input rate and the output rate do match up over a long period of time so that it neither fills up nor empties out.

There are, however, some additional uses for FIFOs which arise from other, rather different circumstances. For instance, your digital system may simply need some extra buffer storage scattered around locally at different points on your block diagram, and you and your system may really just not care whether this storage is accessed on a random or on a queue basis. Under these circumstances, it is ordinarily less hassle to use a FIFO than to use a small RAM and come up with some extra logic to generate addresses and timing signals for it. Often the FIFO modus operandi is in fact the natural one for the application; as for instance when your system must accumulate a block of 64 characters and then run them by all at once in order to examine them for the presence of some control character, using some scanning logic - or perhaps even a microprocessor - which is otherwise occupied most of the time

A less obvious but interesting application of FIFOs is as automatic "bus-watchers" for jump-history recording for hardware or even software diagnostic purposes. A FIFO whose inputs are connected to a minicomputer's program counter or microprogram counter, or to a microcomputer's main address bus, may be operated so as to record every new jump address generated by the program. This way, if at some point the hardware freaks out or the operating system crashes, a record exists of the last 64 jumps which were taken before the system was halted, assuming of course that you have provided some

happened just before everything went haywire. FIFOs may be used in this way either as part of built-in self-monitoring features in digital systems, or as part of various kinds of external test equipment.

FIFOs may also be used as controllable delay elements for digital information which cannot be used immediately upon receipt — perhaps it must be matched against other information which is not yet available, or perhaps it must be synchronized with other streams of information which are out of phase by a varying amount. An example of the latter situation is deskewing several bit-streams off a parallel-format magnetic tape, which commonly has to be done when high recording densities are used. One FIFO per bit-stream is required - but the net resulting logic may still be the most reliable and economical way to get the job done, when compared with other possible digital designs. Another example is that of using FIFOs as data memories in digital correlators; the lag in an autocorrelation operation can be set simply by controlling how many words are in the FIFO at one time, and so forth. There are even some applications in which it is advantageous to operate a FIFO with all of its input and output cycles synchronized, so that absolutely all it does is to delay the data by some certain number of clock intervals.

References (1), (2), and (3) are formal applications notes available from Monolithic Memories, which discuss FIFOs from different viewpoints than this paper has taken. Each of them presents a more detailed explanation of one or more applications than there has been room for here. Reference (1) is mainly an overall applications survey, reference (2) emphasizes digital communications, and reference (3) emphasizes digital spectrum analyzers and also includes an overview of digital signal processing in general.



"A LESS OBVIOUS BUT INTERESTING APPLICATION OF FIFOS IS AS AUTOMATIC 'BUS-WATCHERS' . . . "

References

- "First In First Out Memories...Operations and Applications," applications note published March 1978 by Monolithic Memories Inc. and being reissued.
- (2) "Understanding FIFO's," applications note published by Monolithic Memories Inc. The author, Alan Weissberger, has also gotten a modified version of this note published as a magazine article, "FIFOs Eliminate the Delay when Data Rates Differ," in *Electronic Design*, November 27, 1981, Despite the general title, the emphasis is on digital communications applications.
- (3) "PROMs, PALs, FIFOs and Multipliers Team Up to Implement Single-Board High-Performance Audio Spectrum Analyzer," applications note published by Monolithic Memories Inc. The author, Richard Wm. Blasco, also got this note published in *Electronic Design* in two installments, in the issues of August 20 and September 3, 1981 under the titles "PAL Shrinks Audio Spectrum Analyzer" and "PAL Improves Spectrum Analyzer Performance" respectively.

8

Asynchronous First-In First-Out Memory (FIFO) 16x5 74S225/A

Features/Benefits

- . DC to 20-MHz shift-in/shift-out rates
- · Fully expandable by word width and depth
- Three-state outputs
- TTL-compatible inputs and outputs
- Functionally compatible with T.I. SN74S225
- · Designed for extended testability

Description

The 74S225/A is a Schottky-clamped transistor-transistor logic (STTL) 16x5 First-In-First-Out memory (FIFO) which operates from DC to 10/20 MHz. The data is loaded and emptied on a

Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
74S225	J, N	10 MHz Com
74S225A	J, N	20 MHz Com

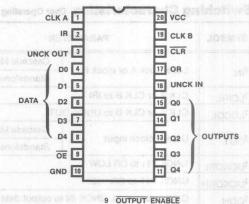
first-in-first-out basis through asynchronous input and output ports. These devices are used in digital systems performing data transfers when source and receiver are not operating at the same data rate. FIFOs are also used as data buffers where the source and receiver are not operating at the same time. Both word length and FIFO depth are expandable. Unload clock output (Pin 3) is designed for testability of V_{OL}.

Pin Names

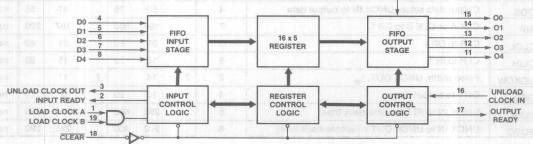
PIN#	PIN NAME	DESCRIPTION
1	CLK A	Load clock A
2	IR	Input ready
3	UNCK OUT	Unload clock output
4-8	D0-D4	Data inputs
9	ŌĒ	Output enable
10	GND	Ground pin
11-15	Q4-Q0	Data outputs
an 16 88	UNCLK IN	Unload clock input
20 17 OA	OR	Output ready
18	CLR	Clear
19	CLK B	Load clock B
20	Vcc	Supply voltage

Pin Configuration

74S225/A . . J or N Package (Top View)



Block Diagram



TWX: 910-338-2376 2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2374



Absolute Maximum Ratings

Supply voltage V _{CC}	0.5 V to 7 V
Input voltage	1.5 V to 7 V
Off-state output voltage	0.5 V to 5.5 V
Storage temperature	65 to +150°C

Operating Conditions

SYMBOL	PARAMETER	FIGURE	74S225 MIN TYP MAX	74S225A MIN TYP MAX	UNIT
VCC	Supply voltage		4.75 5.25	4.75 5.25	V
t _A	Operating free-air temperature		0 75	0 75	°C
tLCKH	LOAD CLOCK pulse width, A or B, tw (HIGH)	2	25	22 36	ns
tIDS	Setup time, data to load clock	2	-201*	-201*	ns
^t IDH	Hold time, data from load clock	2	70t	501	ns
tUCKL	UNLOAD CLOCK INPUT pulse width, tw (LOW)	a no 4ellam	data a debes a simb	7 SHIM 02 01 36	ns
tCLW	CLEAR pulse width, t _W (low)	2	40	20	ns
tCLCK	Setup time, clear release to load clock, t _{SU}	2	251	10	ns

^{*} Data must be setup within 20 ns after valid Load Clock (A or B) pulse (positive transition).

Switching Characteristics Over Operating Conditions

SYMBOL	PARAME	TER	FIGURE	74S22S MIN TYP	MAX	74S225 MIN TYP	To a second	UNIT
	Annual pool pool	Cascade Mode**	ni ni	(Braund u		CIAD -		
fIN	Load clock A or clock B	Standalone Mode	2	10 20		20 22		MHz
tLCIRL	CLK A or CLK B to IRI **	on 3 Alleo	nug2i doc	0 baoint 55	75	43	55	ns
tLCCOL	CLK A or CLK B to UNCK (2 ///	25	50	31	40	ns
four	Unload clock input	Cascade Mode***	4	40	FT	20 22	8	MHz
		Standalone Mode		10 20		20 22		
tuckorl.	UNCK IN I to OR LOW		4	30	45	26	35	ns
^t UCKORH	UNCK IN 1 to OR HIGH		4	40	60	32	45	ns
todh	Output data hold, UNCK IN to output data		4	20 50		20 30	alū :	ns
tods	Output data setup, UNCK II	N to output data	4	50	75	41	55	ns
t _{RIP}	CLK A or CLK B to OR 1		7	190	300	167	220	ns
tCLOL	CLR to OR I	18 ST	6	35	60	31	40	ns
^t CLIH	CLR to IR f		6	16	35	15	20	ns
tuckow	Pulse width, UNCK OUT, tv	v	2	7 14		7 11		ns
tORD	OR † to output data	Karakaan	4	10	20	9	15	ns
^t BUBI	UNCK IN to IR 1 (bubble-ba	ack time)	8	255	400	214	290	ns
t _{BUBC}	UNCK IN to UNCK OUT 1 ((bubble-back time)	8	270	400	226	290	ns

Arrow indicates that it is referenced to the high-to-low transition.

^{† =} Arrow indicates that it is referenced to the o-high transition.

^{** 16}th word only

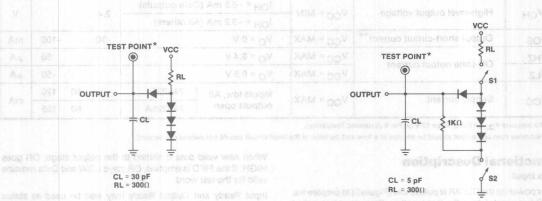
^{***} Devices connected to provide FIFO of greater than 16 word depth.

Switching Characteristics Over Operating Conditions and and an included an included and an included and an included and an included an included and an included an included and an included an included an included and an included an included and an included an

SYMBOL	PARAMETER PARAMETER	FIGURE	74S225 MIN TYP	MAX	74S225 MIN TYP	MAX	UNIT
t _{PHZ}	Output disable delay, \overline{OE} to Q _i , C _L = 5 pF	1	10	25	8	25	ns
tPLZ			10	-25	18	25	
tPZL	Output enable delay, $\overline{\sf OE}$ to Q _i , C _L = 5 pF	100	7.05	40	19	40	ns
t _{PZH}		YCC - MAK	25	40	23	40	

Test Load for Bi-State Output

Test Load for Three-State Output



* The "TEST POINT" is driven by the output under test, turning O years a second of the control o

Input Pulse Amplitude = 3.0 V Input Rise and Fall Time (15%–90%) = 2.5 ns Measurements made at 1.5 V

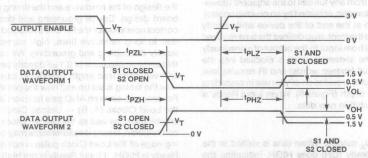


Figure 1. Enable and Disable

Waveform 1 is for an output with internal conditions such that the output is low except when disabled.

Waveform 2 is for an output with internal conditions such that the output is high except when disabled.

SYMBOL	PARAME	TER	TEST CONDITIONS			MIN TYP	MAX	UNIT		
VIL	Low-level input v	oltage				in of the section	0.8	V		
VIH	High-level input	voltage		ع _{ار} در - 6 و3	or 90 velebald	2.0		V		
VIC	Input clamp volta	age	V _{CC} = MIN	I _I = -18 mA			-1.5	V		
hL1	Low-level	D ₀ -D ₄	V _{CC} = MAX	V ₁ = 0.5 V = 10 nO or 30 , when std		Voc = MAX		Cutput ena	-1	mA
I _{IL2}	input current	All others	.00				25	mA		
	High level input	ourrant.	V MAY	Data inputs			40	^		
IH	High-level input	current	V _{CC} = MAX	V _I = 2.7 V Others			25	μΑ		
-I _I	Maximum input	current	V _{CC} = MAX	V _I = 5.5 V			1	mA		
V/	KING STATE	rational than a	1801 1081	I _{OL} = 16 mA (Data outputs)		1415 TOT	0.5	V		
VOL	Low-level output	voitage	V _{CC} = MIN	I _{OL} = 8 mA (All o	others)		0.5	V		
14	Liberta Laval avidavi	aval autaut valtaga		I _{OH} = -6.5 mA (I	Data outputs)	2.4		V		
VOH	High-level outpu	t voitage	V _{CC} = MIN	I _{OH} = -3.2 mA (A	All others)	2.4		V		
los	Output short-circ	cuit current**	V _{CC} = MAX	V _O = 0 V		-30	-100	mA		
IHZ	Off state suitant	HOS TEST	V _{CC} = MAX	V _O = 2.4 V			50	μΑ		
ILZ	Off-state output	current	V _{CC} = MAX	V _O = 0.5 V	an Š		-50	μΑ		
	Supply autont	A TURN	V - MAY	Inputs low, All	74S225	80	120	m A		
lcc	Supply current		V _{CC} = MAX	outputs open	74S225A	80	125	mA		

* To measure VOL on Pin 3, force 10 V on Pin 9 (Extended Testability).

** Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

Functional Description

Data Input

After power up the CLEAR is pulsed low (Figure 5) to prepare the FIFO to accept data in the first location. Clear must be applied prior to use to ensure proper operation. When Input Ready (IR) is HIGH, the first location is ready to accept data from the Dy inputs. Data then present at the data inputs is entered into the first location when both Load Clocks (CLK A and CLK B) are brought HIGH. The CLK A HIGH and CLK B HIGH signal causes the IR and UNCK OUT to pulse LOW. Once data is entered into the first cell, the transfer of data from any full cell to the adjacent (downstream) empty cell is automatic, activated by an on-chip control. Thus data will stack up at the end of the device while empty locations will "bubble" to the front, trup defines the time required for the first data to travel from input to the output of a previously empty device. When the sixteenth word is clocked into the device, the memory is full (sixteen words) and IR remains low. The Unload Clock Output is provided chiefly for use in cascading devices to extend FIFO depth (Figure 9). When Input Ready is Low, do not attempt to shift-in new data.

Data Output

Data is read from the Q_X outputs. When data is shifted to the output stage, Output Ready (OR) goes HIGH, indicating the presence of valid data. When the OR is HIGH, data may be shifted out by bringing the Unload Clock Input (UNCK IN) LOW. A LOW signal at UNCK IN causes the OR to go LOW. Valid data is maintained while the UNCK IN is LOW. When UNCK IN is brought HIGH the upstream data, provided that stage has valid data, is shifted to the output stage.

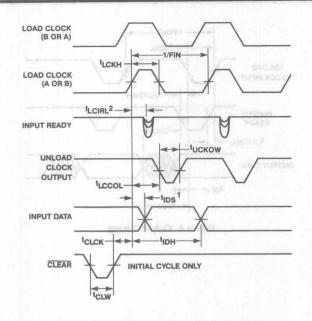
When new valid data is shifted to the output stage, OR goes HIGH. If the FIFO is emptied, OR stays LOW and Data remains valid for the last word.

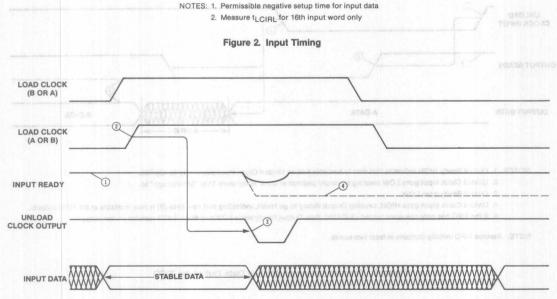
Input Ready and Output Ready may also be used as status signals indicating that the FIFO is completely full (Input Ready stays LOW for at least tbub) or completely empty (Output Ready stays LOW for at least trip).

AC Test and High-Speed App. Notes

Since the FIFO is a high-speed device, care must be exercised in the design of the hardware and the timing utilized within the PC board design. Device grounding and decoupling is crucial to correct operation as the FIFO will respond to very small glitches due to long reflective lines, high capacitances and/or poor supply decoupling and grounding. We recommend a monolithic ceramic capacitor of 0.1 µF directly between V_{CC} and GND with very short lead length. In addition, care must be exercised in how the timing is set up and how the parameters are measured. For example, since an AND gate function is associated with both the Load Clocks (A, B) — Unload Clock Output-Input Ready combination, as well as the Unload Clock Input-Output Ready combination, timing measurements may be misleading, i.e., rising edge of the Load Clock pulse is not recognized until Input Ready is HIGH. If Input Ready is not high due to (a) too high a frequency, or (b) FIFO being full or affected by (CLR), the LOAD-CK activity will be ignored. This will affect the device from a functional standpoint, and will also cause the "effective" timing of Input Data Hold time (tIDH) and the next activity of Input Ready (tLCIRL) to be extended relative to Load Clock (A or B) going HIGH







- NOTES: 1. Input Ready HIGH indicates space is available and a Load Clock (A and B) pulse may be applied.
 - 2. Input Data is loaded into the first word.
 - Unload Clock Output pulses indicating the first word is full and the Data from the first word is released for "fall-through" to second word.
 - 4. If the second word is already full, then the data remains at the first word. Since the FIFO is now full, Input Ready remains LOW.

Figure 3. The Mechanism of Clocking Data into the FIFO

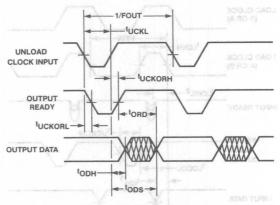
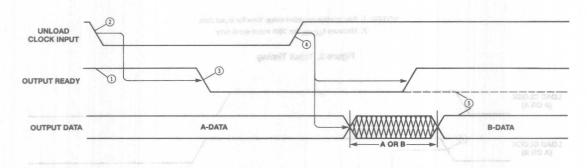


Figure 4. Output Timing

WITHING BLOYD LIATER



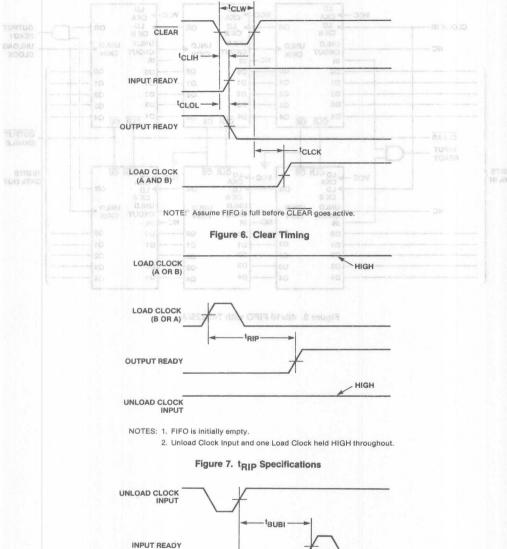
NOTES: 1. Output Ready HIGH indicates that data is available and an Unload Clock Input pulse may be applied.

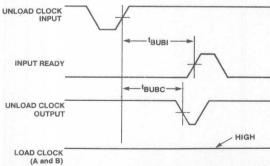
- 2. Unload Clock Input goes LOW creating an empty position at word 16 for word 15 to "fall-through" to.
- 3. Output Ready goes LOW.
- 4. Unload Clock Input goes HIGH, causing Output Ready to go HIGH, indicating that new data (B) is now available at the FIFO outputs.
- 5. If the FIFO has only one word loaded (A-DATA), then Output Ready stays LOW and the A-DATA remains on the outputs.

NOTE: Assume FIFO initially contains at least two words.

Figure 5. The Mechanism of Shifting Data Out of the FIFO







NOTES: 1. FIFO is initially full.

2. Load Clock (A and B) held HIGH throughout.

Figure 8. t_{BUBI}, t_{BUBC} Specifications

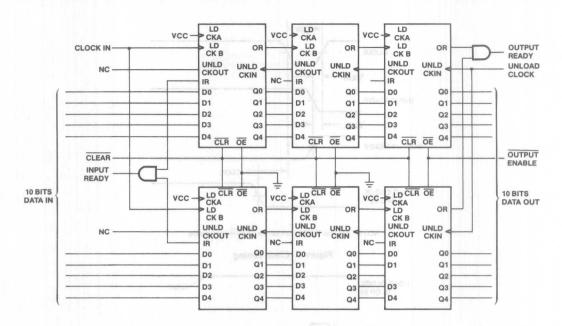


Figure 9. 48x10 FIFO with 74S225/A

First-In First-Out (FIFO) 64x4 64x5 **Cascadable Memory**

C5/67401 C5/67401A C67401B C5/67402A C5/67402 C67402B

Features/Benefits

- . Choice of 16.7, 15 and 10 MHz shift-out/shift-in rates
- Choice of 4-bit or 5-bit data width
- TTL inputs and outputs
- . Readily expandable in the word and bit dimensions
- · Structured pinouts. Output pins directly opposite corresponding input pins
- · Asynchronous operation
- Pin-compatible with Fairchild's F3341 MOS FIFO and many times faster

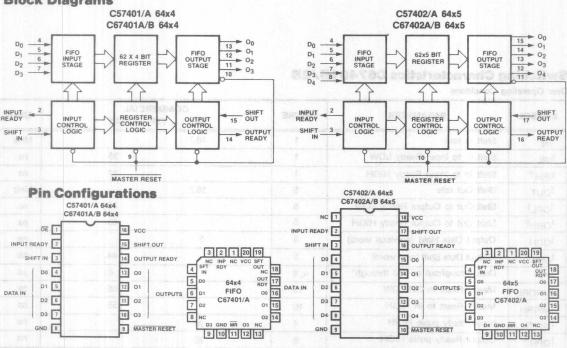
Description

The C5/C67401B/2B/1A/2A/1/2 are "fall-through" high speed First-In First-Out (FIFO) memory organized 64 words by 4 bits and 64 words by 5 bits respectively. A 16.7 MHz data rate allows usage in digital video systems; a 15 MHz data rate allows usage in high speed tape or disc controllers and communications buffer applications. Both word length and FIFO depth are expandable.

Ordering Information

PART NUMBER	PKG	TEMP	DESCRIPTION
C57401	J(20)(L)	Mil	7 MHz 64x4 FIFO
C67401	J,N,NL(20)	Com	10 MHz 64x4 FIFO
C57402	J(20)(L)	Mil	7MHz 64x5 FIFO
C67402	J,N,NL(20)	Com	10 MHz 64x5 FIFO
C57401A	J,(20)(L)	Mil	10 MHz 64x4 FIFO
C67401A	J,N,NL(20)	Com	15 MHz 64x4 FIFO
C57402A	J,(20)(L)	Mil	10 MHz 64x5 FIFO
C67402A	J,N,NL(20)	Com	15 MHz 64x5 FIFO
C67401B	J	Com	16.7 MHz 64x4 FIFO
C67402B	J	Com	16.7 MHz 64x5 FIFO

Block Diagrams



Monolithic Memories TWX: 910-338-2376

Cascadable Memory

Absolute Maximum Ratings

	ACA CE/STACIA CETACIE	
Off-state output voltage	402 CE/67402A C67402B	-0.5 V to 5.5 V

Operating Conditions C67401B/2B

SYMBOL	PARAMETER	FIGURE	COMMERCIAL MC-4 to MG-5 to 6	UNIT
V _{CC}	Supply voltage	tostag	4.75 lid o 5 lino 5.25 i old hinages y	V
T _{A RIA} as	Operating free-air temperature	2011/20	ured binoutis. C 75 ut plus directly or 0 cells corres-	°C
t _{SIH} †	Shift in HIGH time	one same	18	ns
tSIL_	Shift in LOW time	A PARK SACA	.18	ns
tIDS	Input data setup	1	0 19596	ns
tIDH	Input data hold time	1	40	ns
t _{SOH} †	Shift Out HIGH time	- 5	C674018/2B/1A/2A/1/2 are "fall-th 8fgh" high speed	ao ns
tsol	Shift Out LOW time	-5	merchal and show 18 words by 4 bits	ns
tMRW	Master Reset pulse	10	digital video systems; a 15 MHz datides allows usage	ns
tMRS	Master Reset to SI	10	refred another in 35 map by a delication sold to equal beeq	ns

Switching Characteristics C67401B/2B

CS7402/A S4x5 CS7402A/S S4x5

Over Operating Conditions

ci operam	9 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7	discourse and the control of the con					
SYMBOL	PARAMETER TURK	FIGURE	COMMERCIAL MIN TYP MAX	UNI			
fIN	Shift in rate	1	YGA34 87 16.7	MHz			
^t IRL	Shift In to Input Ready LOW	1	35	ns			
t _{IRH} †	Shift In to Input Ready HIGH	1	37	ns			
four	Shift Out rate	5	16.7	MHz			
tORL†	Shift Out to Output Ready LOW	5	38 9 4179478	ns			
tORH†	Shift Out to Output Ready HIGH	5	48	ns			
todh	Output Data Hold (previous word)	5	5 700 1988 609	ns			
tods	Output Data Shift (next word)	5	190 Joy Sur die 38 X2483 VINTED 52 44	ns			
tpT	Data throughput or "fall through"	4, 8	1.45	μς			
^t MRORL	Master Reset to OR LOW	10	55	ns			
^t MRIRH	Master Reset to IR HIGH	10	55	ns			
t _{IPH} *	Input Ready pulse HIGH	4	20	ns			
tOPH*	Output Ready pulse HIGH	8	20	ns			

[†]See AC test and High Speed application note.

^{*}This parameter applies to FIFOs communicating with each other in a cascaded mode.

Absolute Maximum Ratings

Supply voltage V _{CC} -0.5 V to	7 V
Input voltage	7 V
Off-state output voltage -0.5 V to 5	5.5 V
Storage temperature -65° to +15	0°C

Operating Conditions C5/C67401A/2A

SYMBOL	PARAMETER	FIGURE	MILIT MIN TY		COMMERCIAL MIN TYP MAX	UNIT
Vcc	Supply voltage		4.5	5 5.5	4.75 5 5.25	V
TA	Operating free-air temperature	88	-55	*125	0 blod slep tugitl 75	°C
tSIH†	Shift in HIGH time	1	35		23	ns
^t SIL	Shift in LOW time	1	35		25 WOLLDO MAD	ns
t _{IDS}	Input data setup	08 1	0		e Our reset notes M	ns
t _{IDH}	Input data hold time	8a 1	45		40 pessel rotestyl	ns
tson+	Shift Out HIGH time	5	35		23	ns
tSOL	Shift Out LOW time	5	35		25	ns
^t MRW	Master Reset pulse	10	40	745 SOI	35	ns
^t MRS	Master Reset to SI	10	45		35	ns

^{*}Case temperature.

Switching Characteristics C5/C67401A/2A Over Operating Conditions of the last state of the last state

SYMBOL	PARAMETER	FIGURE	MIN	MILITARY TYP MAX	COMMERCIAL MIN TYP MAX	UNIT
fIN	Shift in rate	Or 1	10	evious word)	15 835G USTUO	MHz
t _{IRL} †	Shift In to Input Ready LOW	1		50	n/ Ain2 ais0 juqtuO 40	ans a
t _{IRH} †	Shift In to Input Ready HIGH	1	1	50	no fugnoucini stsG 40	ns
four	Shift Out rate	5	10	NOT	10 15 Israel Literal 1	MHz
tORL†	Shift Out to Output Ready LOW	5	1	65	191 of 16-201 1 29M 45 F	ns
tORH [†]	Shift Out to Output Ready HIGH	06 5		65	eally valor lugal 50	ns
todh	Output Data Hold (previous word)	06 5	10	HOH	Paulo (back many)	ns
tods	Output Data Shift (next word)	5		60	on rollsollage benig 19 rig H 45 mm	ns
t _{PT}	Data throughput or "fall through"	4, 8	ioaurouse.	2.2	1.6	μS
^t MRORL	Master Reset to OR LOW	10		65	60	ns
^t MRIRH	Master Reset to IR HIGH	10	1/2	65	60	ns
tIPH*	Input Ready pulse HIGH	4	30		23	ns
tOPH*	Output Ready pulse HIGH	8	30	1291 tollary regi	23 c novins a "TUICH TEST"	ns

[†] See AC test and High Speed application note.

^{*} This parameter applies to FIFOs communicating with each other in a cascaded mode.

Input voltage	-1.5 V to 7 V
Off-state output voltage	-0.5 V to 5.5 V
Storage temperature	55° to +150°C

Operating Conditions C5/C67401/2

SYMBOL	PARAMETER	FIGURE	MIN	MILITAR' TYP	MAX	MIN	MMERC TYP	MAX	UNIT
V _{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
TA	Operating free-air temperature		-55	UPEC	* 125	0	TENTO-	75	°C
tSIH†	Shift in HIGH time	1	45		REF	23			ns
tSIL	Shift in LOW time	1	45		pp-t-attacks	35			ns
tIDS	Input data setup	1	0			0	For year	Mal	ns
^t IDH	Input data hold time	689 1	55	9	THE TOO CO	45	erating	40	ns
t _{SOH} †	Shift Out HIGH time	5	45			23	28 Pt 10	ne .	ns
tSOL	Shift Out LOW time	5	45			35	UJ ne ste	12	ns
†MRW	Master Reset pulse	10	30	1		35	stan to	119	ans
tMRS	Master Reset to SI	10	45			35	BIRD An	301	ns

^{*}Case temperature.

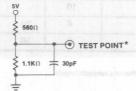
Switching Characteristics C5/C67401/2 Over Operating Conditions

SYMBOL	PARAMETER	FIGURE	MIN	MILITARY TYP MAX	CO	MMERCIAL TYP MAX	UNIT
fIN	Shift in rate	1	7	- 111	10	TTT WAA	MHz
t _{IRL} †	Shift In to Input Ready LOW	1		60		45	ns
t _{IRH} †	Shift In to Input Ready HIGH	1		60		45	ns
four	Shift Out rate	5	7	red CB/CdT	10	nind Chara	MHz
tORL†	Shift Out to Output Ready LOW	5		65		55	ns
tORH [†]	Shift Out to Output Ready HIGH	5 5	UON	70	PARAIR	60	ns
todh	Output Data Hold (previous word)	5	10		10	to all things	ns
tods	Output Data Shift (next word)	5		65	Indet Po	55	ns
tpT	Data throughput or "fall through"	4, 8		4	elet suceri	or at these 3	μS
^t MRORL	Master Reset to OR LOW	10		65	sim	100 may 60	ns
t _{MRIRH}	Master Reset to IR HIGH	10		WOJ 65	banió el	60	ns
t _{IPH} *	Input Ready pulse HIGH	4	30	HOU year	23	NO MINE	ns
tOPH*	Output Ready pulse HIGH	8	30	Torrow eustvo	23	od fuctor	ns

[†] See AC test and High Speed application note.

Test Load

* The "TEST POINT" is driven by the output under test, and observed by instrumentation.



Input Pulse 0 to 3 V Input Rise and Fall Time (10% - 90%) 5 ns minimum Measurements made at 1.5 V

^{*}This parameter applies to FIFOs communicating with each other in a cascaded mode.

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAM	ETER	1	TEST CONDITIONS	MIN TYP	MAX	UNIT
VIL	Low-level input	voltage	and	Annual money		0.8†	V
VIH	High-level input	voltage			2†		V
VIC	Input clamp vol	tage	V _{CC} = MIN	I ₁ = -18mA	Andreas de la constantina della constantina dell	-1.5	V
I _{IL1}	Low-level	D ₀ -D _n , MR	V MANY	V ₁ = 0.45V		-0.8	mA
IL2	input current	SI, SO	V _{CC} = MAX	V ₁ = 0.45V		-1.6	mA
-ЧН	High-level input	current	V _{CC} = MAX	V ₁ = 2.4V	and the second	50	μА
II.	Maximum input	current	VCC = MAX	V ₁ = 5.5V		1	mA
VOL	Low-level output voltage		V _{CC} = MIN	I _{OL} = 8mA		0.5	V
VOH	High-level outpu	ut voltage	V _{CC} = MIN	I _{OH} = -0.9mA	2.4		V
los	Output short-cir	rcuit current *	V _{CC} = MAX	V ₀ = 0V	-20	- 90	mA
		The second of		C5/67401		160	1 1 1
jamen			V _{CC} = MAX	C5/67402	J	180	
Icc	Supply current			C67401A	1 th - 1	170	1 .
- 00	No agreement to the wife of		Inputs low, outputs open	C6702A		190	mA
			outputs open	C67401B, C57401A		180	
				C67402B, C57402A		200	TURN

^{*}Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
†There are absolute voltage with respect to device GND (Pin 8 or 9) and includes all overshoots due to test equipment

Functional Description

Data Input

After power up the Master Reset is pulsed low (Fig. 10) to prepare the FIFO to accept data in the first location. When Input Ready (IR) is HIGH the location is ready to accept data from the $D_{\rm X}$ inputs. Data then present at the data inputs is entered into the first location when the Shift In (SI) is brought HIGH. A SI HIGH signal causes the IR to go LOW. Data remains at the first location until SI is brought LOW. When SI is brought LOW and the FIFO is not full, IR will go HIGH, indicating that more room is available. Simultaneously, data will propagate to the second location and continue shifting until it reaches the output stage or a full location. The first word is present at the outputs before a shift out is applied. If the memory is full, IR will remain LOW.

Data Transfer

Once data is entered into the second cell, the transfer of any full cell to the adjacent (downstream) empty cell is automatic, activated by an on-chip control. Thus data will stack up at the end of the device while empty locations will "bubble" to the front. tp¬ defines the time required for the first data to travel from input to the output of a previously empty device.

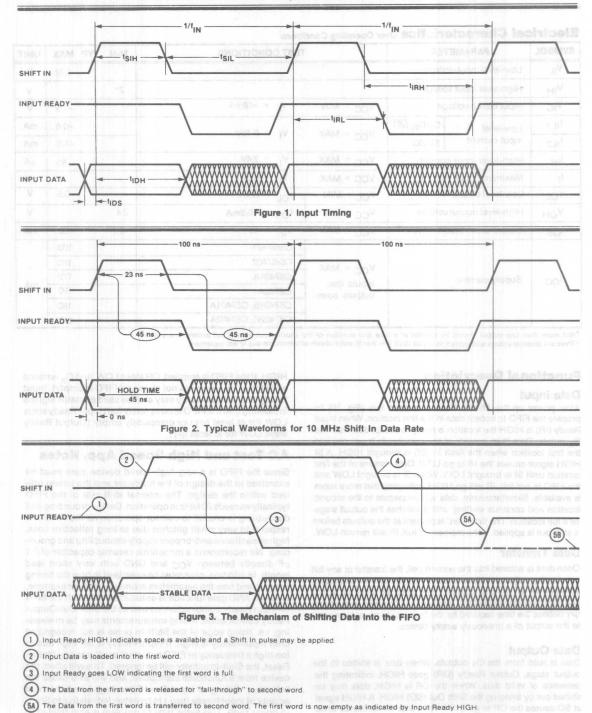
Data Output

Data is read from the O_X outputs. When data is shifted to the output stage, Output Ready (OR) goes HIGH, indicating the presence of valid data. When the OR is HIGH, data may be shifted out by bringing the Shift Out (SO) HIGH. A HIGH signal at SO causes the OR to go LOW. Valid data is maintained while the SO is HIGH. When SO is brought LOW the upstream data, provided that stage has valid data, is shifted to the output stage. When new valid data is shifted to the output stage, OR goes

HIGH. If the FIFO is emptied, OR stays LOW, and O_X remains as before, (i.e. data does not change if FIFO is empty). Input Ready and Output Ready may also be used as status signals indicating that the FIFO is completely full (Input Ready stays LOW for at least tp_T) or completely empty (Output Ready stays LOW for at least tp_T).

AC Test and High Speed App. Notes

Since the FIFO is a very-high-speed device, care must be exercised in the design of the hardware and the timing utilized within the design. The internal shift rate of the FIFO typically exceeds 20 MHz in operation. Device grounding and decoupling is crucial to correct operation as the FIFO will respond to very small glitches due to long reflective lines. high capacitance and/or poor supply decoupling and grounding. We recommend a monolithic ceramic capacitor of 0.1 μF directly between VCC and GND with very short lead length. In addition, care must be exercised in how the timing is set up and how the parameters are measured. For example, since an AND gate function is associated with both the Shift In-Input Ready combination, as well as the Shift Out-Output Ready combination, timing measurements may be misleading, i.e. rising edge of the Shift-In pulse is not recognized until Input-Ready is High. If Input-Ready is not high due to too high a frequency or FIFO being full or affected by Master Reset, the Shift-In activity will be ignored. This will affect the device from a functional standpoint, and will also cause the "effective" timing of Input Data Time (tIDH) and the next activity of Input Ready (tIRL) to be extended relative to Shift-In going High. This same type of problem is also related to tIRH, tORL and tORH as related to Shift-Out.



(58) If the second word is already full then the data remains at the first word. Since the FIFO is now full Input Ready remains low.

NOTE: Shift In pulses applied while Input Ready is LOW will be ignored (See Figure 4).



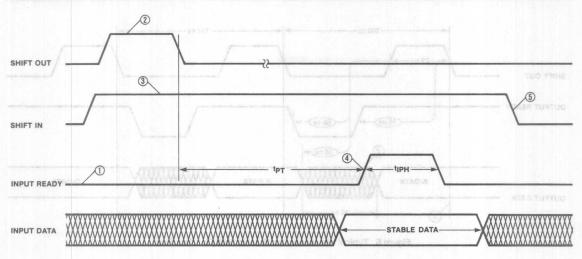
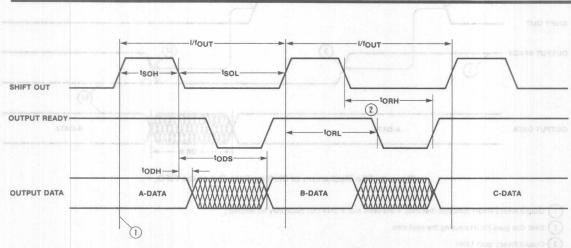


Figure 4. Data is Shifted in Whenever Shift In and Input Ready are Both HIGH

- (1) FIFO is initially full.
- 2) Shift Out pulse is applied. An empty location starts "bubbling" to the front.
- 3 Shift In is held HIGH.
- (4) As soon as Input Ready becomes HIGH the Input Data is loaded into the first word.
- (5) The Data from the first word is released for "fall through" to second word



- 1 The diagram assumes, that at this time, words 63, 62, 61 are loaded with A, B, C Data, respectively.
- 2 Data is shifted out when Shift Out makes a HIGH to LOW transition.

Figure 5. Output Timing

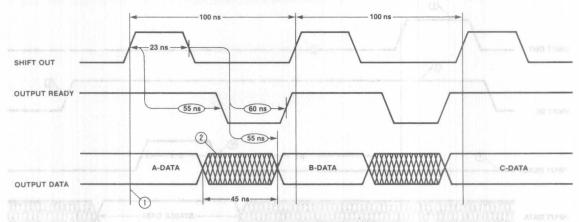


Figure 6. Typical Waveforms for 10 MHz Shift Out Data Rate

- 1) The diagram assumes, that at this time, words 63, 62, 61 are loaded with A, B, C Data, respectively.
- 2 Data in the crosshatched region may be A or B Data.

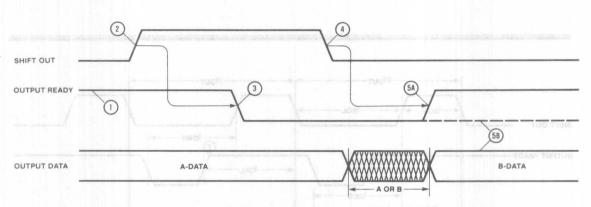
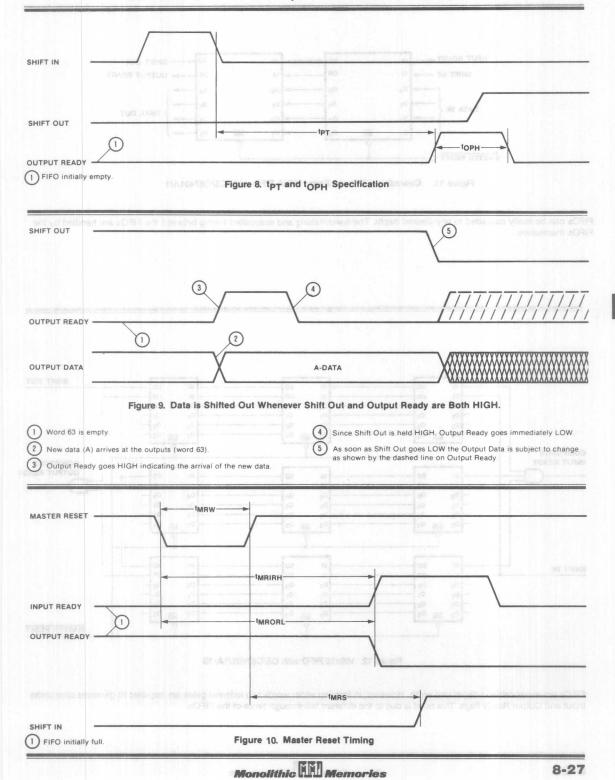


Figure 7. The Mechanism of Shifting Data Out of the FIFO.

- 1) Output Ready HIGH indicates that data is available and a Shift Out pulse may be applied.
- 2 Shift Out goes HIGH causing the next step.
- (3) Output Ready goes LOW.
- (4) Contents of word 62 (B-DATA) is released for "fall through" to word 63.
- (5A) Output Ready goes HIGH indicating that new data (B) is now available at the FIFO outputs.
- (5B) If the FIFO has only one word loaded (A-DATA) then Output Ready stays LOW and the A-DATA remains unchanged at the outputs.

NOTE: Shift Out pulses applied when Output Ready is LOW will be ignored.





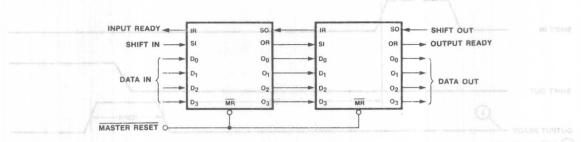


Figure 11. Cascading FIFOs to Form 128x4 FIFO with C5/C67401A/1

FIFOs can be easily cascaded to any desired depth. The handshaking and associated timing between the FIFOs are handled by the FIFOs themselves.

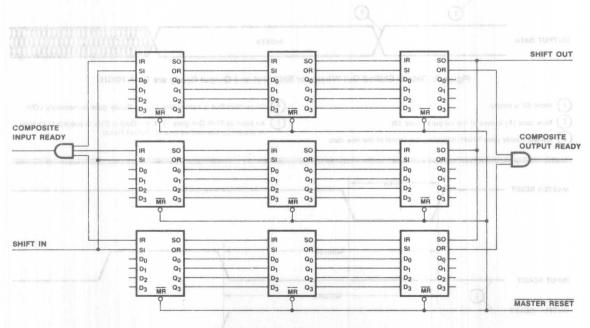


Figure 12. 192x12 FIFO with C5/C67401/1A/1B

FIFOs are expandable in depth and width. However, in forming wider words two external gates are required to generate composite Input and Output Ready flags. This need is due to the different fall-through times of the FIFOs.

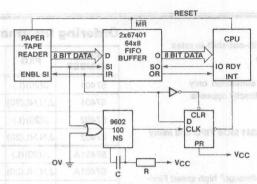
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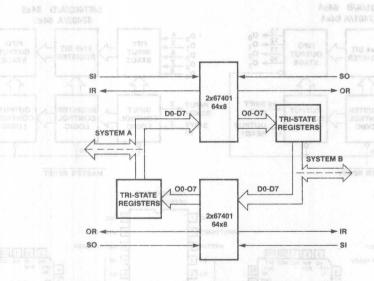
:

Applications



NOTE: The output of monostable holds off the "Buffer full" interrupt for 100ns. If 100ns after shift in, there has not been an input Ready to reset the "D Flip-flop" an interrupt is issued, as the FIFO is full. The CPU then empties the FIFO before the next character is output from the tape drive.

Figure 13. Slow Steady Rate to Fast "Blocked" Rate



NOTE: Both depth and width expansion can be used in this mode. The IR and OR signals are the anded versions of the individual IR and OR signals.

Figure 14. Bidirectional FIFO Application

First-In First-Out (FIFO) 64x4 64x5 Standalone Memory

5/67401 5/67401A 67401B 5/67402 5/67402A 67402B

Features/Benefits

- . Choice of 16.7, 15 and 10 MHz shift-out/shift-in rates
- · Choice of 4-bit or 5-bit data width
- · TTL inputs and outputs
- · Readily expandable in the word dimension only
- Structured pin outs. Output pins directly opposite corresponding input pins
- Asynchronous operation
- Pin-compatible with Fairchild's F3341 MOS FIFO and many times as fast

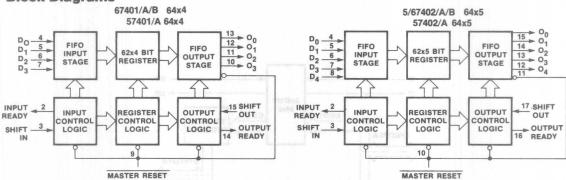
Description

The 5/67401B/2B/1A/2A/1/2 are "fall-through" high speed First-In First-Out (FIFO) memory organized 64 words by 4-bits and 64 words by 5-bits respectively. A 16.7 MHz data rate allows usage in digital video systems; a 15 MHz data rate allows usage in high speed tape or disc controllers and communication buffer applications. Word length is expandable; FIFO depth is not expandable.

Ordering Information

PART NUMBER	PKG	TEMP	DESCRIPTION
57401	J(20)(L)	Mil	7 MHz 64x4 FIFO
67401	J,N,NL(20)	Com	10 MHz 64x4 FIFC
57402	J(20)(L)	Mil	7MHz 64x5 FIFO
67402	J,N,NL(20)	Com	10 MHz 64x5 FIFC
57401A	J,(20)(L)	Mil	10 MHz 64x4 FIFC
67401A	J,N,NL(20)	Com	15 MHz 64x4 FIFC
57402A	J,(20)(L)	Mil	10 MHz 64x5 FIFC
67402A	J,N,NL(20)	Com	15 MHz 64x5 FIFC
67401B	J	Com	16.7 MHz 64x4 FIFO
67402B	J	Com	16.7 MHz 64x5 FIFO

Block Diagrams



Pin Configurations C57402/A 64x5 C67402A/B 64x5 C57401/A 64x4 C67401A/B 64x4 18 VCC 17 SHIFT OUT INPUT READY 2 OE 1 16 VCC 15 SHIFT OUT 16 OUTPUT READY PUT READY 2 SHIFT IN 3 3 2 1 20 19 3 2 1 20 19 15 00 14 OUTPUT READY D0 4 SHIFT IN 3 OUT 17 RDY 17 O0 16 O1 15 14 01 13 00 D1 5 D0 4 5 5 D0 12 01 13 O2 12 O3 00 64x4 D1 5 DATA IN D2 6 OUTPUTS OUTPUTS 6 D1 FIFO 6 FIFO 11 02 67401/A D3 7 67402/A D2 6 7 D2 15 7 D2 11 04 10 03 D4 8 D3 7 03 14 GND MR 03 10 MASTER RESET 9 MASTER RESET GND GND 9 9 10 11 12 13 9 10 11 12 13 **Plastic Chip Carrier Plastic Chip Carrier**

Monolithic MM

8

Absolute Maximum Ratings

Supply voltage V _{CC}	
Input voltage	1.5 V to 7 V
Off-state output voltage	
Storage temperature	65° to +150° C

Operating Conditions 67401B/2B

SYMBOL	PARAMETER YEAR	FIGURE	COMMERCIAL MIN TYP MAX	UNIT
V _{CC}	Supply voltage	THE STREET STREET, STR	4.75 5 5.25	V
TA	Operating free-air temperature		0 75	°C
tSIH †	Shift in HIGH time	1	18	ns
tSIL	Shift in LOW time	1	18	ns
tIDS	Input data setup	1	5	ns
tIDH	Input data hold time	1	40	ns
t _{SOH} †	Shift Out HIGH time	5	18	ns
tSOL	Shift Out LOW time	5	18	ns
^t MRW	Master Reset pulse	10	35	ns
^t MRS	Master Reset to SI	10	35	ns

Switching Characteristics 67401B/2B

Over Operating Conditions

ver operating conditions				THE WINE LE	
SYMBOL	PARAMETER	FIGURE	COMMERCIAL MIN TYP MAX	UNI	
fIN	Shift in rate	1	16.7	MHz	
t _{IRL}	Shift In to input ready LOW	1	35	ns	
t _{IRH}	Shift In to input ready HIGH	1	37	ns	
four	Shift Out rate	5	16.7	MHz	
tORL†	Shift Out to Output Ready LOW	5	38	ns	
tORH†	Shift Out to Output Ready HIGH	5	48	ns	
todh	Output Data Hold (previous word)	5	5 Frow Ixem Hine stad algree	ns	
tods	Output Data Shift (next word)	5	44	ns	
tpT	Data throughput or "fall through"	4,8	1.45	μS	
†MRORL	Master Reset to OR LOW	10	HENRI HI GI 155 DIRENT	ns	
†MRIRH	Master Reset to IR HIGH	10	HOM BRIDG V55	ns	
t _{IPH}	Input Ready pulse HIGH	4	15 HOUR Paled VISSA CHEST	ns	
^t OPH	Output Ready pulse HIGH	8	15	ns	

†See A/C Test and High Speed Application Note.

Absolute Maximum Ratings

Supply voltage V _{CC}	-0.5 V to 7 V
Input voltage	-1.5 V to 7 V
Off-state output voltage	0.5 V to 5.5 V
Storage temperature	5° to +150°C

Operating Conditions 5/67401A/2A

SYMBOL	PARAMETER	FIGURE	MIN	MILITAR' TYP	MAX	MIN	MMERC TYP	MAX	UNIT
VCC	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
TA	Operating free-air temperature		-55		*125	0	0.00	75	°C
tSIH†	Shift in HIGH time	1	35		- NEW	23		28†	ns
^t SIL	Shift in LOW time	1	35			25	a settlebe for	uncal.	ns
t _{IDS}	Input data setup	11	5		Maria	5	41410.00		ns
^t IDH	Input data hold time	1 1	45			40		NA P	ns
tson†	Shift Out HIGH time	5	35			23	11.6-6	4	ns
tSOL	Shift Out LOW time	5	35			25	and I had		ns
^t MRW	Master Reset pulse	10	40	<u> </u>	154	35	Ages Cl. No. II		ns
^t MRS	Master Reset to SI	10	45	L		35			ns

^{*}Case temperature.

Switching Characteristics 5/67401A/2A

Over Operating Conditions

SYMBOL	PARAMETER	FIGURE	MIN	MILITARY TYP MAX	COMMERCIAL MIN TYP MAX	UNIT
fIN	Shift in rate	1	10	ROY	15	MHz
tIRL†	Shift In to Input Ready LOW	1		50	40	ns
t _{IRH} †	Shift In to Input Ready HIGH	1	N	50	40	ns
four	Shift Out rate	5	10	H2NH v	15	MHz
tORL†	Shift Out to Output Ready LOW	5		65	45	ns
torh†	Shift Out to Output Ready HIGH	5	2	65	50	ns
todh	Output Data Hold (previous word)	5	10	T FIGHT OWNERS	10	ns
tods	Output Data Shift (next word)	5	a	60	45	ns
t _{PT}	Data throughput or "fall through"	4, 8	2	2.2	1.6	μS
^t MRORL	Master Reset to OR LOW	10	9 A	65	60	ns
^t MRIRH	Master Reset to IR HIGH	10	or -	65	60	ns
t _{IPH}	Input Ready pulse HIGH	4	20	Han	20	ns
tOPH	Output Ready pulse HIGH	8	20	I was	20	ns

Absolute Maximum Ratings

Supply voltage V _{CC}	
Input voltage Off-state output voltage	
Storage temperature	65° to +150°C

Operating Conditions 5/67401/2

SYMBOL	PARAMETER	FIGURE	MIN	MILITAR TYP	MAX	MIN	MMERC TYP	MAX	UNIT
VCC	Supply voltage	VAIS 4 N	4.5	5	5.5	4.75	5	5.25	V
TA	Operating free-air temperature	NO A CONTRACTOR	-55	- 2017	*125	0	Iculai entre	75	°C
tsiH†	Shift in HIGH time	1	45	-		35	minist to be		ns
tSIL	Shift in LOW time	1	45	- 00	-	35	Will two London		ns
tIDS	Input data setup	1	10	- 99		5			ns
t _{IDH}	Input data hold time	1	55	00*	11.00	45	A PROPERTY	ACTOR I	ns
tsoH†	Shift Out HIGH time	5	45			35			ns
tSOL	Shift Out LOW time	5	45	z woV		35		THUR	ns
tMRW	Master Reset pulse†	A 1010	30	aluent.		35	Supply		ns
t _{MRS}	Master Reset to SI	10	45	alugius		35		3001141	ns

^{*}Case temperature.

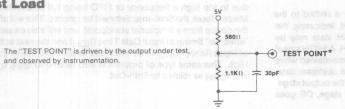
Switching Characteristics 5/67401/2

Over Operating Conditions

SYMBOL	Obns WOLFE PARAMETER SECTION OF	FIGURE	MILITARY MIN TYP MAX	COMMERCIAL MIN TYP MAX	UNIT
fine se be	Shift in rate	A mignif	7 mr will such heating	10	MHz
t _{IRL} †	Shift In to input ready LOW	alangis	togot nortW nortgod 160 s	fit ni atab toes m of CE45 ar	ns
t _{IRH} †	Shift In to input ready HIGH	Li evard	60	45	ns
four	Shift Out rate	5	187A HEIH Integend at 118	110/in/2 ent media coltrac	MHz
tORL†	Shift Out to Output Ready LOW	5	65	OU op of HI art seeus 55	ns
tORH†	Shift Out to Output Ready HIGH	5	rocor som fad gnirso701	HOH og Hw H Juli 160 al	ns
^t ODH	Output Data Hold (previous word)	5	10 s est of elegaçoiq i	10 State manufacture of	ns
tods	Output Data Shift (next word)	5	stated studius entre 65 er	ng at brow tan art mc55 or	ns
t _{PT}	Data throughput or "fall through"	4,8	WOJ mamer aw St. Ji 4	Meaning att 1 beings 3 h	μS
†MRORL	Master Reset to OR LOW	10	65	60	ns
†MRIRH	Master Reset to IR HIGH	10	65	60	ns
t _{IPH}	Input Ready pulse HIGH	TUESSIT4	or 20 ; cu xoate flaw atab a	20 entres circles na vd	ns
^t OPH	Output Ready pulse HIGH	8	20 M Of Sloduc Aw &	20" Viume with eartean	ns

[†]See AC test and high speed application note.

* The "TEST POINT" is driven by the output under test, and observed by instrumentation.



Input Pulse 0 to 3 V Input Rise and Fall Time (10% - 90%) 5 ns minimum Measurements made at 1.5 V

SYMBOL	PARAMET	ER		TEST CONDITIONS	MIN TY	P MAX	UNIT
VIL	Low-level input vol	Itage			ogsfk	0.8†	٧
VIH	High-level input vo	oltage	The second second		2†		V
VIC	Input clamp voltag	je	V _{CC} = MIN	I _I = -18mA	allone.	-1.5	V
IL1	Low-level	D ₀ -D _n , MR	War - MAY	V ₁ = 0.45V		-0.8	mA
I _{IL2}	input current	SI, SO	V _{CC} = MAX	V ₁ = 0.45V		-1.6	mA
ΊΗ	High-level input co	urrent	V _{CC} = MAX	V ₁ = 2.4V	alke yidge	50	μΑ
1	Maximum input current		VCC = MAX	V _I = 5.5V	THE OFFICE OF	1	mA
VOL	Low-level output voltage		V _{CC} = MIN	I _{OL} = 8mA	0.50 5 23 65	0.5	V
VOH	High-level output v	oltage	V _{CC} = MIN	I _{OH} = -0.9mA	2.4		V
los	Output short-circu	uit current *	V _{CC} = MAX	V ₀ = 0V	-20	- 90	mA
80		10	45	5/67401	thi tuo tie	160	Linal
81		1	45	5/67402	OJ NO M	180	arani
Icc	Supply curi	rent	V _{CC} = MAX	67401A	oas Francis	170	lucities!
00		Inputs low, outputs open.	67402A	eater Pase	190	agud	
e man e me en l'ang				67401B, 57401A		180	tred past
				67402B, 57402A		200	200

* Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
†There are absolute voltages with respect to degree GND (PIN 8 or 9) and includes all overshoots due to test equipment.

Functional Description

Data Input

After power up the Master Reset is pulsed low (Fig. 10) to prepare the FIFO to accept data in the first location. When Input Ready (IR) is HIGH the location is ready to accept data from the $D_{\rm X}$ inputs. Data then present at the data inputs is entered into the first location when the Shift In (SI) is brought HIGH. A SI HIGH signal causes the IR to go LOW. Data remains at the first location until SI is brought LOW. When SI is brought LOW and the FIFO is not full, IR will go HIGH, indicating that more room is available. Simultaneously, data will propagate to the second location and continue shifting until it reaches the output stage or a full location. The first word is present at the outputs before a shift out is applied. If the memory is full, IR will remain LOW.

Data Transfer

Once data is entered into the second cell, the transfer of any full cell to the adjacent (downstream) empty cell is automatic, activated by an on-chip control. Thus data will stack up at the end of the device while empty locations will "bubble" to the front. tp_ defines the time required for the first data to travel from input to the output of a previously empty device.

Data Output

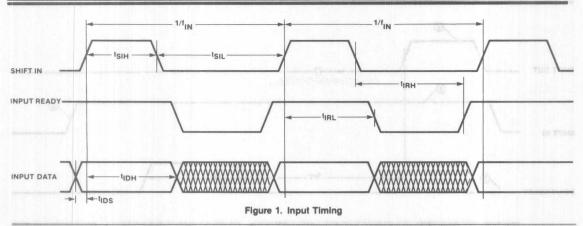
Data is read from the O_X outputs. When data is shifted to the output stage, Output Ready (OR) goes HIGH, indicating the presence of valid data. When the OR is HIGH, data may be shifted out by bringing the Shift Out (SO) HIGH. A HIGH signal at SO causes the OR to go LOW. Valid data is maintained while the SO is HIGH. When SO is brought LOW the upstream data, provided that stage has valid data, is shifted to the output stage. When new valid data is shifted to the output stage, OR goes

HIGH. If the FIFO is emptied, OR stays LOW, and O_X remains as before, (i.e. data does not change if FIFO is empty).

Input Ready and Output Ready may also be used as status signals indicating that the FIFO is completely full (Input Ready stays LOW for at least tpT) or completely empty (Output Ready stays LOW for at least tpT).

AC Test and High Speed App. Notes

Since the FIFO is a very-high-speed device, care must be exercised in the design of the hardware and the timing utilized within the design. The internal shift rate of the FIFO typically exceeds 20 MHz in operation. Device grounding and decoupling is crucial to correct operation as the FIFO will respond to very small glitches due to long reflective lines, high capacitance and/or poor supply decoupling and grounding. We recommend a monolithic ceramic capacitor of 0.1 µF directly between VCC and GND with very short lead length. In addition, care must be exercised in how the timing is set up and how the parameters are measured. For example, since an AND gate function is associated with both the Shift In-Input Ready combination, as well as the Shift Out-Output Ready combination, timing measurements may be misleading, i.e., rising edge of the Shift-In pulse is not recognized until Input-Ready is High. If Input-Ready is not high due to too high a frequency or FIFO being full or affected by Master Reset, the Shift-In activity will be ignored. This will affect the device from a functional standpoint, and will also cause the "effective" timing of Input Data Time (tIDH) and the next activity of Input Ready (tipl) to be extended relative to Shift-In going High. This same type of problem is also related to tIRH, tORI and torh as related to Shift-Out.



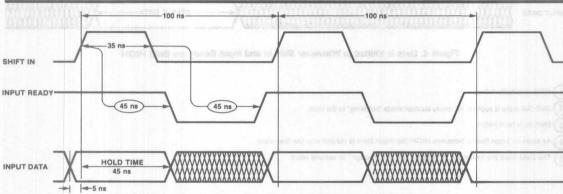
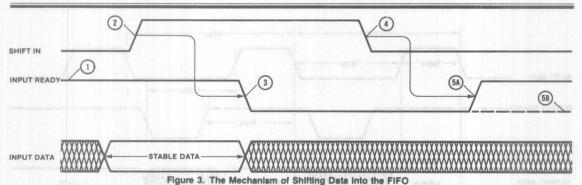


Figure 2. Typical Waveforms for 10 MHz Shift In Data Rate (67401/2)



- 1) Input Ready HIGH indicates space is available and a Shift In pulse may be applied
- 2 Input Data is loaded into the first word.
- (3) Input Ready goes LOW indicating the first word is full.
- 4) The Data from the first word is released for "fall-through" to second word.
- (5A) The Data from the first word is transferred to second word. The first word is now empty as indicated by Input Ready HIGH.
- (5B) If the second word is already full then the data remains at the first word. Since the FIFO is now full Input Ready remains low.

NOTE: Shift In pulses applied while Input Ready is LOW will be ignored. (See Figure 4.)

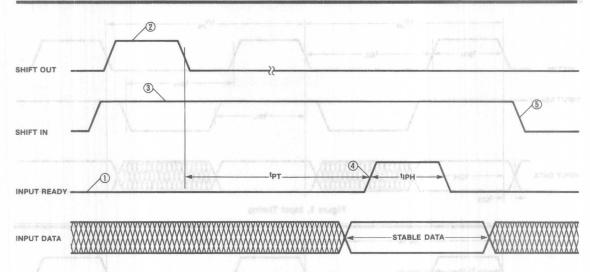


Figure 4. Data is Shifted in Whenever Shift in and Input Ready are Both HIGH

- 1) FIFO is initially full.
- 2 Shift Out pulse is applied. An empty location starts "bubbling" to the front.
- 3 Shift In is held HIGH.
- (4) As soon as Input Ready becomes HIGH the Input Data is loaded into the first word.
- The Data from the first word is released for "fall through" to second word.

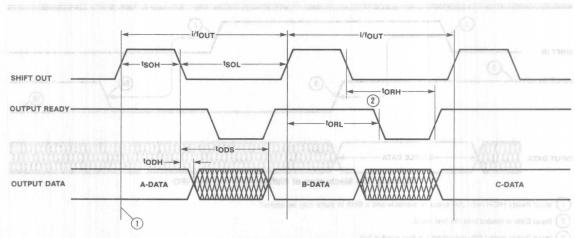


Figure 5. Output Timing

- 1) The diagram assumes, that at this time, words 63, 62, 61 are loaded with A. B. C Data, respectively.
- Data is shifted out when Shift Out makes a HIGH to LOW transition.

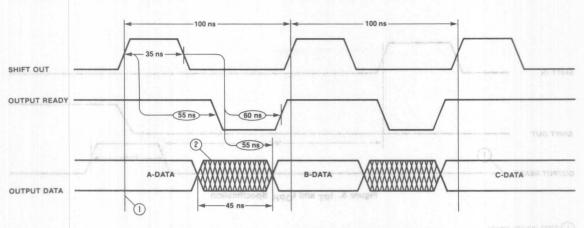


Figure 6. Typical Waveforms for 10 MHz Shift Out Data Rate (67401/2)

- The diagram assumes, that at this time, words 63, 62, 61 are loaded with A, B, C Data, respectively.
- 2 Data in the crosshatched region may be A or B Data.

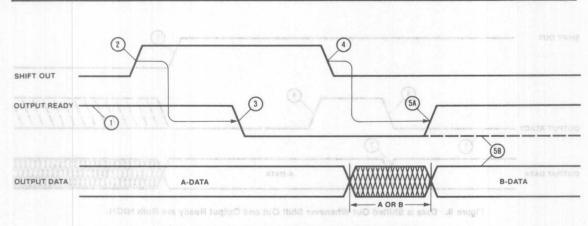
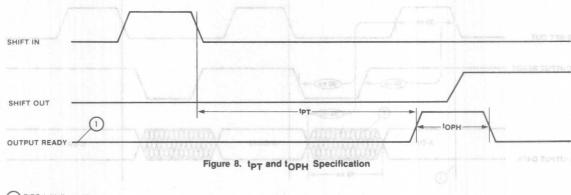


Figure 7. The Mechanism of Shifting Data Out of the FIFO.

- 1) Output Ready HIGH indicates that data is available and a Shift Out pulse may be applied.
- 2) Shift Out goes HIGH causing the next step.
- (3) Output Ready goes LOW.
- (4) Contents of word 62 (B-DATA) is released for "fall through" to word 63.
- (5A) Output Ready goes HIGH indicating that new data (B) is now available at the FIFO outputs.
- (5B) If the FIFO has only one word loaded (A-DATA) then Output Ready stays LOW and the A-DATA remains unchanged at the outputs.

NOTE: Shift Out pulses applied when Output Ready is LOW will be ignored.





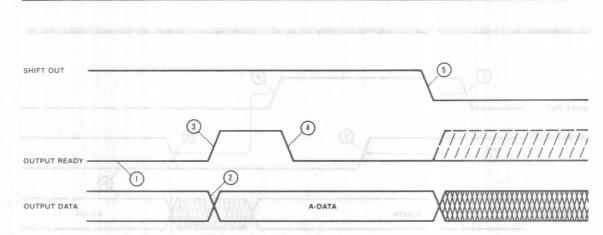
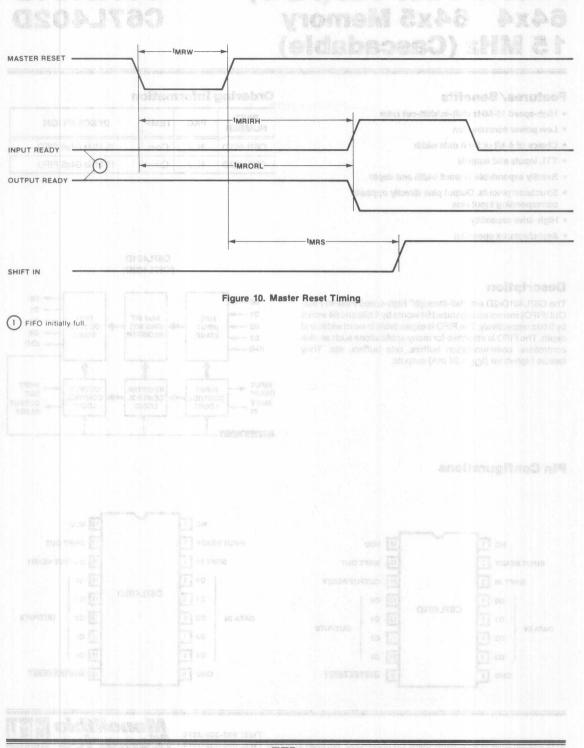


Figure 9. Data is Shifted Out Whenever Shift Out and Output Ready are Both HIGH.

- 1 Word 63 is empty.
- (2) New data (A) arrives at the outputs (word 63).
- Output Ready goes HIGH indicating the arrival of the new data.
- (4) Since Shift Out is held HIGH, Output Ready goes immediately LOW.
- (5) As soon as Shift Out goes LOW the Output Data is subject to change as shown by the dashed line on Output Ready





First-In First-Out (FIFO) 64x4 64x5 Memory 15 MHz (Cascadable)

C67L401D C67L402D

Features/Benefits

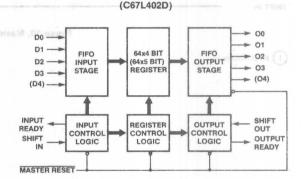
- · High-speed 15-MHz shift-in/shift-out rates
- Low power consumption
- . Choice of 4-bit or 5-bit data width
- . TTL inputs and outputs
- · Readily expandable in word width and depth
- . Structured pinouts. Output pins directly opposite corresponding input pins
- High-drive capability
- Asynchronous operation

Ordering Information

PART NUMBER	PKG	ТЕМР	DESCRIPTION		
C67L401D	N, J	Com	15 MHz 64x4 FIFO		
C67L402D	N, J	Com	15 MHz 64x5 FIFO		

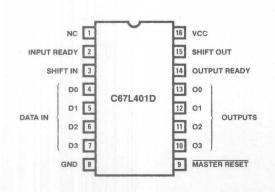
Description

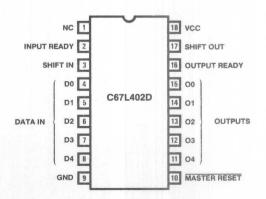
The C67L401D/2D are "fall-through" high-speed First-In First-Out (FIFO) memories organized 64 words by 4 bits and 64 words by 5 bits respectively. The FIFO is expandable in word width and depth. The FIFO is attractive for many applications such as disk controllers, communication buffers, rate buffers, etc. They feature high-drive (IOL = 24 mA) outputs.



C67L401D

Pin Configurations





TWX: 910-338-2376 2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2374

Monolithic Memories

Absolute Maximum Ratings

Supply voltage V _{CC} 0.5	V to 7 V
Input voltage	V to 7 V
Off-state output voltage	/ to 5.5 V
Storage temperature	5 +150°C

Switching Churacteristics over Operating Conditions

Operating Conditions Over Temperature Range

SYMBOL	PARAMETER	8	FIGURE	COMMERCIAL MAX	UNIT
VCC	Supply voltage			4.75 (now txen) fil 5: steC high/C 5.25	e.Vo
TA	Operating free-air temperature	4,8		0 fuqriquenti sisQ 70	°C
fIN	Shift in rate		1 W	15. Mester Resert to Output Ready LO	MHz
tSIH	Shift in High time	or Land		241 yoseH tucni of I feed issisting "to	RIPM
tsiL	Shift in Low time			* Master Foser Ltp Input Ready Ltt	ns
tids	Input data setup to SI (Shift In)		1	Master Reset to Dulpute LOW 0	ns
tIDH	Input data hold from SI (Shift In)	Α	1	26 HOIH salvo yb. at togn	ns
tRIDS	Input data setup to IR (Input Ready)	8	4	Output ready pulse HIGH 0	ns
tRIDH	Input data hold from IR (Input Ready)	2 1	4	26 Bilis V alad of 1 (book) Judia Valid 6	ns
four	Shift out rate dglrl asog FI	ing high when N	outer F5 /d box	Pts not full (IR reph). MR low forces IR fow follow	MHz
tsoH	Shift out High time		-	17	JA GGG
tSOL	Shift out Low time		5	15	ns
tMRW	Master Reset pulse**		10	35	ns
tMRS	Master Reset to SI*		10	35	ns

^{*} If the FIFO is not full (IR High), $\overline{\text{MR}}$ low forces IR low, followed by IR returning high when $\overline{\text{MR}}$ goes high.

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAME	PARAMETER		TEST CONDITION		COMMERCIAL TYP	MAX	UNIT
VIL	Low-level input	voltage					0.8**	V
VIH	High-level input voltage				2**			V
VIC	Input clamp voltage		VCC = MIN	I _I = -18 mA			-1.5	V
IIL	Low-level input current		V _{CC} = MAX	V _I = 0.45 V			-250	μА
IIH	High-level input current		VCC = MAX	V _I = 2.4 V			50	μΑ
11	Maximum input	current	V _{CC} = MAX	V _I = 5.5 V			. 1	mA
V	Low-level	Output, O	VCC = MIN	I _{OL} = 24 mA			0.5	V
VOL	Output voltage	IR, OR	VCC = MIN	IOL = 8 mA		V		
\/-··	High-level	Output, O	VCC = MIN	IOH = -3.0 mA	2.4			V
VOH	Output voltage	IR, OR	VCC = MIN	IOH = -0.9 mA	2.4			V
los	Output short-cir	cuit current*	V _{CC} = MAX	VO = 0V	-20		-90	mA
Icc	Supply current		VCC = MAX All inputs low. All outputs open.	L401D/2D			100	mA

Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second. These are absolute voltages with respect to GND (Pin 8 or 9) and include all overshoots due to test equipment

^{**} See AC test and high-speed application note.

SYMBOL	PARAMETER	FIGURE	COMMERCIAL MIN TYP MAX	UNIT
tIRL†	Shift In 1 to Input Ready LOW		40 110	ns
tIRH†	Shift In ↓ to Input Ready HIGH		26	ns
tORL†	Shift Out † to Output Ready LOW	ognaR europmaT ver 1 Beroldinger 45 H		ns
tORH†	Shift Out ↓ to Output Ready HIGH	5	50	ns
tODH†	Output Data Hold (previous word)	5	12	ns
tods	Output Data Shift (next word)		sparter yapan 40	
tpT	Data throughput	4,8	enulareciment re-neill gallere (1600	
†MRORL	Master Reset ↓ to Output Ready LOW		ette nettade 60	
tMRIRH*	Master Reset † to Input Ready HIGH	10	evnii rigii-i nutrint 30	ns
tMRIRL*	Master Reset ↓ to Input Ready LOW	10	smil way ni itm 50	ns
tMRO	Master Reset ↓ to Outputs LOW		(Al north date setue for Strift (in)	ns
tIPH .	Input ready pulse HIGH	4 (p17(p18) or ment blood state (pant)		ns
^t OPH	Output ready pulse HIGH	8	yoss24 ugan fall of gules such fregal	
tORD	Output ready t to Data Valid	5	S-regul dade read town 12 (tread Read	ns

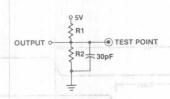
^{*} If the FIFO is not full (IR High), \overline{MR} low forces IR low, followed by IR returning high when \overline{MR} goes high.

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[†] See AC test and high-speed application note.

E

Standard Test Load



Input Pulse Amplitude = 3 V Input Rise and Fall Time (10%–90%) = 2.5 ns Measurements made at 1.5 V

IOL	nog nieft R1 svitslet	R2
24 mA	200 Ω	300 Ω
8 mA	600 Ω	1200 Ω

Functional Description Data Input

After power up the Master Reset is pulsed low (Figure 10) to prepare the FIFO to accept data in the first location. Master reset must be applied prior to use to ensure proper operation. When Input Ready (IR) is HIGH the first location is ready to accept data from the Dy inputs. Data then present at the data inputs is entered into the first location when the Shift-In (SI) is brought HIGH. A SI HIGH signal causes the IR to go LOW. Once data is entered into the first cell, the transfer of data from any full cell to the adjacent (downstream) empty cell is automatic, activated by an on-chip control. Thus data will stack up at the end of the device while empty locations will "bubble" to the front. tpT defines the time required for the first data to travel from input to the output of a previously empty device. When SI is brought LOW and the FIFO is not full, IR will go HIGH, indicating more room is available. If the memory is full, IR will remain LOW. The FIFO should always be cleared by using master reset.

Data Output

Data is read from the O_X outputs. When data is shifted to the output stage, Output Ready (OR) goes HIGH, indicating the presence of valid data. When the OR is HIGH, data may be shifted out by bringing the Shift Out (SO) HIGH. A HIGH signal at SO causes the OR to go LOW. Valid data is maintained while the SO is HIGH. When SO is brought LOW the upstream data, provided the upstream stage has valid data, is shifted to the output stage, When new valid data is shifted to the output stage,

OR goes HIGH. If the FIFO is emptied, OR stays LOW and Data output will not be valid.

Input Ready and Output Ready may also be used as status signals indicating that the FIFO is completely full (Input Ready stays LOW for at least tp_T) or completely empty (Output Ready stays LOW for at least tp_T).

AC Test and High-Speed App. Notes

Since the FIFO is a very-high-speed device, care must be exercised in the design of the hardware and the timing utilized within the design. The internal shift rate of the FIFO typically exceeds 20 MHz in operation. Device grounding and decoupling is crucial to correct operation as the FIFO will respond to very small glitches due to long reflective lines, high capacitances and/or poor supply decoupling and grounding. Monolithic Memories recommends a monolithic ceramic capacitor of 0.1 μF directly between VCC and GND with very short lead length. In addition, care must be exercised in how the timing is set up and how the parameters are measured. For example, since an AND gate function is associated with both the Shift-In-Input-Ready combination, as well as the Shift-Out-Output-Ready combination, timing measurements may be misleading, i.e., rising edge of the Shift-In pulse is not recognized until Input Ready is HIGH. If Input Ready is not high due to (a) too high a frequency, or (b) FIFO being full or effected by Master Reset, the Shift-In activity will be ignored. This will affect the device from a functional standpoint, and will also cause the "effective" timing of Input

Data Hold time (T_{IDH}) and the next activity of Input Ready (T_{IRL}) to be extended relative to shift-in going HIGH. This same type of situation occurs with T_{ORL} and T_{ORH} as related to

Shift-Out. For high-speed applications, proper grounding technique is essential.

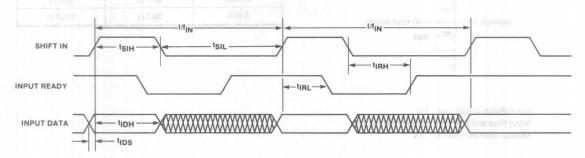


Figure 1. Input Timing

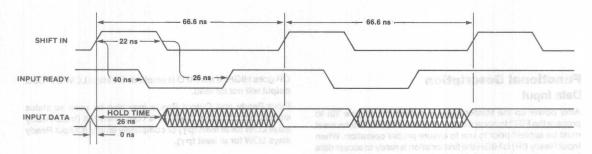


Figure 2. Typical Waveforms for 15-MHz Shift-In Rate

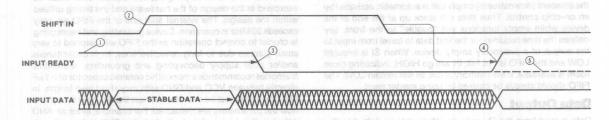


Figure 3. The Mechanism of Shifting Data into the FIFO

- 1 Input Ready HIGH indicates space is available and a Shift-In pulse may be applied.
- 2 Input Data is loaded into the first word. The Data from the first word is released for "fall-through" to second word.
- 3 Input Ready goes LOW indicating the first word is full.
- (4) Shift-In going LOW allows Input Ready to sense the status of first word. The first word is now empty as indicated by Input Ready HIGH.
 - (5) If the second word is already full then the data remains at the first word. Since the FIFO is now full Input Ready remains low. NOTE: Shift-In pulses applied while Input Ready is LOW will be ignored

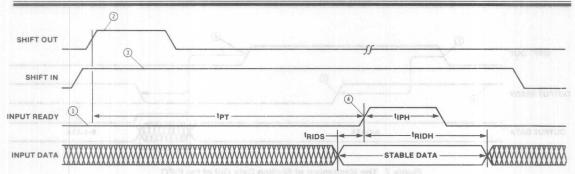


Figure 4. Data is Shifted in Whenever Shift In and Input Ready are Both HIGH

- 1 FIFO is initially full.
- 2) Shift Out pulse is applied. An empty location starts "bubbling" to the front.
- 3 Shift In is held HIGH
- 4 As soon as Input Ready becomes HIGH the Input Data is loaded into the first word.

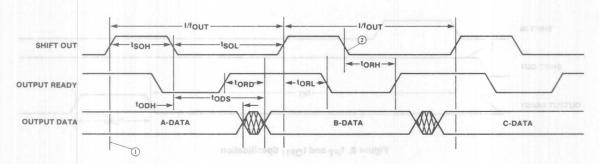


Figure 5. Output Timing

- 1) The diagram assumes that at this time, words 63, 62 and 61 are loaded with A, B and C Data, respectively.
- 2) Output data changes on the falling edge of SO after a valid Shift-Out Sequence, i.e. OR and SO are both high together.

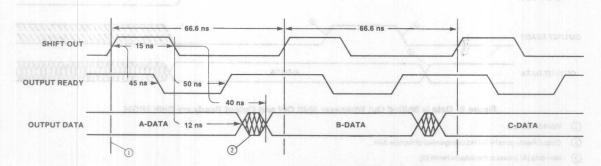


Figure 6. Typical Waveforms for 15-MHz Shift-Out Data Rate

- 1) The diagram assumes that at this time words 63, 62 and 61 are loaded with A, B and C Data, respectively.
- 2 Data in the first crosshatched region may be A or B Data.

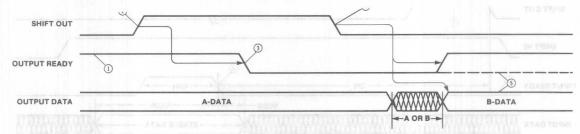


Figure 7. The Mechanism of Shifting Data Out of the FIFO

- ① Output Ready HIGH indicates that data is available and a Shift-Out pulse may be applied.
- ② Shift-Out goes HIGH causing the contents of word 62 (B-Data) to be released for fall-through to word 63. Output data remains as valid A-Data while Shift-Out is HIGH.
- 3 Output Ready goes LOW.
- (4) Shift-out goes LOW causing Output Ready to go HIGH and new data (B) to appear at the data outputs.
- (5) If the FIFO has only one word loaded (A-Data) then Output Ready stays LOW and the output data becomes invalid.

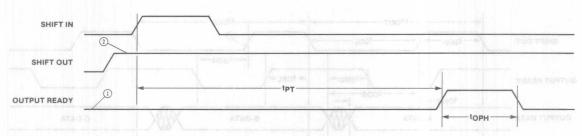


Figure 8. tpT and toPH Specification

- 1 FIFO initially empty.
- (2) Shift Out held HIGH

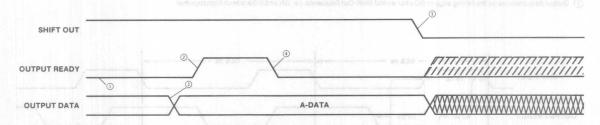
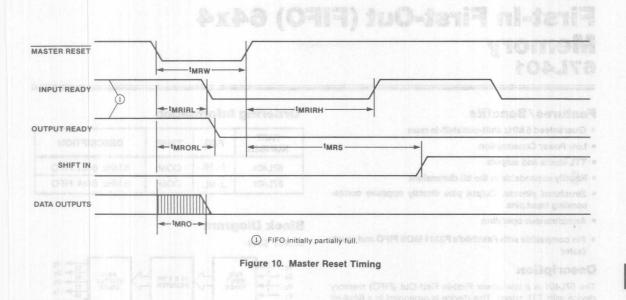


Figure 9. Data is Shifted Out Whenever Shift Out and Output Ready are Both HIGH.

- 1) Word 63 is empty.
- 2) Output Ready goes HIGH indicating arrival of the new data.
- 3 New data (A) arrives at the outputs (word 63).
- 4 Since Shift Out is held HIGH, Output Ready goes immediately LOW.
- (§) As soon as Shift Out goes LOW the Output Data is subject to change. Output Ready will go HIGH or LOW depending on whether there are any additional upstream words in the FIFO.





Monolithic MM Memories

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Low Power First-In First-Out (FIFO) 64x4 Memory 67L401

Features/Benefits

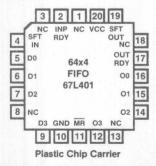
- · Guaranteed 5 MHz shift-out/shift-in rates
- Low Power Consumption
- · TTL inputs and outputs
- · Readily expandable in the bit dimensions
- Structured pinouts. Output pins directly opposite corresponding input pins
- Asynchronous operation
- Pin compatible with Fairchild's F3341 MOS FIFO and much faster

Description

The 67L401 is a low-power First-In First-Out (FIFO) memory device with TTL speed. This device is organized in a 64x4-bit structure and easily expandable to any width. A 5 MHz data rate with fast "fall through" time allows usage in tape and disc controllers, printers and communications buffer applications. This data rate is much faster than a comparable MOS device. The FIFO is a register-based device. Data entered at the inputs "falls through" to the empty space closest to the output. Data is shifted out in the same sequence it is shifted in. Also, the width can be increased by putting the Input Ready signals through an AND gate to give a composite Input Ready. Similarly, the Output Ready signals should be gated to form a composite Output Ready.

Generally, FIFOs are used in digital systems performing data transfers when source and receiver are not operating at the same data rate. FIFOs are also used as data buffers where the source and receiver are not operating at the same time. The 67L401 is particularly useful where low-power consumption is critical

Pin Configurations

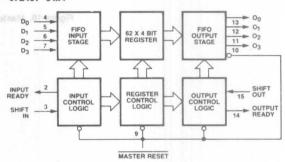


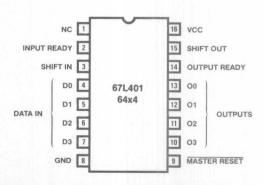
Ordering Information

PART NUMBER	PKG	TEMP	DESCRIPTION
67L401	N, NL	СОМ	5 MHz 64x4 FIFO
67L401	J, NL	СОМ	5 MHz 64x4 FIFO

Block Diagram

67L401 64x4





Monolithic Memories

TWX: 910-338-2376 2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2374

Electrical Characteristics over overline Conditions

Absolute Maximum Ratings

Supply voltage Voc	0.5 V to 7 V
	-1.5 V to 7 V
	0.5 V to 5.5 V
	65° to +150°C

Operating Conditions

SYMBOL	PARAMETER	FIGURE	MIN	COMMERCIAL	MAX	UNIT
V _{CC}	Supply voltage		4.75	62 18 II	5.25	V
TA	Operating free-air temperature	V	AAM 0 00V	nour current	75	°C
tSIH†	Shift in HIGH time	1_1_	55	approduced and	Tuguxelvi	ns
tSIL tsil	Shift in LOW time	1	55	agailov rugitu	o leve-wou	ns
tIDS	Input data setup	0 1	10	sčenov indirv	Fight-fevel c	ns
^t IDH	Input data hold time	1	80	TABITUQ IIUONO-I	Origina	ns
tsoH†	Shift Out HIGH time	5	55	7081	IOD ALEBRIC	ns
tsol	Shift Out LOW time one error bedoes fon bludde i	1010 5 Me 9	1 to a 55 up to a	ould be shorted at a fine	na pine profinal sh	ns
^t MRW	Master Reset pulse	10	40	UNA sone to pages in	W lightest emices	ns
^t MRS	Master Reset to SI	10	35			ns

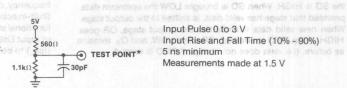
Switching Characteristics Over Operating Conditions

SYMBOL	tut vibroignous at Catta out tent gattasapat earning vibroit vibroit PARAMETER set to to WOLL as	FIGURE	COMMERCIAL MIN TYP MAX	UNIT
fIN	Shift in rate	1 18	A H5IH inguino si (I2) ni fini3 em nervi notal	MHz
t _{IRL} †	Shift in to Input Ready LOW	1	Hard is artementally Woulder of Florit 175 to be	ns
tIRH†	Shift in to Input Ready HIGH	1 m	not 67. IR will go HIGH, Indicating that more room	ns
four	Shift Out rate	5	coes 5 m of avagequity like was ylsucientilumics.	MHz
tORL†	Shift Out to Output Ready LOW	5	aled studiod self to increase at provincial self-	ns
tORH†	Shift Out to Output Ready HIGH	5	s app 08d. If the memory is full, IR will remain LO	ns
t _{ODH}	Output Data Hold (previous word)	5	8 Totans	ns
tops	Output Data Shift (next word)	9 5 mg	en 070 into the second cell, the transfer of any	ns
tpT	Data throughput or "fall through"	4, 8	singly at the young (misertanwon) into a los	μS
^t MRORL	Master Reset to OR LOW	10	levice 18 maly locations will "bubble" to the mo	ns
^t MRIRH	Master Reset to IR HIGH	10	is most level of sist tell edit of best of 85	ns
tIPH*	Input Ready pulse HIGH and digned basel had	a 4	20	ns
tOPH*	Output Ready pulse HIGH	8	20	ns

[†] See AC test and application note.

Test Load

* The "TEST POINT" is driven by the output under test. and observed by instrumentation.



seon AD leasts to Input Pulse 0 to 3 V stab billsy even nartW Input Rise and Fall Time (10% - 90%) TEST POINT* 5 ns minimum on 2005 Miss all granded as Measurements made at 1.5 V

^{*} This parameter applies to FIFOs communicating with each other in a cascade mode.

SYMBOL	PARAN	METER		MIN TYP	MAX	UNIT	
V _{IL}	Low-level inpu	t voltage	A NO S		entite .	0.8	V
VIH	High-level inpu	ut voltage			2†	nila	V
VIC	Input clamp vo	oltage	V _{CC} = MIN	I _I = -18mA		-1.5	V
I _{IL1}	Low-level	D ₀ -D ₃ MR	V. MAN	DAIN PARTITION		-0.8	mA
I _{IL2}	input current	SI, SO	V _{CC} = MAX	V _I = 0.45V	Sandy your	-1.6	mA
I _{IH}	High-level inpu	ut current	V _{CC} = MAX	V ₁ = 2.4V	est our day word	50	μΑ
Tien	Maximum inpu	ut current	V _{CC} = MAX	V _I = 5.5V	12 84 of 8883	1.	mA
VOL	Low-level outp	out voltage	V _{CC} = MIN	I _{OL} = 8mA	Shift in LOw	0.5	V
VOH	High-level outp	out voltage	V _{CC} = MIN	I _{OH} = -0.9mA	2.4		V
los	Output short-c	circuit current*	V _{CC} = MAX	V ₀ = 0V	-20	-90	mA
lcc	Supply Current V _{CC} = MAX Inpu		puts Low, Outputs Open	95	110	mA	

^{*} Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

Functional Description Data Input

After power up the Master Reset is pulsed low (Fig. 11) to prepare the FIFO to accept data in the first location. When Input Ready (IR) is HIGH the location is ready to accept data from the $D_{\rm X}$ inputs. Data then present at the data inputs is entered into the first location when the Shift In (SI) is brought HIGH. A SI HIGH signal causes the IR to go LOW. Data remains at the first location until SI is brought LOW. When SI is brought LOW and the FIFO is not full, IR will go HIGH, indicating that more room is available. Simultaneously, data will propagate to the second location and continue shifting until it reaches the output stage or a full location. The first word is present at the outputs before a shift out is applied. If the memory is full, IR will remain LOW.

Data Transfer

Once data is entered into the second cell, the transfer of any full cell to the adjacent (downstream) empty cell is automatic, activated by an on-chip control. Thus data will stack up at the end of the device while empty locations will "bubble" to the front. tpt defines the time required for the first data to travel from input to the output of a previously empty device.

Data Output

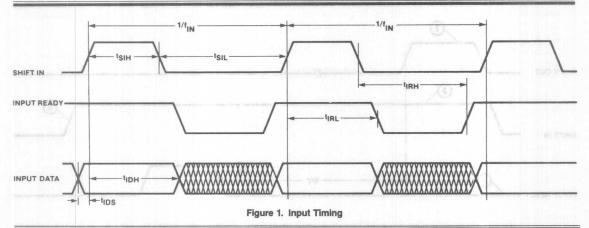
Data is read from the O_X outputs. When data is shifted to the output stage, Output Ready (OR) goes HIGH, indicating the presence of valid data. When the OR is HIGH, data may be shifted out by bringing the Shift Out (SO) HIGH. A HIGH signal at SO causes the OR to go LOW. Valid data is maintained while the SO is HIGH. When SO is brought LOW the upstream data, provided that stage has valid data, is shifted to the output stage. When new valid data is shifted to the output stage, OR goes HIGH. If the FIFO is emptied, OR stays LOW, and O_X remains as before, (i.e. data does not change if FIFO is empty).

Input Ready and Output Ready may also be used as status signals indicating that the FIFO is completely full (Input Ready stays LOW for at least tp_) or completely empty (Output Ready stays LOW for at least tp_).

AC Test and Application Note

Since the FIFO is a very-high-speed device, care must be exercised in the design of the hardware and the timing. Though the external data rate is 5 MHz internally the device is several times as fast. Device grounding and decoupling is crucial to correct operation, as the FIFO will respond to very small glitches caused by long reflective lines, high capacitances and/or poor supply decoupling and grounding. We recommend a monolithic ceramic capacitor of 0.1 µF directly between Voc and GND with very short lead length. In addition, care must be exercised in timing set up and measurement of parameters. For example, since an AND gate function is associated with both the Shift In-Input Ready Combination, as well as the Shift Out-Output Ready Combination, timing measurements may be misleading, i.e., rising edge of the Shift-In pulse is not recognized until Input-Ready is High.If Input-Ready is not high due to too high a frequency, or the FIFO being full or affected by Master Reset, the Shift-In activity will be ignored. This will affect the device from a functional standpoint, and will also cause the "effective" timing of Input Data Time (tIDH) and the next activity of Input Ready (tIRL) to be extended relative to Shift-In going High.

[†] This is an absolute voltage with respect to device GND (Pin 8 or 9) and includes all overshoots due to test equipment.



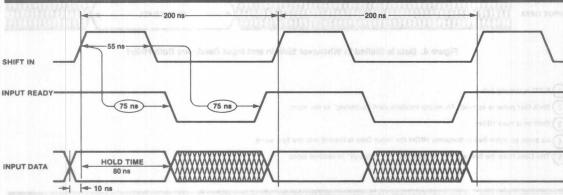
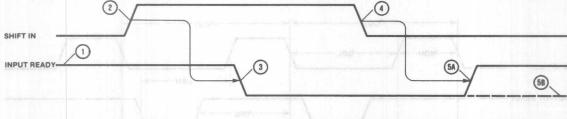


Figure 2. Typical Waveforms for 5-MHz Shift In Data Rate



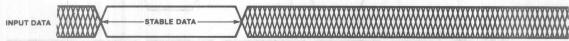


Figure 3. The Mechanism of Shifting Data Into the FIFO

- 1 Input Ready HIGH indicates space is available and a Shift In pulse may be applied.
- (2) Input Data is loaded into the first word.
- 3 Input Ready goes LOW indicating the first word is full.
- (4) The Data from the first word is released for "fall-through" to second word.
- (5A) The Data from the first word is transferred to second word. The first word is now empty as indicated by Input Ready HIGH.
- (58) If the second word is already full then the data remains at the first word. Since the FIFO is now full Input Ready remains low.

 NOTE: Shift In pulses applied while Input Ready is LOW will be ignored (See Figure 5).

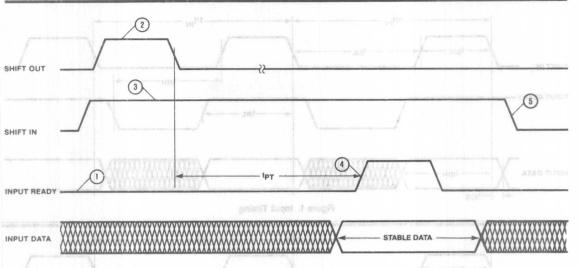
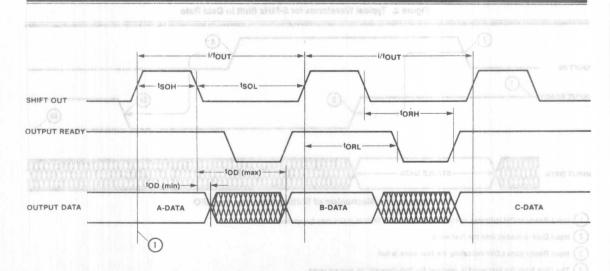


Figure 4. Data is Shifted in Whenever Shift In and Input Ready are Both HIGH

- 1) FIFO is initially full.
- (2) Shift Out pulse is applied. An empty location start "bubbling" to the front.
- 3 Shift In is held HIGH.
- (4) As soon as Input Ready becomes HIGH the Input Data is loaded into the first word.
- (5) The Data from the first word is released for "fall through" to second word.



1 The diagram assumes, that at this time, words 63, 62, 61 are loaded with A, B, C Data, respectively

Figure 5. Output Timing



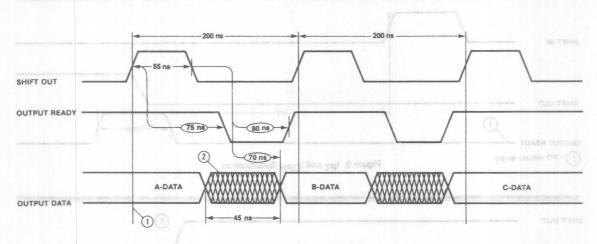


Figure 6. Typical Waveform for 5 MHz Shift Out Data Rate

- 1) The diagram assumes, that at this time, words 63, 62, 61 are loaded with A, B, C Data, respectively.
- 2 Data in the crosshatched region may be A or B Data

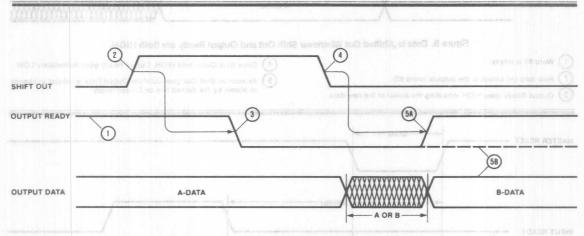
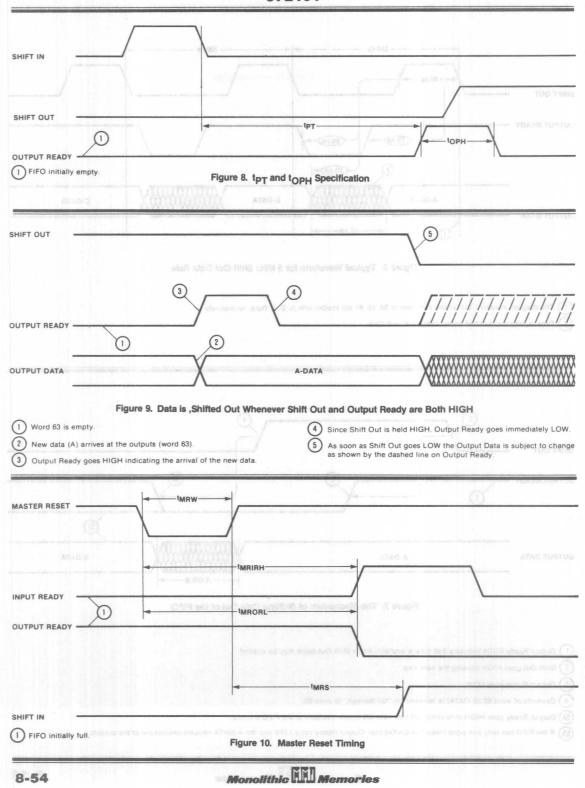


Figure 7. The Mechanism of Shifting Data Out of the FIFO

- 1) Output Ready HIGH indicates that data is available and a Shift Out pulse may be applied.
- 2) Shift Out goes HIGH causing the next step.
- (3) Output Ready goes LOW.
- (4) Contents of word 62 (B-DATA) is released for "fall through" to word 63.
- (5A) Output Ready goes HIGH indicating that new data (B) is now available at the FIFO outputs.
- (5B) If the FIFO has only one word loaded (A-DATA) then Output Ready stays LOW and the A-DATA remains unchanged at the outputs.



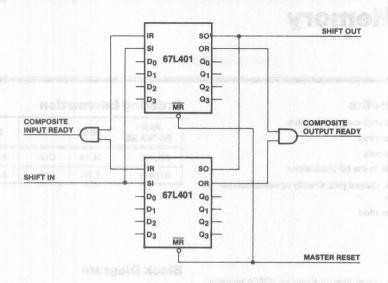
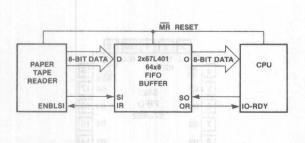


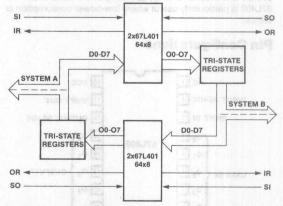
Figure 12. 64x8 FIFO With Two 67L401's

FIFOs are expandable in depth and width. However, in forming wider words two external gates are required to generate composite Input and Output Ready flags. This need is due to the different fall through times of the FIFOs.

Applications

FIFOs are typically used as temporary data buffers between mismatching data rates. Such an application is shown in Figure 13. The 67L401 can also be used in a bidirectional operation as shown in Figure 14.





NOTE: Both depth and width expansion can be used in this mode.

Figure 13. FIFO As Data Buffer Between Slow Steady Rate and Fast 'Burst' Rate

Figure 14. Bidirectional FIFO Application

Low Power First-In First-Out (FIFO) 64x5 Memory 67L402

Features/Benefits

- Guaranteed 5 MHz shift-out/shift-in rates
- Low power consumption
- TTL inputs and outputs
- · Readily expandable in the bit dimensions
- Structured pinouts. Output pins directly opposite corresponding input pins
- Asynchronous operation

Ordering Information

	PART PACKAGE	PKG	TEMP	DESCRIPTION
-	67L402	N, NL	Com	5 MHz 64x5 FIFO
	67L402	J, NL	Com	5 MHz 64x5 FIFO

Description

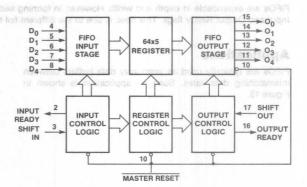
The 67L402 is a low-power First-In First-Out (FIFO) memory device with TTL speed. This device is organized in a 64x5-bit structure and easily expandable to any width. A 5 MHz data rate with fast "fall through" time allows usage in tape and disc controllers, printers and communications buffer applications. This data rate is much faster than a comparable MOS device. The FIFO is a register-based device. Data entered at the inputs "falls through" to the empty space closest to the output. Data is shifted out in the same sequence it is shifted in. Also, the width can be increased by putting the Input Ready signals through an AND gate to give a composite Input Ready. Similarly, the Output Ready signals should be gated to form a composite Output Ready.

Generally, FIFOs are used in digital systems performing data transfers when source and receiver are not operating at the same data rate. FIFOs are also used as data buffers where the source and receiver are not operating at the same time. The 67L402 is particularly useful where low-power consumption is critical

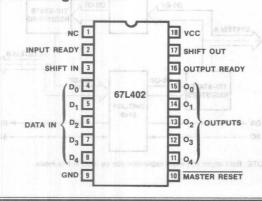
Block Diagram

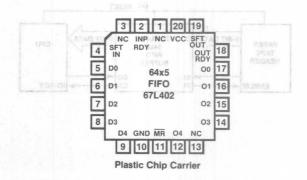
571,401

67L402 64x5



Pin Configurations





TWX: 910-338-2376

Monolithic MMI Memories

Absolute Maximum Ratings

Supply voltage V _{CC}	0.5 V to 7 V
Input voltage	
Off-state output voltage	0.5 V to 5.5 V
Storage temperature	-65° to +150° C

Operating Conditions

SYMBOL	PARAMETER	FIGURE	MIN	COMMERCIAL TYP MAX	UNIT
Vcc	Supply voltage		4.75	5 5.25	V
TA	Operating free-air temperature	V.	000	memo augm a ver-75	°C
tSIH†	Shift in HIGH time	1	55	Inempo (popi i umpor/	ns
tSIL tsi	Shift in LOW time	10 1	55	alignos trighto lesal-wort	ns
tIDS	Input data setup	10 1	10	Pagar-les el output vonaga	ns
^t IDH	Input data hold time	1	80	Have an out-of-come and income	ns
tsoH†	Shift Out HIGH time	5	55	suppry current	ns
tSOL	Shift Out LOW time	5 4 9	55	navia a la barrarla ed blunde sugue ano m	ns
^t MRW	Master Reset pulse	10	40	Sifey sames of pergen flink obston as los	ns
^t MRS	Master Reset to SI	10	35		ns

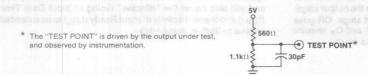
Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	FIGURE	MIN	COMMERCIAL TYP	MAX	UNIT
fIN	Shift in rate	1 18	5	one al (S) nt flind on	t rathe notice	MHz
t _{IRL} †	Shift in to Input Ready LOW	1 787		n steU WOJeg of FR	10	ns
t _{IRH} †	Shift in to Input Ready HIGH	1		21 go HIGH, Indicatin	7.5	ns
four	Shift Out rate	5	0	aly, data will propaga	a Simultaniou	MHz
tORL†	Shift Out to Output Ready LOW	5	merodice sen	State to company of those to	75	ns
tORH†	Shift Out to Output Ready HIGH	5 W	OJ nierder tile	ne memory is full, IR v	80	ns
todh	Output Data Hold (previous word)	5	8		redene	ns
tops	Output Data Shift (next word)	5 44	rensfer of any	siti, kao bingges crit i	56 70 mm	ns
t _{PT}	Data throughput or "fall through"	4, 8	motes at ite	Ownstream) simply o	4	μs
†MRORL	Master Reset to OR LOW	10	d ent of faldd	d" like enotispet vign	95	ns
t _{MRIRH}	Master Reset to IR HIGH	10	o bravia from i	ued for the first data t	85	ns
t _{IPH}	Input Ready pulse HIGH	4	20	A STATE OF THE STATE OF	Or	ns
^t OPH	Output Ready pulse HIGH	8	20		300030	ns

[†] See AC test and application note.

Test Load "Into shir tess it is test with the roof to no flut point

^{*} The "TEST POINT" is driven by the output under test, and observed by instrumentation.



Input Pulse 0 to 3 V Input Rise and Fall Time (10% - 90%) 5 ns minimum

SYMBOL	PARAMETER			TEST CONDITIONS		MIN TYP	MAX	UNIT
VIL	Low-level inpu	t voltage				Sterilands	0.8	٧
VIH	High-level inpu	ut voltage			enoi	2†	all and	V
VIC	Input clamp vo	oltage	V _{CC} = MIN	I _I = -18mA			-1.5	٧
I _{IL1}	Low-level	D ₀ -D ₃ MR	VMAY		JW, USAY		-0.8	mA
I _{IL2}	input current	SI, SO	V _{CC} = MAX	V _I = 0.45V		ov vdcbu3	-1.6	mA
liH.	High-level inpu	ut current	V _{CC} = MAX	V _I = 2.4V	n ia-en	Operating	50	μΑ
I _L	Maximum inpu	it current	V _{CC} = MAX	V _I = 5.5V	amit Hill	Endton H	1	mA
VOL	Low-level outp	ut voltage	V _{CC} = MIN	I _{OL} = 8mA	instruction	Lalaire i	0.5	V
VOH	High-level outp	out voltage	V _{CC} = MIN	I _{OH} = -0.9mA	ra (166) s	2.4	- T	V
los	Output short-c	ircuit current*	V _{CC} = MAX	V ₀ = 0V	e rei besel	-20	-90	mA
Icc	Supply Curren	t	V _{CC} = MAX In	puts Low, Outputs Open	A -6 HOW	113	130	mA

^{*} Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

Functional Description Data Input

After power up the Master Reset is pulsed low (Fig. 11) to prepare the FIFO to accept data in the first location. When Input Ready (IR) is HIGH the location is ready to accept data from the D_X inputs. Data then present at the data inputs is entered into the first location when the Shift In (SI) is brought HIGH. A SI HIGH signal causes the IR to go LOW. Data remains at the first location until SI is brought LOW. When SI is brought LOW and the FIFO is not full, IR will go HIGH, indicating that more room is available. Simultaneously, data will propagate to the second location and continue shifting until it reaches the output stage or a full location. The first word is present at the outputs before a shift out is applied. If the memory is full, IR will remain LOW.

Data Transfer

Once data is entered into the second cell, the transfer of any full cell to the adjacent (downstream) empty cell is automatic, activated by an on-chip control. Thus data will stack up at the end of the device while empty locations will "bubble" to the front. tp¬ defines the time required for the first data to travel from input to the output of a previously empty device.

Data Output

Data is read from the O_X outputs. When data is shifted to the output stage, Output Ready (OR) goes HIGH, indicating the presence of valid data. When the OR is HIGH, data may be shifted out by bringing the Shift Out (SO) HIGH. A HIGH signal at SO causes the OR to go LOW. Valid data is maintained while the SO is HIGH. When SO is brought LOW the upstream data, provided that stage has valid data, is shifted to the output stage. When new valid data is shifted to the output stage, OR goes HIGH. If the FIFO is emptied, OR stays LOW, and O_X remains as before, (i.e. data does not change if FIFO is empty).

Input Ready and Output Ready may also be used as status signals indicating that the FIFO is completely full (Input Ready stays LOW for at least tpt) or completely empty (Output Ready stays LOW for at least tpt).

AC Test and Application Note

Since the FIFO is a high-speed device, care must be exercised in design of the hardware and the timing. Though the external data rate is 5 MHz, internally the device is several times as fast. Device grounding and decoupling is crucial to correct operation, as the FIFO is sensitive to very small glitches caused by long reflective lines, high capacitances, and/or poor supply decoupling and grounding. We recommend a monolithic ceramic capacitor of 0.1 µF directly between VCC and GND with a very short lead length. In addition, care must be exercised in timing setup and measurement of parameters. For example, since an AND gate function is associated with both the Shift In-Input Ready Combination as well as the Shift Out-Output Ready Combination. timing measurements may be misleading, i.e., rising edge of the Shift-In pulse is not recognized until Input-Ready is High. If Input-Ready is not high due to too high a frequency, or the FIFO being full or affected by Master Reset, the Shift-In activity will be ignored. This will affect the device from a functional standpoint. and will also cause the "effective" timing of Input Data Time (t_{IDH}) and the next activity of Input Ready (t_{IRL}) to be extended relative to Shift-In going High.

[†] This is an absolute voltage with respect to device GND (Pin 8 or 9) and includes all overshoots due to test equipment.



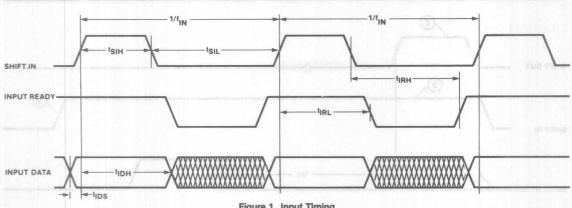


Figure 1. Input Timing

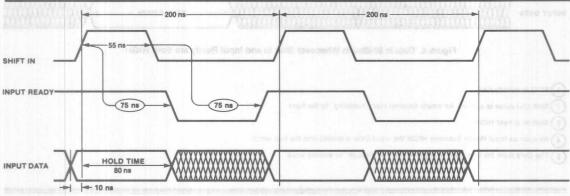


Figure 2. Typical Waveforms for 5 MHz Shift in Data Rate

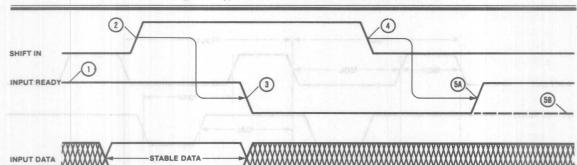


Figure 3. The Mechanism of Shifting Data into the FIFO

- (1) Input Ready HIGH indicates space is available and a Shift In pulse may be applied.
- 2 Input Data is loaded into the first word.
- 3 Input Ready goes LOW indicating the first word is full.
- (4) The Data from the first word is released for "fall-through" to second word.
- (5A) The Data from the first word is transferred to second word. The first word is now empty as indicated by Input Ready HIGH.
- (58) If the second word is already full then the data remains at the first word. Since the FIFO is now full Input Ready remains low. NOTE: Shift In pulses applied while Input Ready is LOW will be ignored (See Figure 5).

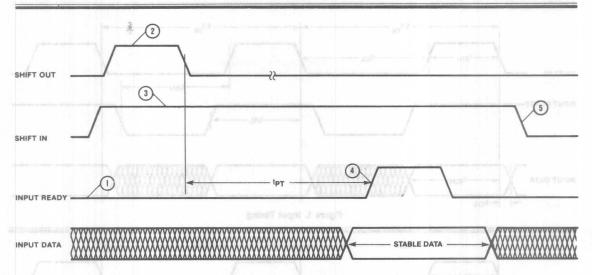
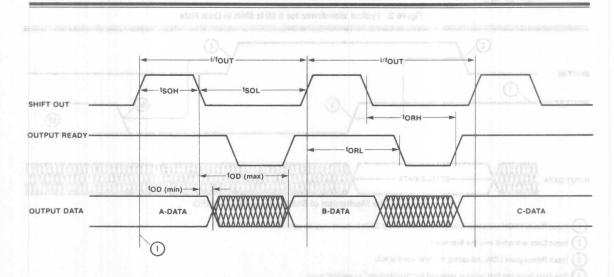


Figure 4. Data is Shifted in Whenever Shift In and Input Ready are Both HIGH

- 1) FIFO is initially full.
- 2 Shift Out pulse is applied. An empty location start "bubbling" to the front.
- 3 Shift In is held HIGH
- (4) As soon as Input Ready becomes HIGH the Input Data is loaded into the first word.
- (5) The Data from the first word is released for "fall through" to second word.



1 The diagram assumes, that at this time, words 63, 62, 61 are loaded with A. B. C Data, respectively

Figure 5. Output Timing



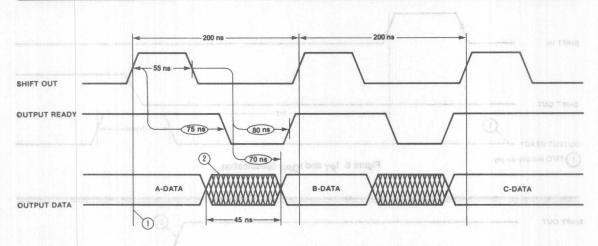


Figure 6. Typical Waveform for 5 MHz Shift Out Data Rate

- 1) The diagram assumes, that at this time, words 63, 62, 61 are loaded with A, B, C Data, respectively.
- (2) Data in the crosshatched region may be A or B Data

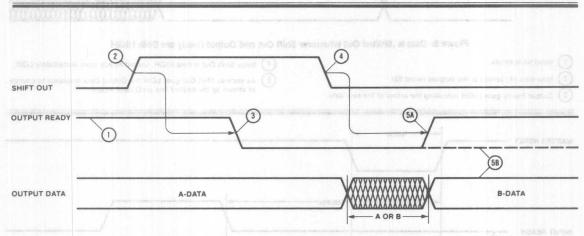
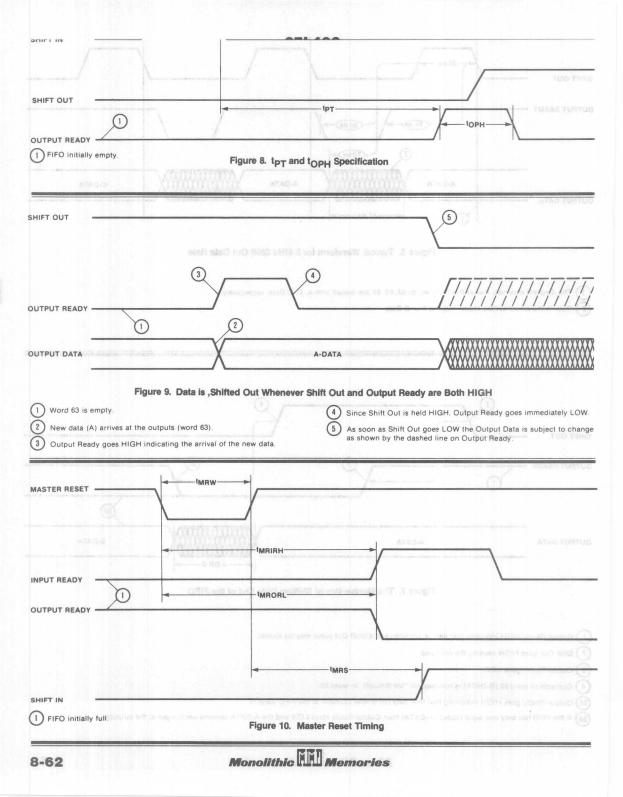


Figure 7. The Mechanism of Shifting Data Out of the FIFO

- 1) Output Ready HIGH indicates that data is available and a Shift Out pulse may be applied.
- 2) Shift Out goes HIGH causing the next step.
- (3) Output Ready goes LOW.
- (4) Contents of word 62 (B-DATA) is released for "fall through" to word 63.
- (5A) Output Ready goes HIGH indicating that new data (B) is now available at the FIFO outputs.
- (58) If the FIFO has only one word loaded (A-DATA) then Output Ready stays LOW and the A-DATA remains unchanged at the outputs.



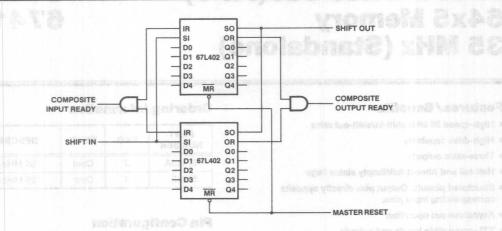


Figure 11. 64x8 FIFO With 67L402's

FIFOs are expandable in depth and width. However, in forming wider words two external gates are required to generate composite Input and Output Ready flags. This need is due to the different fall through times of the FIFOs.

Applications

FIFOs are typically used as temporary data buffers between mismatching data rates. Such an application is shown in Figure 12. The 67LS402 can also be used in a bidirectional operation as shown in Figure 13.

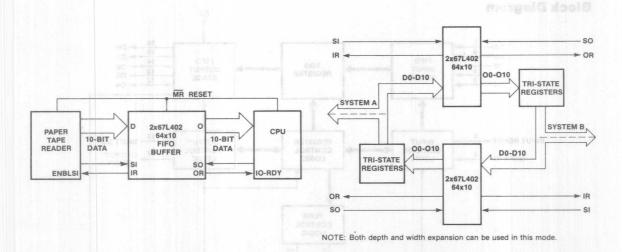


Figure 12. FIFO As Data Buffer Between Slow Steady Rate and Fast 'Burst' Rate

Figure 13. Bidirectional FIFO Application

First-In First-Out (FIFO) 64x5 Memory 35 MHz (Standalone)

67413A 67413

Features/Benefits

- · High-speed 35 MHz shift-in/shift-out rates
- High-drive capability
- Three-state outputs
- Half-full and Almost-full/Empty status flags
- · Structured pinouts. Output pins directly opposite corresponding input pins.
- Asynchronous operation
- TTL-compatible inputs and outputs

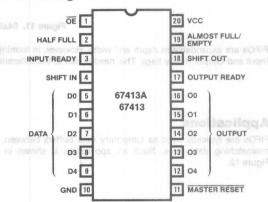
Description

The 67413A is a high-speed, 64x5 First-In-First-Out (FIFO) memory which operates at 35-MHz input/output rates (67413 operates at 25-MHz in-out). The data is loaded and emptied on a first-in-first-out basis. It is a three-state device with high-drive (IOI = 24 mA) data outputs. These devices can be connected in parallel to give FIFOs of any word length. It has a Half-full flag (thirty-two or more words full) and an almost full/empty flag (fifty-six or more words or eight or less words). The main applications of 67413A, 67413 are rate buffers; sourcing and absorbing data at different rates. Other applications are high-speed tape and disk controllers, data communications systems and plotter control systems.

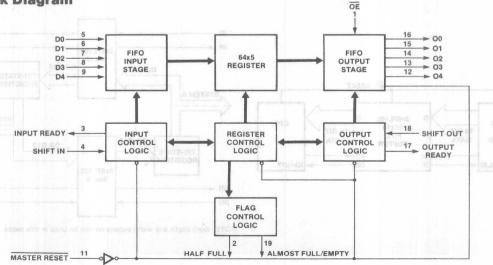
Ordering Information

PART NUMBER	PKG	TEMP	DESCRIPTION
67413A	J	Com	35 MHz-in/out
57413	J	Com	25 MHz-in/out

Pin Configuration



Block Diagram



TWX: 910-338-2376
2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2374

Memories

B

Absolute Maximum Ratings and the control of the con

Supply voltage V _{CC}	0.5 to 7 V
Input voltage	1.5 to 7 V
Off-state output voltage	0.5 to 5.5 V
Storage temperature	-65°C to +150°C

67413A Operating Conditions Over Temperature Range

SYMBOL	PARAMETER	FIGURE	MIN	COMMERCIAL MAX	UNIT
Vcc	Supply voltage		4.75	5 5.25	V
TA	Operating free-air temperature		0	75	°C
tSIH [†]	Shift in HIGH time	1	9	Mark Charles And	ns
t _{SIL} †	Shift in LOW time	1	17	1000 8 0110 1111	ns
tIDS	Input data set up	1	2	Ostpur Disable Delay	ns
tIDH	Input data hold time	1	15		ns
tson†	Shift Out HIGH time	5	9	Output Enable Delay	ns
tsol	Shift Out LOW time	5	17		ns
^t MRW	Master Reset pulse †	10	30	(15 may out fall 1 to (15 m 10 m) * 2.5 ps.	ns
tMRS	Master Reset to SI	10	35		ns

67413A Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER Am 8	FIGURE	MIN	TYP	MAX	UNIT
fIN	Shift in rate	1	DC DC		††30 †††35	MHz
t _{IRL} †	Shift In 1 to Input Ready LOW	1		12	18	ns
t _{IRH} †	Shift In I to Input Ready HIGH	1		14	20	ns
four	Shift Out rate	5 20%	DC DC	e Pulse Argulude – A Pire and Fall Timo A Pire and Fall Timo	††30 †††35	MHz
tORL†	Shift Out 1 to Output Ready LOW	5		12	18	ns
tORH†	Shift Out ↓ to Output Ready HIGH	5		14	20	ns
todh†	Output Data Hold (previous word)	5	12			ns
tods	Output Data Shift (next word)	5			34	ns
t _{PT}	Data throughput or "fall through"	4,8	108.5	510	650	ns
†MRORL	Master Reset I to Output Ready LOW	10		18	28	ns
t _{MRIRH}	Master Reset 1 to Input Ready HIGH	10	3	21	28	ns
t _{MRIRL}	Master Reset ↓ Input Ready LOW*	10		18	28	ns
^t MRO	Master Reset I to Outputs LOW	10		32	45	ns

Note: Typicals at 5 V VCC and 25°C TA.

* If the FIFO is not full (IR High), MR low forces IR low, followed by IR returning high when MR goes high.

† See AC test and high-speed application note.

†† Tested

††† Guaranteed by design (see test load).

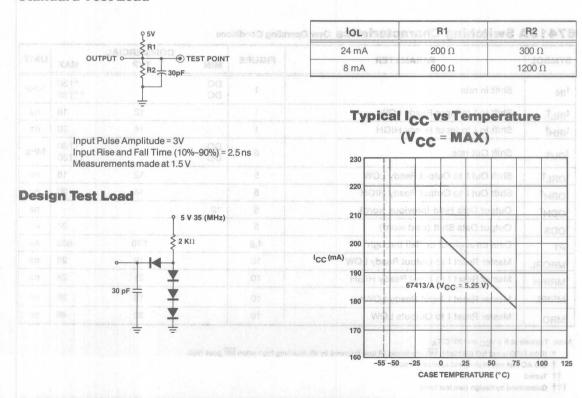
67413A Switching Characteristics Over Operating Conditions (continued)

SYMBOL	PARAMETER	FIGURE	MIN TYP	MAX	UNIT
tiph o	Input ready pulse HIGH	4	. 5	eqma)	ns
^t OPH	Output ready pulse HIGH	8	5 12		ns
tORD	Output ready † HIGH to Data Valid	5	V 4 V 10 10 10 10 10 10	18	ns
tAEH*	Shift Out 1 to AF/E HIGH	11	100	135	ns
tAEL*	Shift In 1 to AF/E LOW	11	язтаманан 450	600	ns
t _{AFL} *	Shift Out 1 to AF/E LOW	12	450	600	ns
t _{AFH} *	Shift In 1 to AF/E HIGH	12	100	135	ns
tHFH*	Shift In 1 to HF HIGH	13	280	360	ns
tHFL*	Shift Out 1 to HF LOW	13	280	360	S
t _{PHZ}	Output Disable Dales	А	14	25	ns
t _{PLZ}	Output Disable Delay	А	14	25	ns
t _{PZL}	Output Enghla Dalay	А	14	25	ns
t _{PZH}	Output Enable Delay	Α	24	38	ns

Note: Input rise and fall time (10%-90%) = 2.5 ns. * See timing diagram for explanation of parameters.

67413A/67413

Standard Test Load



8

Absolute Maximum Ratings (a) and allowed goldested and authorized and allowed & A.T.

Supply voltage V _{CC}	0.5 V to 7 V
Input voltage	1.5 V to 7 V
Off-state output voltage	0.5 V to 5.5 V
Storage temperature	65° to +150° C

67413 Operating Conditions Over Temperature Range

SYMBOL	PARAMETER	12	FIGURE	MIN	COMMERCIAL	MAX	UNIT
VCC	Supply voltage	5.1		4.75	5	5.25	V
TA	Operating free-air temperature			0	THE PARTY OF THE P	75	°C
t _{SIH} †	Shift in HIGH time	0	1 1	16	MANUAL MARKET TOTAL TOTAL	THE .	ns
t _{SIL} †	Shift in LOW time		1	20	to: Disable Delay-	uo 👆	ns
t _{IDS}	Input data set up		1	3			ns
t _{IDH}	Input data hold time	A	1	25	tour Englise Delay	a0 L	ns
t _{SOH} †	Shift Out HIGH time		5	16			ns
tSOL	Shift Out LOW time		5	20	eg to no manajoka isa mg	e a grant Le	ns
^t MRW	Master Reset pulse †		10	35			ns
^t MRS	Master Reset to SI		10	35			ns

67413 Switching Characteristics Over Temperature Range

SYMBOL	PARAMETER	FIGURE	MIN	COMMERCIAL TYP	MAX	UNIT
fIN	Shift in rate	1	DC		25	MHz
t _{IRL} †	Shift In 1 to Input Ready LOW	1		12	28	ns
t _{IRH} †	Shift In 1 to Input Ready HIGH	1		14	25	ns
four	Shift Out rate	5	. DC		25	MHz
tORL†	Shift Out 1 to Output Ready LOW	5		12	28	ns
tORH†	Shift Out ↓ to Output Ready HIGH	5		14	25	ns
tODH [†]	Output Data Hold (previous word)	5	10			ns
tods	Output Data Shift (next word)	5			40	ns
t _{PT}	Data throughput or "fall through"	4,8		510	750	ns
†MRORL	Master Reset ↓ to Output Ready LOW	10		18	30	ns
tMRIRH	Master Reset † to Input Ready HIGH	10		21	30	ns
t _{MRIRL}	Master Reset ↓ Input Ready LOW*	10		18	30	ns
^t MRO	Master Reset ↓ to Outputs LOW	10		32	55	ns

Note: Typicals at 5 V VCC and 25°C TA.

^{*} If the FIFO is not full (IR High), $\overline{\text{MR}}$ low forces IR low, followed by IR returning high when $\overline{\text{MR}}$ goes high.

[†] See AC test and high-speed application note.

SYMBOL	PARAMETER	FIGURE		ERCIAL (P	MAX	UNIT
t _{IPH}	Input ready pulse HIGH	4	5	2	100fte	ns
^t OPH	Output ready pulse HIGH	8	5	2	stegmor	ns
tORD	Output ready † HIGH to Data Valid	5	7		20	ns
t _{AEH} *	Shift Out ↑ to AF/E HIGH	11		00	145	ns
t _{AEL} *	Shift In 1 to AF/E LOW	11	4	50	650	ns
t _{AFL} *	Shift Out 1 to AF/E LOW	12	RETERIARNS 4	50	650	ns
t _{AFH} *	Shift In 1 to AF/E HIGH	12	man adoption in the same of	00	145	ns
t _{HFH} *	Shift In 1 to HF HIGH	13	2	80	380	ns
tHFL*	Shift Out 1 to HF LOW	13	2	80	380	ns
t _{PHZ}	Output Disable Delay	А		4	30	ns
tPLZ	Output Disable Delay	A		4	30	ns
t _{PZL}	Output Enable Delay	А	an al	4	30	ns
t _{PZH}	Output Enable Delay	A	2	24	50	ns

Note: Input rise and fall time (10%-90%) = 2.5 ns.

* See timing diagram for explanation of parameters.

87413 Switteling Chi actorisics our respenses Benge

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					25	
		10				

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	i il alcilizgati	MIN TYP M	XA	UNIT			
V _{IL}	Low-level input voltage	se rasidaria h	0.	8†	V			
VIH	High-level input voltage	TOCH STATE OUT	2†	Mil	V			
VIC	Input clamp voltage	V _{CC} = MIN I _I = -18 mA				Lucio religio	1.5	٧
IL	Low-level input current	V _{CC} = MAX	V _I = 0.45 V	-2	250	μΑ		
IH	High-level input current	V _{CC} = MAX	V _I = 2.4 V				50	μΑ
I	Maximum input current	V _{CC} = MAX	V _I = 5.5 V				1	mA
/	V _{OL} Low-level output voltage		I _{OL} (Data outputs)	67413A 67413	24 mA	W.	700	
V _{OL}		Low-level output voltage V _{CC} =	V _{CC} = MIN	I _{OL} (IR, OR)	67413A 67413	8 mA††	l d	0.5
AL VANCO.	WATER AT	I _{OL} (Flag outputs)	67413A 67413	8 mA		ATP AT	water.	
VOH	High-level output voltage	V _{CC} = MIN	IOH (Data outputs)	67413A 67413	-3.0 mA	L. V. Name		V
			I _{OH} (IR,OR)		-0.9 mA	2.4		
			IOH (Flag outputs)		-0.9 mA			
los	Output short-circuit current*	V _{CC} = MAX	V _O = 0 V			-20 -	90	mA
I _{HZ}	0#	V _{CC} = MAX	$\begin{array}{c c} IAX & V_O = 2.4 V \\ IAX & V_O = 0.4 V \end{array}$			+	20	μΑ
ILZ	Off-state output current	V _{CC} = MAX				J	20	μΑ
lcc	Supply current	V _{CC} = MAX. All inputs low. All outputs open. (67413A/67413)				**2	40	mA

^{*} Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

Functional Description

Data Input

After power up the Master Reset is pulsed low (Figure 10) to prepare the FIFO to accept data in the first location. Master Reset must be applied prior to use to ensure proper operation. When Input Ready (IR) is HIGH the first location is ready to accept data from the Dx inputs. Data then present at the data inputs is entered into the first location when the Shift-In (SI) is brought HIGH. A SI HIGH signal causes the IR to go LOW. Once data is entered into the first cell, the transfer of data in any full cell to the adjacent (downstream) empty cell is automatically activated by an on-chip control. Thus data will stack up at the end of the device (while empty locations will "bubble" to the front when data is shifted out). tpT defines the time required for the first data to travel from input to the output of a previously empty device. When SI is brought LOW and the FIFO is not full, IR will go HIGH, indicating more room is available. If the memory is full, IR will remain LOW.

Data Output

Data is read from the ${\sf O}_{\sf X}$ outputs. When data is shifted to the output stage, Output Ready (OR) goes HIGH, indicating the

presence of valid data. When the OR is HIGH, data may be shifted out by bringing the Shift Out (SO) HIGH. A HIGH signal at SO causes the OR to go LOW. Valid data is maintained while the SO is HIGH. When SO is brought LOW the upstream data, provided that there is valid upstream data, is shifted to the output stage. When new valid data is shifted to the output stage, OR goes HIGH. If the FIFO is emptied, OR stays LOW and Data output will not be valid.

Input Ready and Output Ready may also be used as status signals indicating that the FIFO is completely full (Input Ready stays LOW for at least tp_T) or completely empty (Output Ready stays LOW for at least tp_T).

AC Test and High-Speed App. Notes

Since the FIFO is a very-high-speed device, care must be exercised in the design of the hardware and the timing utilized within the design. The internal shift rate of the FIFO typically exceeds 60 MHz in operation. Device grounding and decoupling is crucial to correct operation as the FIFO will respond to very small glitches due to long reflective lines, high capacitances and/or poor supply decoupling and grounding. Monolithic Memories recommends a monolithic ceramic capacitor of 0.1 $\mu \rm F$ directly between VCC and GND with very short lead length. In addition,

^{**} See curve for I_{CC} vs. temp.

[†] There are absolute voltages with respect to GND (PIN 8 or 9) and includes all overshoots due to test equipment.

^{††} Care should be taken to minimize as much as possible the DC and capacitive load on IR and OR when operating at frequencies above 25 MHz.

care must be exercised in how the timing is set up and how the parameters are measured. For example, since an AND gate function is associated with both the Shift-In-Input Ready combination, as well as the Shift-Out-Output Ready combination, timing measurements may be misleading, i.e., rising edge of the Shift-In pulse is not recognized until Input Ready is HIGH. If Input Ready is not high due to (a) too high a frequency, or (b) FIFO being full or effected by Master Reset, the Shift-In activity

will be ignored. This will affect the device from a funcitonal standpoint, and will also cause the "effective" timing of Input Data Hold time ($T_{\rm IDH}$) and the next activity of Input Ready ($T_{\rm IRL}$) to be extended relative to Shift-ingoing HIGH. This same type of problem is also related to $T_{\rm IRH}$, $T_{\rm ORL}$ and $T_{\rm ORH}$ as related to Shift-Out. Data outputs driving a bus should be limited to 10 MHz frequency. For high-speed applications, proper grounding technique is essential.

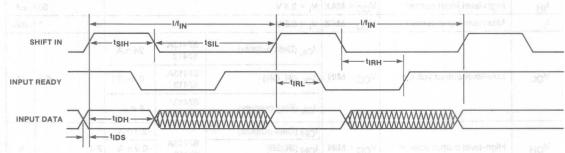


Figure 1. Input Timing

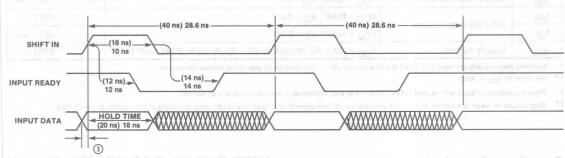


Figure 2. Typical Waveforms for 35 MHz Shift-In Data Rate (67413A)

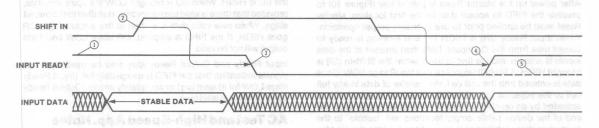


Figure 3. The Mechanism of Shifting Data into the FIFO

- 1 Input Ready HIGH indicates space is available and a Shift-In pulse may be applied.
- 2 Input Data is loaded into the first word. The Data from the first word is released for "fall-through" to second word.
- 3 Input Ready goes LOW indicating the first word is full.
- Shift-In going LOW allows Input Ready to sense the status of first word: The first word is now empty as indicated by Input Ready HIGH.
- 5. If the second word is already full then the data remains at the first word. Since the FIFO is now full Input Ready remains low.

 Note: Shift-In pulses applied while Input Ready is LOW will be ignored (See Figure 5).

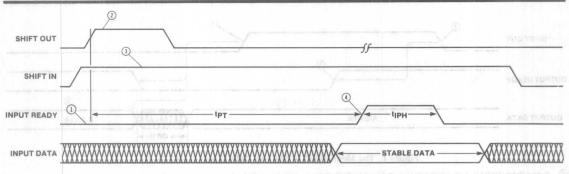


Figure 4. Data is Shifted in Whenever Shift In and Input Ready are Both HIGH

- 1 FIFO is initially full.
- ② Shift Out pulse is applied. An empty location starts "bubbling" to the front.
- 3 Shift In is held HIGH
- 4 As soon as Input Ready becomes HIGH the Input Data is loaded into the first word.

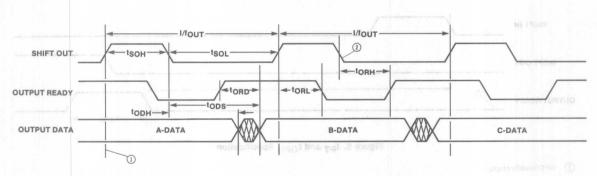


Figure 5. Output Timing

- 1 The diagram assumes that at this time, words 63, 62 and 61 are loaded with A, B and C Data, respectively.
- (2) Output data changes on the falling edge of SO after a valid Shift-Out Sequence, i.e. OR and SO are both high together.

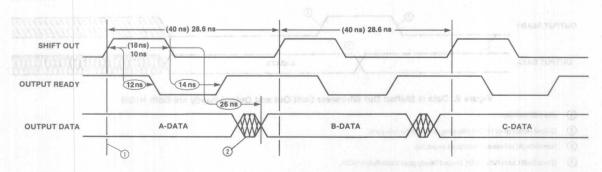


Figure 6. Typical Waveforms for 35 MHz Shift-Out Data Rate (67413A)

- 1 The diagram assumes that at this time words 63, 62 and 61 are loaded with A, B and C Data, respectively.
- 2 Data in the first crosshatched region may be A or B Data.

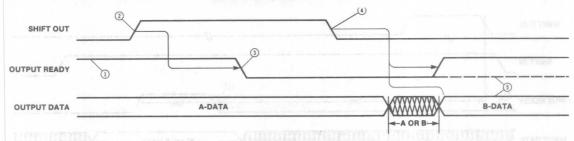


Figure 7. The Mechanism of Shifting Data Out of the FIFO

- ① Output Ready HIGH indicates that data is available and a Shift-Out pulse may be applied.
- Shift-Out goes HIGH causing the contents of word 62 (B-Data) to be released for fall-through to word 63. Output data remains as valid A-Data while Shift-Out is HIGH.
- 3 Output Ready goes LOW.
- 4 Shift-out goes LOW causing Output Ready to go HIGH and new data (B) to appear at the data outputs.
- (5) If the FIFO has only one word loaded (A-Data) then Output Ready stays LOW and the output data becomes invalid.

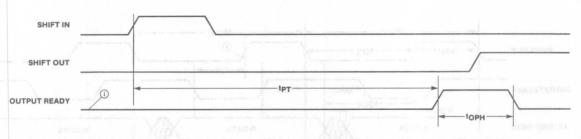


Figure 8. tpT and toPH Specification

FIFO initially empty.

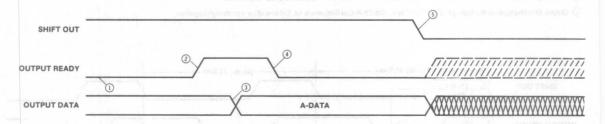


Figure 9. Data is Shifted Out Whenever Shift Out and Output Ready are Both HIGH

- (1) Word 63 is empty.
- Output Ready goes HIGH indicating arrival of the new data.
- 3 New data (A) arrives at the outputs (word 63).
- Since Shift Out is held HIGH, Output Ready goes immediately LOW.
- As soon as Shift Out goes LOW the Output Data is subject to change. Output Ready will go HIGH or LOW depending on whether there are any additional upstream words in the FIFO.



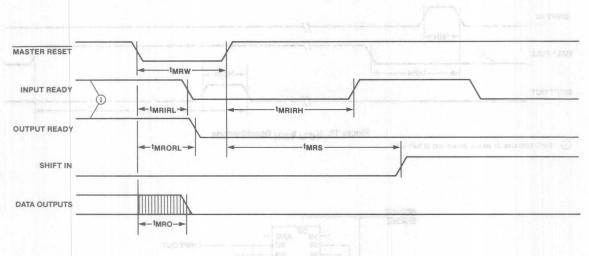


Figure 10. Master Reset Timing

1 FIFO is partially full.

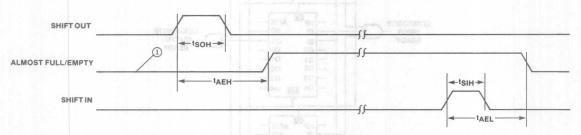


Figure 11. t_{AEH}, t_{AEL} Specifications

1) FIFO contains 9 words (one more than almost empty).

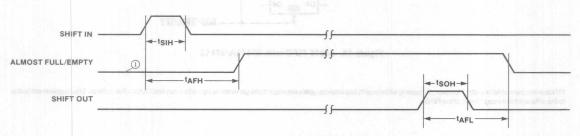
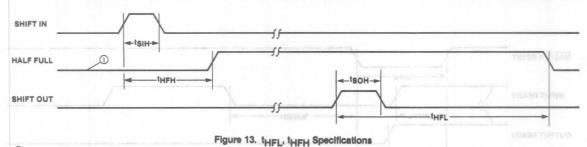


Figure 12. t_{AFH}, t_{AFL} Specifications

1 FIFO contains 55 words (one short of almost full)



1 FIFO contains 31 words (one short of half full).

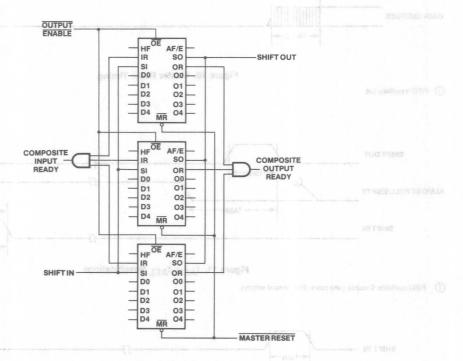


Figure 14. 64x15 FIFO with 67413A/67413

FIFOs are expandable in width. However, in forming wider words two external gates are required to generate composite Input and Output Ready flags. This requirement is due to the different fall through times of the FIFOs.



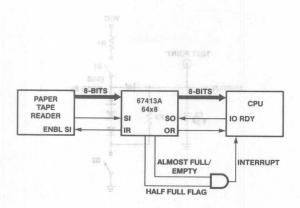
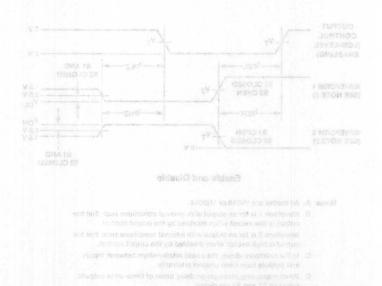


Figure 15. Application for 67413A "Slow and Steady Rate to Fast 'Blocked Rate'"

Note: Cascading the FIFO's in word width is done by ANDing the IR and OR as shown in Figure 14.

Dealgn Test Load



Three-State Test Load

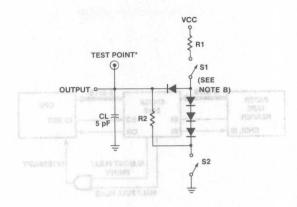
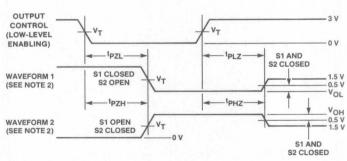


Figure 15. Application for 67410A, "Slow and Stendy Rate to Fast "Horized Rate"."

Design Test Load



Enable and Disable

Notes: A. All diodes are 1N916 or 1N3064.

- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

 Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
- D. When measuring propagation delay times of three-state outputs, switches S1 and S2 are closed.

35 MHz (Standalone)

Features/Benefits

- High-speed 35-MHz shift-in/shift-out rates
- · Choice of 4-bit or 5-bit data width
- · TTL inputs and outputs
- · Readily expandable in word width
- · Structured pinouts. Output pins directly opposite corresponding input pins
- Asynchronous operation
- · Pin-compatible with Fairchild's F3341 MOS FIFO and many times faster

Description

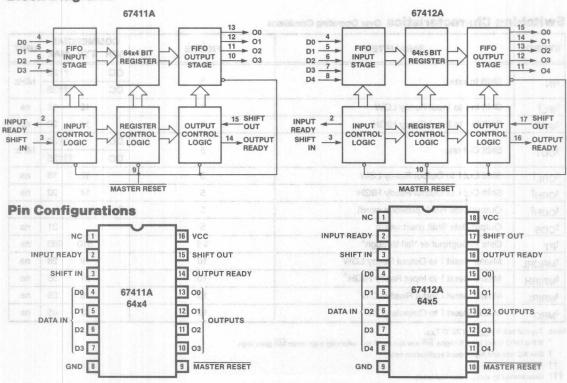
The 67411/2A are "fall-through" high-speed First-In First-Out (FIFO) memory organized 64 words by 4 bits and 64 words by 5 bits respectively. The FIFO is expandable in word width only. It is

Ordering Information

PART NUMBER	PKG	TEMP	DESCRIPTION
67411A	J	Com	35 MHz 64x4 FIFO
67412A	J	Com	35 MHz 64x5 FIFO

the fastest FIFO available on the market. The FIFO is attractive for many applications such as disk controllers, communication buffers, rate buffers, etc.

Block Diagrams



TWX: 910-338-2376

2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2374



Absolute Maximum Ratings

Absolute Maximum Ratings	A A 53
Supply voltage V _{CC}	0.5 V to 7 V
Input voltage	1.5 V to / V
Off-state output voltage	5 V to 5.5 V
Storage temperature ————————————————————————————————————	65° C to +150° C

Features/Benefits

Operating Conditions Over Temperature Range

SYMBOL	PARAMETER	FIGURE	COMMERCIAL MIN TYP MAX	UNIT
VCC	Supply voltage	rithiw b	4.75 5 5.25	V
TA	Operating free-air temperature	pins thecity opposite	Otuo amonio 75	°C
t _{SIH} †	Shift in HIGH time	1	9 A Augal Palbaco	ns
tIDS	Input data set up	1 2000 2000 2000 2000	2	ns
t _{IDH}	Input data hold time	1	14 restat asmit	ns
tsoH [†]	Shift Out HIGH time	5	11	ns
^t MRW	Master Reset pulse †	10	30	ns
t _{MRS}	Master Reset to SI*	2 of almow Labin place A of abrow	35 AS	ns

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER 1 00 00 00 10 10 10 10 10 10 10 10 10 1		NG Asi	COL	MMERC TYP	IAL MAX	UNIT
10 mm	Shift In rate	DI ATE		DC		††30	NALL-
fIN	Shift In rate		A	DC	/1	††35	MHz
t _{IRL} †	Shift In 1 to Input Ready LOW				12	18	ns
t _{IRH} †	Shift In↓ to Input Ready HIGH	THE ST TUTTUC AL	IVEID	SH /	14,9	20	ns
TURILIO BI	Shift Out rate	TURTUO AL SISOLI	SIDO	DC	01810	††30	NAME:
four	Shift Out rate	5	5		DC †††35		MHz
torl†	Shift Out↑ to Output Ready LOW	5	-18		12	18	ns
tORH†	Shift Out↓ to Output Ready HIGH	5	制度	REAM	14	20	ns
tODH†	Output Data Hold (previous word)	5	- 31	9	gara	Timo-	ns
tods	Output Data Shift (next word)	5	-	Property & St. According	1-4	31	ns
t _{PT}	Data throughput or "fall through"	4,8			510	650	ns
^t MRORL	Master Reset ↓ to Output Ready LOW	10			18	28	ns
t _{MRIRH}	Master Reset † to Input Ready HIGH*	10			21	35	ns
^t MRIRL	Master Reset ↓ Input Ready LOW*	100	ATTN	8	18	28	ns
^t MRO	Master Reset I to Outputs LOW	10	735		32	45	ns

Note: Typical at 5 V V_{CC} and 25°C T_{AA}.

* If the FIFO is not full (IR High), MR low forces IR low returning high when MR goes high.

[†] See AC test and high-speed application note.

^{††} Tested.

^{†††} Guaranteed by design (see test load).

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	MEDOPE	TEST CONDIT	ION		MIN TY	PMAX	UNIT		
VIL	Low-level input voltage	Ь		HO	dy enlactiff	- i Judni	0.8†	V		
VIH	High-level input voltage	9 - HOTH salug you						V		
VIC	Input clamp voltage	V _{CC} = MIN I _I = -18 mA				re tug JO	-1.5	V		
IIL	Low-level input current	V _{CC} = MAX V _I = 0.45 V					-50	μΑ		
^I IH	High-level input current	V _{CC} = MAX	X V _I = 2.4 V				50	μΑ		
1	Maximum input current	V _{CC} = MAX	V _I = 5.5 V				1	mA		
V-				V - MINI	I _{OL} (Data Outputs)	67411/2A = 24 mA			0.5	V
VOL	Low-level output voltage	V _{CC} = MIN	I _{OL} (IR, OR)	67411/2A	8 mA ††	I See'l'	0.5	V		
Management	l lieb level entent veltere	ut voltage Vcc = MIN -	IOH (Data Out)	67411/04	-3.0 mA	2.4		V		
VOH	High-level output voltage		I _{OH} (IR,OR)	67411/2A -0.9 mA		2.4		V		
los	Output short-circuit current*	V _{CC} = MAX	V _O = 0 V			-20	-90	mA		
ICC 1 00	Supply current	V _{CC} = MAX.	Inputs low, outputs ope	n (67411/2A)		ec Young	**240	mA		

- * Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- ** See curve for ICC vs. temp.
- † These are absolute voltages with respect to GND (Pin 8 or 9) and includes all overshoots due to test equipment.
- †† Care should be taken to minimize as much as possible the DC and capacitive load on IR and OR when operating at frequencies above 25 MHz.

Functional Description Data Input

After power up the Master Reset is pulsed low (Fig. 10) to prepare the FIFO to accept data in the first location. Master reset must be applied prior to use to ensure proper operation. When Input Ready (IR) is HIGH the first location is ready to accept data from the D_X inputs. Data then present at the data inputs is entered into the first location when the Shift-In (SI) is brought HIGH. A SI HIGH signal causes the IR to go LOW. Once data is entered into the first cell, the transfer of data from any full cell to the adjacent (downstream) empty cell is automatic, activated by an on-chip control. Thus data will stack up at the end of the device while empty locations will "bubble" to the front. tpt defines the time required for the first data to travel from input to the output of a previously empty device. When SI is brought LOW and the FIFO is not full, IR will go HIGH, indicating more room is available. If the memory is full, IR will remain LOW.

Data Output

Data is read from the O_X outputs. When data is shifted to the output stage, Output Ready (OR) goes HIGH, indicating the presence of valid data. When the OR is HIGH, data may be shifted out by bringing the Shift Out (SO) HIGH. A HIGH signal at SO causes the OR to go LOW. Valid data is maintained while the SO is HIGH. When SO is brought LOW the upstream data, provided the upstream stage has valid data, is shifted to the output stage. When new valid data is shifted to the output stage,

OR goes HIGH. If the FIFO is emptied, OR stays LOW and Data output will not be valid.

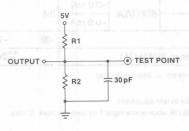
Input Ready and Output Ready may also be used as status signals indicating that the FIFO is completely full (Input Ready stays LOW for at least tp_T) or completely empty (Output Ready stays LOW for at least tp_T).

AC Test and High-Speed App. Notes

Since the FIFO is a very-high-speed device, care must be exercised in the design of the hardware and the timing utilized within the design. The internal shift rate of the FIFO typically exceeds 60 MHz in operation. Device grounding and decoupling is crucial to correct operation as the FIFO will respond to very small glitches due to long reflective lines, high capacitances and/or poor supply decoupling and grounding. Monolithic Memories recommends a monolithic ceramic capacitor of 0.1 μF directly between VCC and GND with very short lead length. In addition, care must be exercised in how the timing is set up and how the parameters are measured. For example, since an AND gate function is associated with both the Shift-In-Input-Ready combination, as well as the Shift-Out-Output-Ready combination, timing measurements may be misleading, i.e., rising edge of the Shift-In pulse is not recognized until Input Ready is HIGH. If Input Ready is not high due to (a) too high a frequency, or (b) FIFO being full or effected by Master Reset, the Shift-In activity will be ignored. This will affect the device from a functional standpoint, and will also cause the "effective" timing of Input

SYMBOL	PARAMETER OFFICION OF TREE	FIGURE	COMMERCIAL MIN TYP MAX	UNIT
t _{IPH}	Input ready pulse HIGH	4 ensilov	5 12 12	ns
^t OPH	Output ready pulse HIGH	8 egyfloy I	5 12	ns
tORD	Ouput ready t to Data Valid	s of MMA = 5V spat	progrado Augor 18	ns

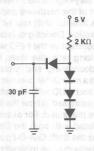
Standard Test Load



Input Pulse Amplitude = 3 V Input Rise and Fall Time (10%-90%) = 2.5 ns Measurements made at 1.5 V

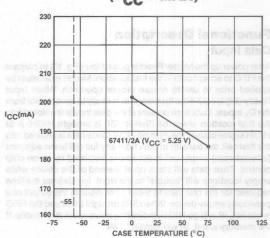
Test Load

Design Test Load (35 MHz)



I_{OL} R1 R2 24 mA 200 Ω 300 Ω 8 mA 600 Ω 1200 Ω

Typical I_{CC} vs Temperature $(V_{CC} + MAX)$





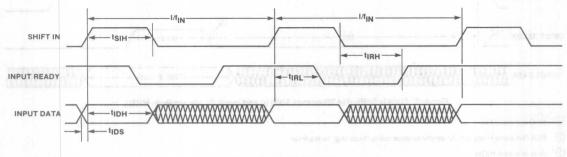


Figure 1. Input Timing

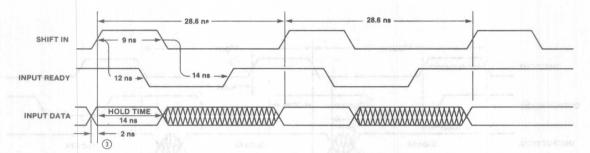


Figure 2. Typical Waveforms for 35 MHz Shift-In Data Rate

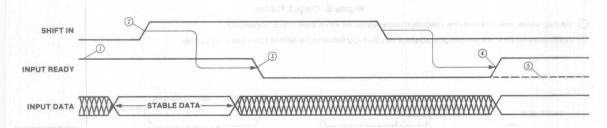


Figure 3. The Mechanism of Shifting Data into the FIFO

- (1) Input Fieady HIGH indicates space is available and a Shift-In pulse may be applied.
- (2) Input Data is loaded into the first word. The Data from the first word is released for "fall-through" to second word.
- (3) Input Ready goes LOW indicating the first word is full.
- (4) Shift-In going LOW allows Input Ready to sense the status of first word. The first word is now empty as indicated by Input Ready HIGH.
- 3 If the second word is already full then the data remains at the first word. Since the FIFO is now full Input Ready remains low. NOTE: Shift-In pulses applied while Input Ready is LOW will be ignored (See Figure 5).

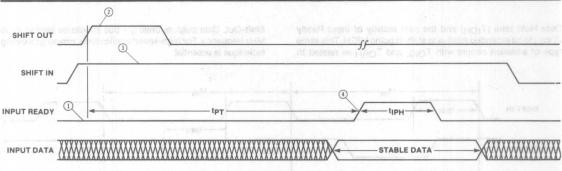


Figure 4. Data is Shifted in Whenever Shift In and Input Ready are Both HIGH

- 1 FIFO is initially full.
- ② Shift Out pulse is applied. An empty location starts "bubbling" to the front.
- 3 Shift In is held HIGH
- 4 As soon as Input Ready becomes HIGH the Input Data is loaded into the first word.

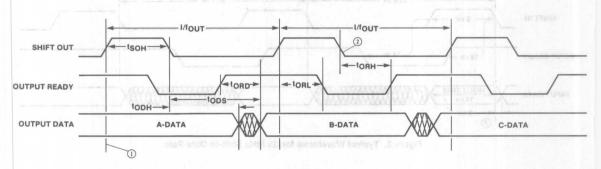


Figure 5. Output Timing

- 1 The diagram assumes that at this time, words 63, 62 and 61 are loaded with A, B and C Data, respectively.
- 2 Output data changes on the falling edge of SO after a valid Shift-Out Sequence, i.e. OR and SO are both high together.

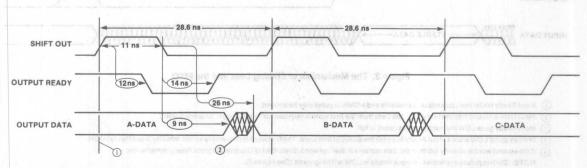


Figure 6. Typical Waveforms for 35 MHz Shift-Out Data Rate

- 1 The diagram assumes that at this time words 63, 62 and 61 are loaded with A, B and C Data, respectively.
- 2 Data in the first crosshatched region may be A or B Data.



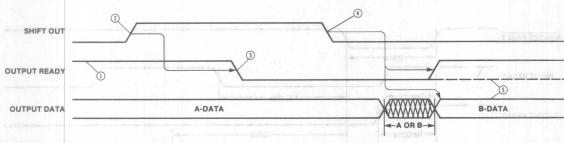


Figure 7. The Mechanism of Shifting Data Out of the FIFO

- 1) Output Ready HIGH indicates that data is available and a Shift-Out pulse may be applied.
- Shift-Out goes HIGH causing the contents of word 62 (B-Data) to be released for fall-through to word 63. Output data remains as valid A-Data while Shift-Out is HIGH.
- 3 Output Ready goes LOW.
- 4 Shift-out goes LOW causing Output Ready to go HIGH and new data (B) to appear at the data outputs.
- (5) If the FIFO has only one word loaded (A-Data) then Output Ready stays LOW and the output data becomes invalid.

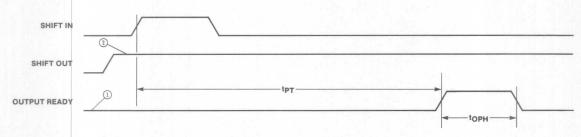


Figure 8. tpT and topH Specification

- 1 FIFO initially empty.
- (2) Shift Out held HIGH

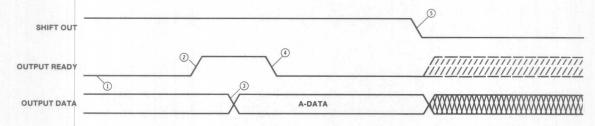
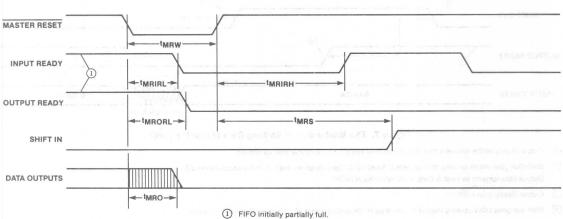
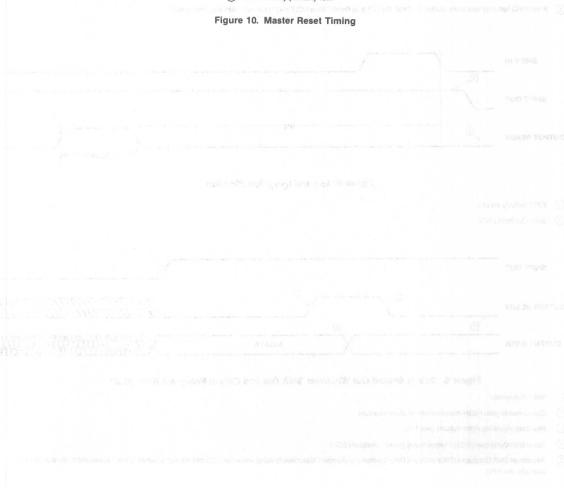


Figure 9. Data is Shifted Out Whenever Shift Out and Output Ready are Both HIGH.

- 1) Word 63 is empty.
- 2 Output Ready goes HIGH indicating arrival of the new data.
- 3 New data (A) arrives at the outputs (word 63).
- (4) Since Shift Out is held HIGH, Output Ready goes immediately LOW.
- (3) As soon as Shift Out goes LOW the Output Data is subject to change. Output Ready will go HIGH or LOW depending on whether there are any additional upstream words in the FIFO.





Features/Benefits

- · High-speed 28-MHz serial shift-in/shift-out rate
- 10-MHz parallel shift-in/shift-out rate
- . Three-state outputs with Hi-current drive
- · Cascadable at parallel port only
- · Half-full flag (32 or more)
- . Selectable 64x8 or 64x9 FIFO configuration thus providing "frame mark bit"

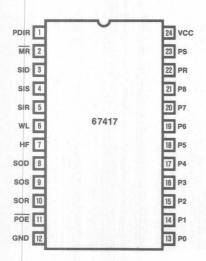
Typical Applications

- LAN equipment
- Data communication
- Office automation
- Microcomputers
- Minicomputers
- Disk/tape controllers

Description

The 67417 is a serializing/deserializing FIFO. This FIFO, the first one of its type in the industry, is organized 64 words x 8/9 bits wide. Like traditional Monolithic Memories' FIFOs it is cascadable, but only at the parallel port.

Pin Configuration



Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE	DESCRIPTION
67417	J	Com	64×8/9

In addition, the device has the ability to connect directly to a system bus. These features make it a complete "sub-system on a

The FIFO basically has three modes of operation;

- 1. Serial in to parallel out
- 2. Parallel in to serial out
- 3. Serial in to serial out (requires non-standard logic level on PDIR).

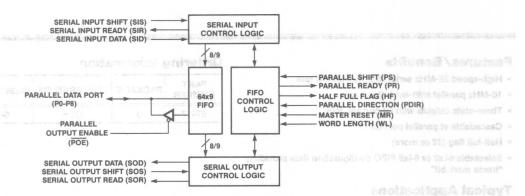
In the first mode, serial data can be accepted at up to 28 MHz and the FIFO outputs parallel data at up to 10 MHz. Similarly, in the alternate mode parallel data can be transformed into serial data. Please refer to appendix for detailed description.

Pin Names

P0-P8	Parallel Data
PS	Parallel Shift In/Out
PR	Parallel Input/Output Ready
POE	Parallel Output Enable
SID	Serial Input Data
SIS	Serial Input Shift
SIR	Serial Input Ready
SOD	Serial Output Data
sos	Serial Output Shift
SOR	Serial Output Ready
PDIR	Parallel Port Direction
WL	Word Length
MR	Master Reset
HF	Half Full Flag
VCC	VCC
GND	Ground



Block Diagram



LAN equipment

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ne 674.17 is a socializing/dependent of FTC. This REC, the histing of the ordinary, is one arrived 64 words x 4.9 oits industry, is one arrived 64 words x 4.9 oits industry historial Monovilla Niemo, as ERFOs it is use adate, but only at the penaltal port.

(FIFO) 64x8/9 Hemory

Pin Conflagation



Prince Victor Prince Pr

Absolute Maximum Ratings

Supply voltage V _{CC}	
Input voltage	
Off-state output voltage	-0.5 V to 5.5 V
Storage temperature	65° to +150° C

Operating Conditions

SYMBOL	PARAMETER	FIGURE	COMMERCIAL MIN TYP MAX	UNIT
Vcc	Voltage 6 0 8 Höfft ybraff	Serial Outpu	4.75 5.25	V
TA	Operating free-air temperature	-Full LOW	0 of 1 min2 funte 0 Island 75	°C
	SERIAL INPUT PARAMETERS	ARAS TUST	FARALLEL IMPUT/OIL	
fSIN	Max. Serial Shift-In Rate	V/O1 ybss	R lettered of Little College 28	MHz
tSISH	Serial Shift-In HIGH time	HOIN ybas	Parallel Shift to Para 22 p	ns
tSISL	Serial Shift-In LOW time	HINR II	Family Shift of H	ns
tSIDS	Serial Input Data Setup time	V/(1 .) (60)	He14 or I foO-min3 tellands	ns
tSIDH	Serial Input Data Hold time	BMARAS TI	PARALLEL OLO PA	ns
tSIRHS	Recovery Time Serial Input Ready † to Serial Input Shift †	Oupuj data	Minimum Parnilei Shift of to	ns
40	SERIAL OUTPUT PARAMETERS	to be seen a see	Polar and transaction and the	UUSY
fsout	Max. Serial Shift-Out Rate	1	28	MHz
tsosh	Serial Shift-Out HIGH time	3	15	ns
tsosl	Serial Shift-Out LOW time	3	15	ns
^t ORHS	Recovery time Serial Output Ready † to Serial Output Shift †	3 O H	Parelle: Output Ready (5)ie	ns
an d	WORD LENGTH PARAMETERS	WO.	Master Reset I to Data Out	ORM
tswL	Setup SIS, SOS	1,3	gnige Reset Lto Sen 81 np	ns
^t HWL	Hold SIS, SOS	1,3	and lates of the set in Serial Mp	ns
801 0	PARALLEL PORT PARAMETERS	14.0°T 4588	A SHARES OF LIGHT SHARES	PARME
fp u	Parallel shift-in/shift-out rate	8	THE STATE OF LOSS TO SHARE TO SHARE TO	MHz
t _{PSH}	Parallel Shift-In/Out HIGH time	5/8	30	ns
tPSL	Parallel Shift-In/Out LOW time	5/8	30	ns
tPIDS	Parallel Input Data Setup time	5	-5 PODE 12 POD	ns
^t PIDH	Parallel Input Data hold time	5	35	ns
tPDIRSL	Shift LOW to parallel direction transition	14	50	ns
t _{PDIRSH}	Parallel direction transition to Shift HIGH	14	50	ns
t _{PRHS}	Parallel Ready t to Parallel Shift Low	10/11	30	ns
an c	MASTER RESET PARAMETER	5-0	Curout uschis and Post to 1	234
^t MRW	Master Reset LOW time	12/13	40	ns

sprift I muminsk etulosdA

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	FIGURE	COMMERCIAL MIN TYP MA)	UNIT
D' - F-01	SERIAL INPUT PARAMETERS		ordin ag	the epino
tSIRL	Serial Input Shift † to Serial Input Ready LOW	2	23	3 ns
tSIHFH	Serial Input Shift 1 to Half-Full Flag HIGH	7	1.3	3 μs
	SERIAL OUTPUT PARAMETERS		ing Cor Jilloms	inteq.
tSORL	Serial Output Shift † to Serial Output Ready LOW	4	23	3 ns
tsop	Serial Output Shift † to Serial Output data	3	23	3 ns
todrh	Serial Output Data valid to Serial Output Ready HIGH	3	0 25 apatiov	ns
tSOHFL	Serial Output Shift † to Half-Full LOW	7 843	enegment is earl guitare QO 1.	3 μs
	PARALLEL INPUT/OUTPUT PARAMETERS	PARAMETER	TUSM MER	
t _{PSPRL}	Parallel Shift † to Parallel Ready LOW	5/8	Max Bertal Shife-In Plots	5 ns
^t PSPRH	Parallel Shift ↓ to Parallel Ready HIGH	5/8/10	8 Senet Shift-In Affording	ns
t _{PSHFH}	Parallel Shift-In↓to Half-Full HIGH	6	1 Satiat Snift-In LC 1 time	3 μs
^t PSHFL	Parallel Shift-Out ↓ to Half-Full LOW	9	1 Senal Input Cara Setup tem	3 μs
ap.	PARALLEL OUTPUT PARAMETERS		Serial logist Dates Lote time	HOIR
^t PODH	Minimum Parallel Shift ↓ to Ouput data	01 8 8	Recovery Time S and 20 or	ns
t _{POD}	Maximum Parallel Shift ↓ to Output data	8	61	0 ns
t _{PODV}	Minimum Output data valid to parallel ready HIGH	8	0 15	ns
and de	OTHER PARAMETERS			7006
t _{PT}	Fall-through time	10/11/16/17	2.0	6 μs
t _{IPH}	Parallel Input Ready pulse HIGH	11	30	ns
^t OPH	Parallel Output Ready pulse HIGH	10	30 program Colores of	ns
^t MRO	Master Reset ↓ to Data Out LOW	12	HTGMELGROW 6	5 ns
t _{MRSIRL}	Master Reset ↓ to Serial Input Ready LOW	12	208,818 cure 3 4	0 ns
^t MRSIRH	Master Reset † to Serial Input Ready HIGH	12	por promise 4	o ns
^t MRPRL	Master Reset I to Parallel Ready LOW	12/13	4	0 ns
^t MRPRH	Master Reset † to Parallel Ready HIGH	13	en nun studial en etima (stimas) 3	0 ns
t _{MRSORL}	Master Reset ↓ to Serial Output Ready LOW	13	HOUR monathing rathered. 4	o ns
^t MRHFL	Master Reset ↓ to Half-Full LOW	12/13	P INO 1 OLONG PRINCE DEPENDED 60	o ns
^t PDIROR	Parallel Direction change to new Output Ready	14	in mater stack formal tests and 60) ns
tPDIROD	Parallel Direction change to Output data valid	14	mit block used them in the 60	ns ns
t _{PDIRPZ}	Parallel Direction change to Parallel Output data Hi-Z	14	transit, to tenso or biO.1 meg. 30	5 ns
t _{PDIRSZ}	Parallel Direction changes to Serial Output-data Hi-Z	14	8 Paratlel direction recognice	ns ns
t _{PZX}	Output enable time POE to P0-8	15	tations of Labour Indiana 30	o ns
tPXZ	Output disable time POE to P0-8	15	3.	5 ns

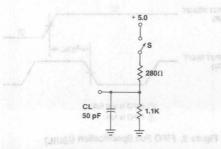
Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMET	TER		TEST CONDITIO	ONS		MIN TYP		UNIT
V _{IL}	Low-level input vo	ltage						0.8†	V
VIH	High-level input vo	oltage					2†		V
VIC	Input clamp voltag	ge	V _{CC} = MIN	I _I = -18 mA				-1.5	V
IIL	Low-level input cu	irrent	V _{CC} = MAX	V _I = 0.4 V		-0.4		mA	
IH	High-level input co	urrent	V _{CC} = MAX	V _I = 2.4 V				mA	
l _l	Maximum input co	urrent	V _{CC} = MAX	V _I = 5.5 V			0.4		mA
			V _{CC} = MIN	Data Outputs P0-P8, SOD	I _{OL} =24 mA	0-80°C		0.58	
Va	Low-level output voltage	25°C					0.55	V	
VOL		I _{OL} = 16 mA			0-80°C		0.5	7	
				All other outputs	I _{OL} =8 mA			0.5	
VOH	High-level output	voltage	V _{CC} = MIN	I _{OH} = -3 mA	and the second s		2.4		V
los	Output short-circ	uit current*	V _{CC} = MAX	V _O = 0 V		e company di	-20	-90	mA
ILZ	Off-state	SOD	V - MAY	V _O = 0.4 V			and the state of	-100	μΑ
I _{HZ}	output current*	P0 to P8	V _{CC} = MAX	V _O = 2.4 V		(85%)_	100	mA	
Icc	Supply current		V _{CC} = MAX	annina d	: A.	TI	O 19818 332.	350	mA
OV	PDIR non-standa over voltage	rd	Serial-In, Ser	ial-Out		See See	10	16	V

^{*} Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

Test Waveforms

TEST	S = OPEN	S = CLOSED	OUTPUT WAVEFORM-MEAS-LEVEL
All t _{PD}		All t _{PD}	V _{OH} 1.5 V
t _{PXZ}	^t PHZ	t _{PLZ}	V _{OH} 0.5 V 2.8 V V _{OL} 0.5 V 0.0 V
t _{PZX}	t _{PZH}	t _{PZL}	2.8 V VOH



[†] This is an absolute voltage with respect to device GND (pin 12) and includes all overshoots due to test equipment.

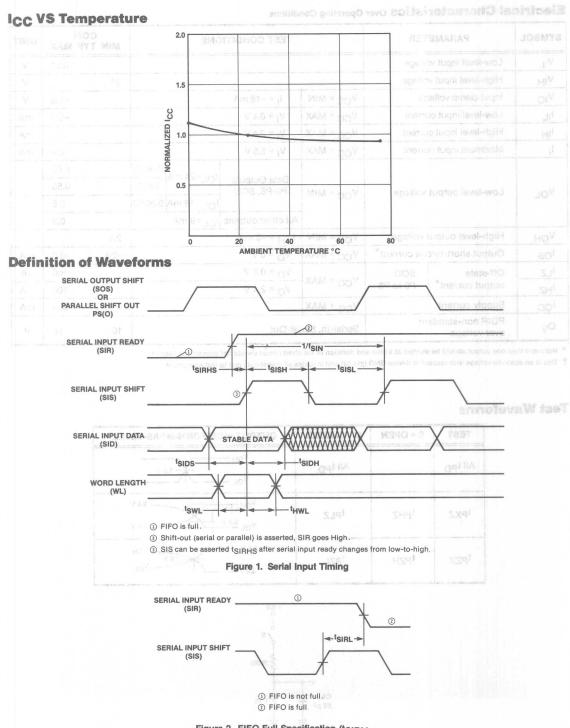
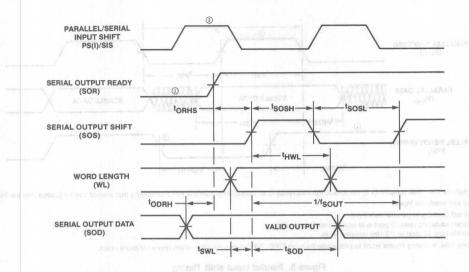


Figure 2. FIFO Full Specification (tSIRL)

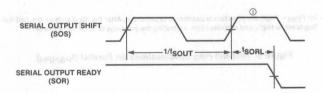
8

Definition of Waveforms (cont'd)



- ① FIFO is empty, output ready remains Low and shift-out cannot be applied.
- After a word is shifted in, output ready goes High and shift-out can be applied.
- 3 The first serial bit is P0.

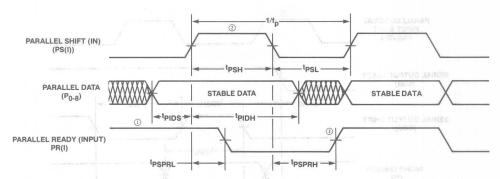
Figure 3. Serial Output Timing



① After the last shift-out, output ready goes Low indicating FIFO is empty.

Figure 4. FIFO Empty Specifications (tSORL)

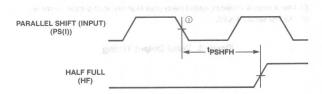
Definition of Waveforms (cont'd)



NOTE: PDIR = High for the mode parallel-in to serial-out. Parallel ready is an output flag from the FIFO indicating that a word can be loaded into the FIFO.

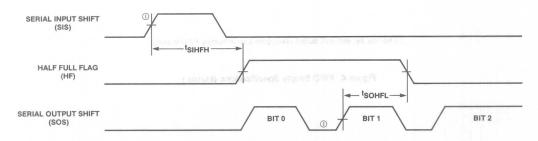
- ① FIFO is not full and ready for input.
- PS (In) is asserted, shifting in parallel data P0-8.
 PR (In) goes Low indicating parallel port is in use and no longer ready.
 PR (In) will remain Low as long as PS (In) remains High.
- ③ PS (In) has gone Low, allowing recent word to propagate through FIFO, PR (In) returns High when ready for more input.

Figure 5. Parallel Input Shift Timing



① for P_{DIR} = High, the direction is parallel-in to serial-out. After the 32nd shift-in, the half-full flag is set to High, and remains High, indicating the presence of 32 or more words.

Figure 6. Half-full Flag Specifications on Parallel (tpSHFH)

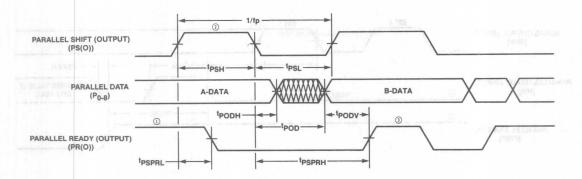


- ① When there are 31 words in the FIFO, the next shift-in on the 32nd word sets the half-full flag (HF) High indicating that there are 32 or more words.
- ② As soon as one word is partially shifted out, HF goes Low indicating there are less than 32 words.

Figure 7. Half-full Flag Specification on Serial Operation (tSIHFH, tSOHFL)

8

Definition of Waveforms (cont'd)

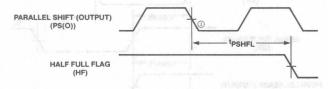


NOTE: For above conditions P_{DIR} = Low indicating that the direction is from serial-in to parallel-out.

Thus parallel ready indicates the output status.

- ① FIFO is not empty and at least one word is valid and ready at P0-8 outputs.
- ② PS (Out) is asserted, shifting out parallel data. Data remains valid, but:
- PR (Out) goes Low to indicate parallel port is in use and no longer ready.
- PR (Out) will remain Low as long as PS (Out) remains High.
- PS (Out) has gone Low, allowing data word to be shifted out. Next data word appears at output and
 PR (Out) is asserted to indicate valid data ready.

Figure 8. Serial-in to Parallel-out Specifications (tpop, tpopH, topy)



NOTE: For PDIR = Low the direction is serial-in to parallel-out.

 When a word is shifted out and the half-full flag goes Low, 31 words or less are in the FIFO.

Figure 9. Half-full Flag Specification on Parallel Shift-out (tpshfl)

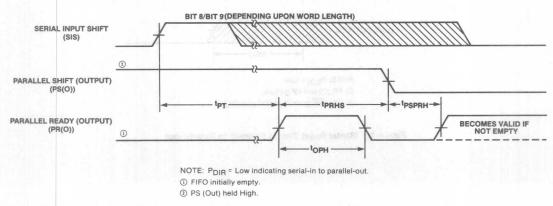
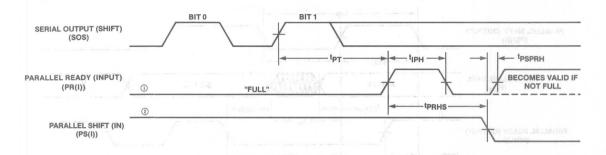


Figure 10. tpSPRH, tpT, tpOH Specifications (Serial Input Mode)

Definition of Waveforms (cont'd)



NOTE: P_{DIR} = High (parallel-in to serial-out).

- © FIFO is full, and the proceeding would a gradient difference or and of the
- ② PS (I) held High.

Figure 11. Fall-through Specifications

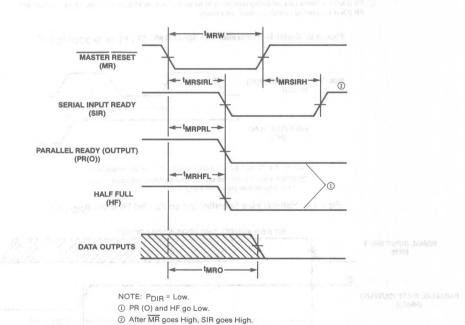


Figure 12. Master Reset Timing Serial-in to Parallel-out

8

Definition of Waveforms (cont'd)

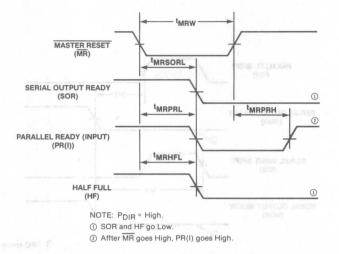
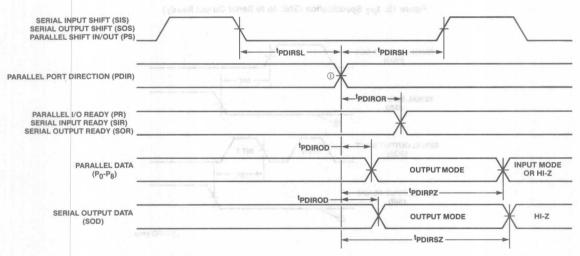


Figure 13. Master Reset Timing (Parallel-in to Serial-out)



NOTE: When the FIFO is used as a stack, change the port direction before the FIFO is full; otherwise, data may be lost.

Figure 14. PDIR Transition Parameters

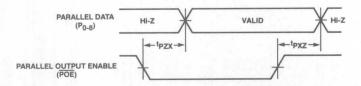


Figure 15. Parallel Port Enable and Disable Timing

Definition of Waveforms (cont'd)

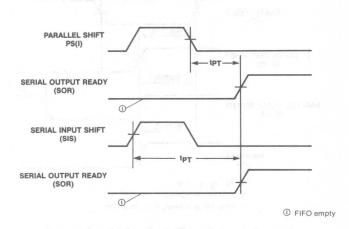


Figure 16. tpT Specification (Shift-in to Serial Output Ready)

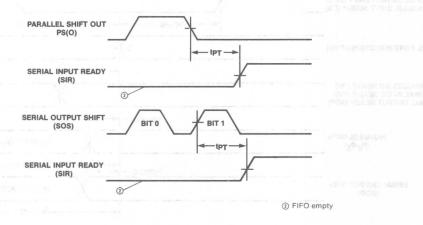


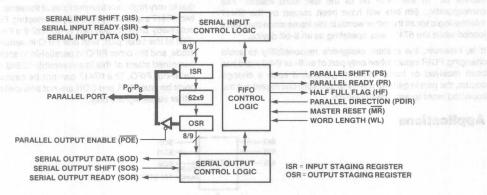
Figure 17. tpT Specification (Shift-in to Serial Input Ready)

Appendix Detailed Functional / Description for 67417

The 67417 is a serializing FIFO intended as a one-chip solution for data buffering and serializing/deserializing. It can be successfully used for interfacing parallel-format computing equipment to serial-format data communications and mass-memory equipment. The 67417 is a word-oriented device. It is meant to function with complete 8- or 9-bit words of data.

Parallel Port was a perferive ad the LW due

This is a fully bidirectional port, and it operates at a more conservative data rate of 10 MHz. The input-staging register (ISR) internally controls the parallel input data port bus signals. Likewise the OSR internally controls the parallel output data port. The ISR data outputs drive the parallel data inputs to the cell array, and the OSR inputs are likewise driven by the final parallel data stage of the cell array



Basically the major internal subsystems of the 67417 are:

- (i) The serial input port
- (ii) The serial output port
- (iii) The parallel port
- (iv) The FIFO control logic and
- (v) The cell array

Modes of Operation

There are three modes in which the 67417 can operate

(i) Parallel-in to serial-out

67401/2.

- (ii) Serial-in to parallel-out and
- (iii) Serial-in to serial-out.

In the parallel-in to serial-out mode, PDIR = HIGH. Thus Parallel Shift (PS) acts as a Shift In (SI) and similarly, Parallel Ready (PR) as Input Ready (IR). The first bit shifted out of the serial port will be bit 0 of the parallel word input.

disabled (during Master Reset) and PDIR = Low. The parallel

port is controlled by Parallel Shift (PS) input and Parallel Direc-

tion Input (PDIR). Parallel Ready (PR) is the handshake/status

output. At the Parallel Port PS and PR do accomplish a hand-

shake with the outside world as SI, IR, SO and OR on the

Similarly for serial-in to parallel-out mode, PDIR = LOW, and Parallel Shift (PS) acts as a Shift Out(SO) and Parallel Ready (PR) as Output Ready (OR). The first bit shifted into the serial port will be bit 0 of the parallel word output.

If the direction mode for a particular application of the 67417 is not intended to change during system operation, the PDIR input should be strapped to a logic LOW or HGH.

In the serial-in to serial-out mode, PDIR = 10 V minimum.

The parallel port does not function during this mode and is three-stated. The direction operating mode should not be changed if the FIFO is FULL otherwise stored data will be lost.

Cell Array

The 67417 cell array can function either as a 64x8 FIFO (with the 9th bit padded to a zero) or as a 64x9 FIFO, according to the setting of the word length (WL) control input. Like the PDIR

Serial Port

The two serial ports (input and output) are entirely separate which allows a high-speed data rate of 28 MHz. These serial ports do not share data pins, control pins, or internal circuits. However, since the serial output data is a three-state output, the serial data ports could be connected together in the normal serial-parallel operation mode with separate SOR and SIR status signals.

The serial input port interface consists of the Serial Input Ready (SIR) output, Serial Input Data (SID) input, and the Serial Input Shift (SIS) clock input. Unlike the analogous SI and IR signals on the 67401/2, SIS and SIR do not accomplish a "handshake" with the rest of the logic of the system which incorporates the 67417; rather SIR is asserted whenever the 67417 is still capable of receiving at least one more bit. SIS is a positive edge-triggered input which sequences the serial input control logic. This logic in turn controls SIR and the 8/9-bit Input Staging Register (ISR).

The serial output port interface is the dual of the above, with a Serial Output Data (SOD) output, a Serial Output Shift (SOS) clock input, and a Serial Output Ready (SOR) status output. SOR is asserted whenever at least one more bit is available at the output. SOS is a positive edge-triggered input which sequences the 8/9-bit Output Staging Register (OSR). Serial Output Data is automatically three-stated whenever the serial output port is

control input, WL can be switched at electronic speeds during system operations; but if the word length of a particular 67417 is never to change during system operation, WL for that part can be strapped to ground or $V_{\hbox{\scriptsize CC}}$.

It is a permissible 67417 mode of operation to almost fill the FIFO (there should be at least two empty locations) with WL set to 8-bit operation, then switch WL to 9-bit operation (WL = HIGH) to load one more word plus a frame marker in the last bit, and then switch PDIR and unload the 67417 in a 9-bit mode. This sequence of operations has the effect of providing a "frame marker bit" in the ninth bit of the last word loaded. The corresponding 9th bits will have been zeroed by the 67417 internal logic for all the other words in the frame since they were loaded while the 67417 was operating as an 8-bit device.

It is, however, the system designer's responsibility to avoid changing PDIR inputs when only part of an 8- or 9-bit word has been received or transmitted. In general, if such a change occurs, the part in general will try to add zero bits to pad out the impacted word to assume full length.

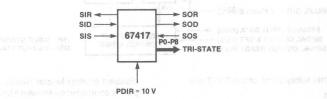
Half-Full Flag

This status output indicates when the 67417 statically contains 32 words or more. This provides an indication to send in more data if the device is operated in a mostly-empty mode or send out more data if the 67417 is operated in a mostly-full mode.

Cascading

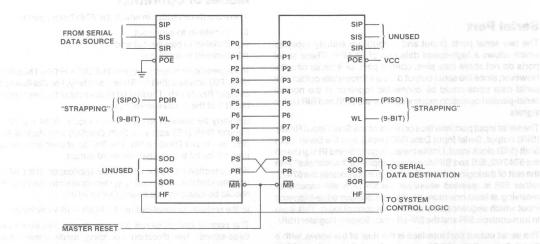
The 67417 is designed to be cascaded at the parallel port only, due to very high data transfer rates at the serial ports. Cascading two 67417's is accomplished by connecting Parallel Input/Output Ready (PR) of each part to control the Parallel Shift In/Out (PS) of the other part, with one FIFO in serial-in to parallel-out mode, and the other FIFO in parallel-in to serial-out mode. The combined effect of this is a reversible 128x8 or 128x9 serial-in serial-out FIFO. The 67417 can not be cascaded at the serial ports because SIR and SOR are not acknowledged signals but rather status signals only.

Applications



NOTE: It can shift in data serially in the multiples of 8- or 9-bit according to WL.

Figure 18. 512/576x1 Serial-in to Serial-out Mode



* SIPO = Serial-in to Parallel-out.

** PISO = Parallel-in to Serial-out.

Figure 19. Cascading of Two 'S417s for Serial-in to Serial-out states and page 18 to 10 hd -6/48 of Operation as a 128x9 (1152x1) FIFO and the serial states are the states of the serial states and the serial states are t

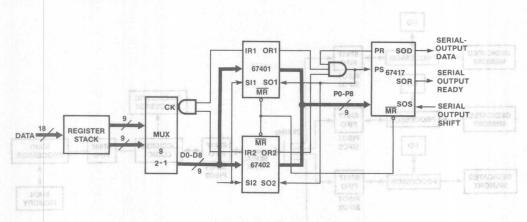


Figure 20. An Example of an Expansion Scheme for a 64x18 Parallel-to-Serial FIFO

An 18-bit data word is multiplexed into the two 67401/2 FIFOs. Since the 67417 FIFO is cascadable at the parallel port only, two

67401/2 FIFOs were used along with the 67417 to obtain the appropriate organization.

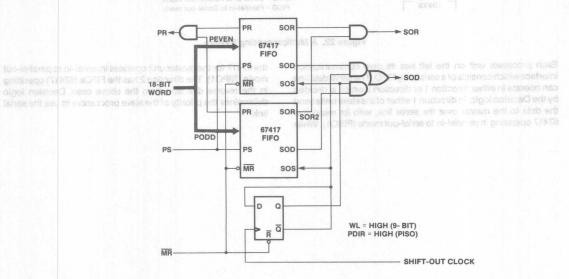


Figure 21. Another Example of an Expansion Scheme for a 64x18 Parallel-in to Serial-out FIFO Two 67417 FIFOs Are Used to Implement a 64x18 Parallel-in to Serial-out FIFO

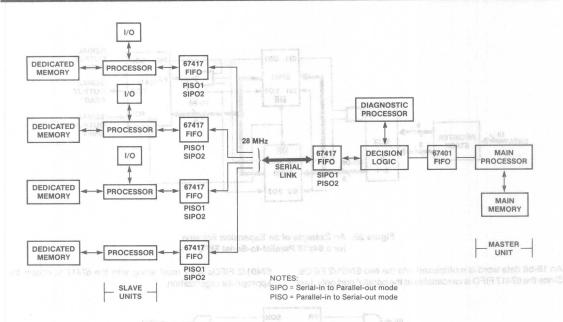


Figure 22. A Multiprocessing System

Each processor unit on the left has its own communication interface which consists of a serializing FIFO. The serial data link can operate in either direction 1 or direction 2 which is decided by the Decision logic. In direction 1 either of the slave units send the data to the master over the serial link, with its respective 67417 operating in parallel-in to serial-out mode (PISO1). While

the 67417 for the master unit operates in serial-in to parallel-out mode (SIPO1). The direction 2 has the FIFOs (67417) operating in the reverse direction from the above case. Decision logic determines the priority of the slave processors to use the serial link.

Figure 21: Another Example of un Especialm Schema for a 64s16 Paradicky to 54 (a) out PIPO. Two 67417 PIPOs Are Used to regions in a 64x16 Paradickie to 54 (a) out PIPO.

Features/Benefits

- High-speed 15 MHz shift-in/shift-out rates
- · High drive capability
- Low-power consumption
- Three-state outputs
- · Fully expandable by word width and depth
- · Half-Full and Almost-Full/Empty status flags
- Structured pinouts. Output pins directly opposite corresponding input pins.
- Asynchronous operation
- TTL-compatible inputs and outputs

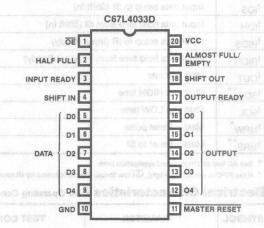
Description

The C67L4033D is a high-speed, 64x5 First-In-First-Out (FIFO) memory which operates at 15 MHz input/output rates. The data is loaded and emptied on a first-in-first-out basis. It is a three-state device with high-drive (I_{OL} = 24 mA) data outputs. These devices can be expanded to any word width and depth. It has a Half-Full flag (thirty-two or more words full) and an almost full/empty flag (fifty-six or more words or eight or less words). The main application of C67L4033D is as a rate buffer; sourcing and absorbing data at different rates. Other applications are high-speed tape and disk controllers, data communications systems and plotter control systems.

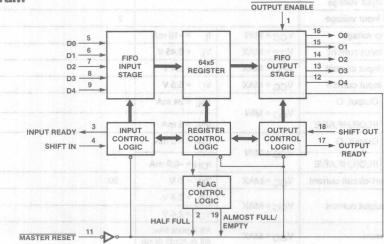
Ordering Information

PART NUMBER	PKG	TEMP	DESCRIPTION
C67L4033D	N,J	Com	15 MHz in/out

Pin Configuration



Block Diagram



TWX: 910-338-2376

Monolithic Memories 8

Absolute Maximum Ratings

	The state of the s
Supply voltage V _{CC}	0.5 V to 7 V
Input voltage	
Off-state output voltage	-0.5 V to 5.5 V
Storage temperature	

Operating Conditions Over Temperature Range

SYMBOL	PARA	METER	FIGURE	MIN	COMMERCIAL MAX	UNIT
V _{CC}	Supply voltage	HBGMUA		4.75	5 5.25	V
TA	Operating free-air temp	erature G8804 J160		0	nobembanos 70°0	°C
fIN	Shift In rate		1	15		
t _{SIH} *	Shift in HIGH time	·	1	24	TO THE WINDS OF STREET	ns
tSIL*	Shift in LOW time	Pin Configurat	1	15	ania funtuti atungsia ben	ns
t _{IDS}	Input data setup to SI (S	Shift In)	1	0	posiding logal pins.	ns
^t IDH	Input data hold time from SI (Shift In)		1	26	nothredb armon	ns
t _{RIDS}	Input data setup to IR (Input Ready)		4	0	Ingluo iste ziugni etdilagina	ns
t _{RIDH}	Input data hold time from IR (Input Ready)		4	26		ns
four -	Shift Out rate	TO YOUR TURNS	5		15	MHz
tson**	Shift Out HIGH time	CT au raise	(CAI75100-18	17 Haring	L4032D is a high-speed, 84x	ns
tsol	Shift Out LOW time	Film	5	15	it-rii-taiil s no baagma bns l	ns
tMRW*	Master Reset pulse	Section 1	sest 10studie	35 (Am	ice with nigh-drive (IOL = ?	ns
tMRS**	Master Reset to SI	Pulsa de la comp	10	35	an the experided to any work flag (thirty-five or more w	ns

^{*} See AC test and high-speed application note.

Electrical Characteristics Over Operating Conditions a another number of the season of

SYMBOL	PA	RAMETER	TEST C	CONDITION	COMMERCIAL	MAX	UNIT
V _{IL} *	Low-level	input voltage	KHA TURTUM		1000	0.8	V
VIH*	High-level	input voltage	1		2		V
VIC	Input clam	p voltage	V _{CC} = MIN	I _I = -18 mA	0	-1.5	V
IIL	Low-level	input current	V _{CC} = MAX	V _I = 0.45 V	1000	-250	μΑ
IIH	High-level	input current	V _{CC} = MAX	V _I = 2.4 V	14VB 40	50	μΑ
II	Maximum	input current	V _{CC} = MAX	V _I = 5.5 V	6	. 1	mA
\/ -	Low-level output voltage	Output, O	V _{CC} = MIN	I _{OL} = 24 mA	A	0.5	V
VOL		IR,OR,HF,AF/E		IOL = 8 mA	American Company of the Company of t	0.5	
VOH	High-level	Output, O	V _{CC} = MIN	I _{OH} = - 3 mA	2.4 TIME		V
	output voltage	IR,OR,HF,AF/E		I _{OH} = -0.9 mA			
los**	Output she	ort-circuit current	V _C C = MAX	VO = 0 V	-20	-90	mA
lozL	Off state of	tat arrant	VNAV	V _O = 0.4 V		-50	
lozh	On-state o	output current	VCC = MAX	V _O = 2.4 V		50	μΑ
Icc	Supply cui	rrent	V _{CC} = MAX	All inputs low. All outputs open.		120	mA

^{*} These are absolute voltages with respect to GND (Pin 10) and include all overshoots due to system and/or tester noise.

^{**} If the FIFO is not full (IR High), MR low forces IR low, followed by IR returning high when MR goes high.

^{**} Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	FIGURE	COMMERCIAL MIN M	AX	UNIT
t _{IRL} non	Shift In 1 to Input Ready LOW - 20 He Am 8	1	Part of the second seco	40	ns
t _{IRH}	Shift In ↓ to Input Ready HIGH	1	191-\$	26	ns
tORL	Shift Out 1 to Output Ready LOW	5	on that @ Tuell	45	ns
^t ORH	Shift Out ↓ to Output Ready HIGH	5	30.00 × 55	50	ns
todh	Output Data Hold (previous word)	5	12		ns
tods	Output Data Shift (next word)	5		40	ns
t _{PT}	Data throughput	4,8	16	600	ns
^t MRORL	Master Reset ↓ to Output Ready LOW	10	V E = shulkton/ oslu? to	60	ns
tMRIRH*	Master Reset ↑ to Input Ready HIGH	10	V 8.1 de epant a mellus	30	ns
tMRIRL*	Master Reset ↓ to Input Ready LOW	10	acquar so arey'r er asbniú	50	ns
^t MRO	Master Reset ↓ to Outputs LOW	10		60	ns
^t IPH	Input ready pulse HIGH	4	17		ns
^t OPH	Output ready pulse HIGH	8	24	na l	ns
tORD	Output ready † to Data Valid	5		-3	ns
t _{AEH} *	Shift Out 1 to AF/E HIGH	of rollings	I wol treature at fearer? retains only 3	320	ns
tAEL*	Shift in 1 to AF/E LOW	- neter 11 .noi3	soci tetil etti ni steb tosoos di O72	100	ns
tAFL*	Shift Out 1 to AF/E LOW	12	poisson and edition of the life of the 14	100	ns
t _{AFH} *	Shift In 1 to AF/E HIGH	12	matter imputs. Cass then precent a	320	ns
tHFH*	Shift In 1 to HF HIGH	13	to of Pterit seems tanger HE1-118 A	300	ns
tHFL*	Shift Out 1 to HF LOW and to make on the basis	13	to the third cell, the franchist of day	300	ns
t _{PHZ} *	Output Disable Delay	erti ta qui Ao	ar lies gapine (mevas two) mass ar lies at la durit doutnos en o-num	30	Marketa
tPLZ *	d per unor mana della anti ast retita ango los soo di telo		no iliw anotheori ytami eli ini) esh	30	ns
t _{PZL} *	Output Fooklo Dolovi serili evinosite i nor of euro seriorio	of hAlunent	to supplied orthograms on a recent	30	200
tPZH *	Output Enable Delay	Juli ton a O	kil adi bna WOLI tilguon La nasitV	40	ns

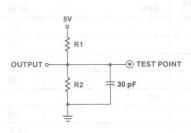
^{*} See timing diagram for explanation of parameters.

See table on following page for Resistor values

Three-State Test Load -tPZL S1 AND S2 CLOSED S1 CLOSED S2 OPEN WAVEFORM 1 1.5 V VOL +0.5 V TEST POINT want to o tPZH-VOH V_{OH} 1.5 V S1 OPEN S2 CLOSED S1 AND CL= V_T = 1.5 V S2 CLOSED ₹ R2 5 pF Figure A. Enable and Disable Waveform 1 is for a data output with internal conditions such that the output is 9 S2 low except when disabled by the output control. Waveform 2 is for a data output with internal conditions such that the output

Monolithic IIII Memories

is high except when disabled by the output control.



Input Pulse Amplitude = 3 V Input Rise and Fall Time (10%-90%) = 2.5 ns Measurements made at 1.5 V All Diodes are 1N916 or 1N3064

loL	R1	R2
24 mA (Data)	200 Ω	300 Ω
8 mA (IR, OR, Flags)	600 Ω	1200 Ω

Functional Description Data Input

After power up the Master Reset is pulsed low (Figure 10) to prepare the FIFO to accept data in the first location. Master Reset must be applied prior to use to ensure proper operation. When Input Ready (IR) is HIGH the first location is ready to accept data from the Dx inputs. Data then present at the the data inputs is entered into the first location when the Shift-In (SI) is brought HIGH. A SI HIGH signal causes the IR to go LOW. Once data is entered into the first cell, the transfer of data in any full cell to the adjacent (downstream) empty cell is automatically activated by an on-chip control. Thus data will stack up at the end of the device (while empty locations will "bubble" to the front when data is shifted out). tpt defines the time required for the first data to travel from input to the output of a previously empty device. When SI is brought LOW and the FIFO is not full, IR will go HIGH, indicating more room is available. If the memory is full, IR will remain LOW. The FIFO should always be cleared by using Master Reset before starting the operation.

Data Output

Data is read from the O_X outputs. When data is shifted to the output stage, Output Ready (OR) goes HIGH, indicating the presence of valid data. When the OR is HIGH, data may be shifted out by bringing the Shift Out (SO) HIGH. A HIGH signal at SO causes the OR to go LOW. Valid data is maintained while the SO is HIGH. When SO is brought LOW the upstream data, provided that there is valid upstream data, is shifted to the output stage. When new valid data is shifted to the output stage, OR goes HIGH. If the FIFO is emptied, OR stays LOW and Data output will not be valid.

Input Ready and Output Ready may also be used as status signals indicating that the FIFO is completely full (Input Ready stays LOW for at least tp_T) or completely empty (Output Ready stays LOW for at least tp_T).

AC Test and High-Speed App. Notes

Since the FIFO is a very-high-speed device, care must be exercised in the design of the hardware and the timing utilized within the design. The internal shift rate of the FIFO typically exceeds 20 MHz in operation. Device grounding and decoupling is crucial to correct operation as the FIFO will respond to very small glitches due to long reflective lines, high capacitances and/or poor supply decoupling and grounding. Monolithic Memories recommends a monolithic ceramic capacitor of 0.1 µF directly between VCC and GND with very short lead length. In addition, care must be exercised in how the timing is set up and how the parameters are measured. For example, since an AND gate function is associated with both the Shift-In-Input Ready combination, as well as the Shift-Out-Output Ready combination, timing measurements may be misleading, i.e., rising edge of the Shift-In pulse is not recognized until Input ready is HIGH. If Input Ready is not high due to (a) too high a frequency, or (b) FIFO being full or effected by Master Reset, the Shift-In activity will be ignored. This will affect the device from a functional standpoint, and will also cause the "effective" timing of Input Data Hold time (TIDH) and the next activity of Input Ready (TIRL) to be extended relative to Shift-in going HIGH. This same type of problem is also related to TIRH, TORL and TORH as related to Shift-Out. For high-speed applications, proper grounding technique is essential.

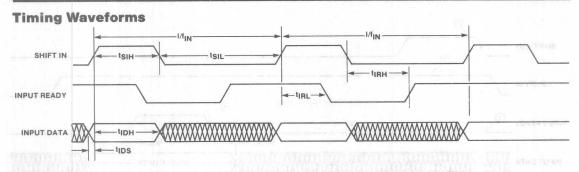


Figure 1. Input Timing

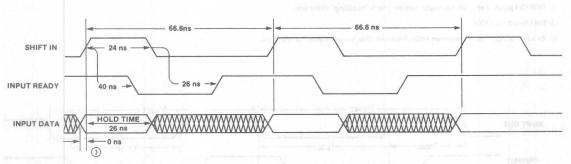


Figure 2. Typical Waveforms for 15 MHz Shift-In Data Rate

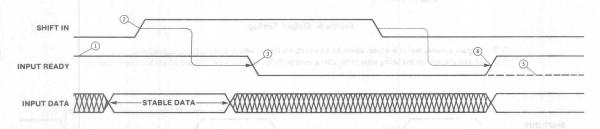


Figure 3. The Mechanism of Shifting Data into the FIFO

- ① Input Ready HIGH indicates space is available and a Shift-In pulse may be applied.
- ② Input Data is loaded into the first word. The data from the first word is released for "fall-through" to second word.
- 3 Input Ready goes LOW indicating the first word is full.
- Shift-In going LOW allows Input Ready to sense the status of first word. The first word is now empty as indicated by Input Ready HI.H.
- (3) If the second word is already full then data remains at the first word. Since the FIFO is now full Input Ready remains low.
 Note: Shift-In pulses applied while Input Ready is LOW will be ignored (See Figure 5).

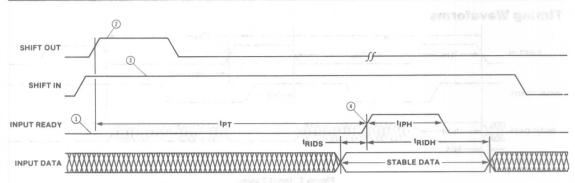


Figure 4. Data is Shifted in Whenever Shift In and Input Ready are Both HIGH

- ① FIFO is initially full.
- ② Shift Out pulse is applied. An empty location starts "bubbling" to the front.
- 3 Shift In is held HIGH.
- (4) As soon as Input Ready becomes HIGH the Input Data is loaded into the first word.

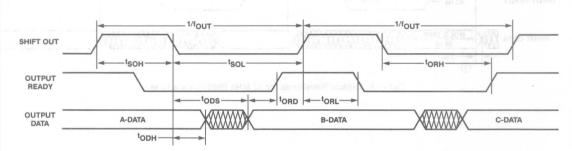


Figure 5. Output Timing

- ① The diagram assumes that at this time, words 64, 63 and 62 are loaded with A, B and C Data, respectively.
- 3 Output data changes on the falling edge of SO after a valid Shift-Out Sequence, i.e., OR and SO are both high together.

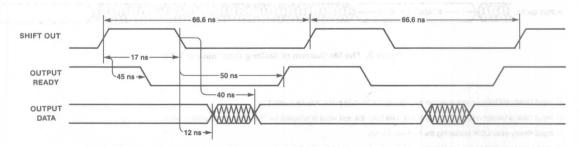


Figure 6. Typical Waveforms for 15 MHz Shift-Out Data Rate

- ① The diagram assumes that at this time words 64, 63 and 62 are loaded with A, B and C Data, respectively.
- ② Data in the first crosshatched region may be A or B Data.

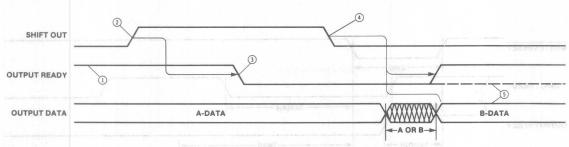


Figure 7. The Mechanism of Shifting Data Out of the FIFO

- ① Output Ready HIGH indicates that data is available and a Shift-Out pulse may be applied.
- ③ Shift-Out goes HIGH causing the contents of word 63 (B-Data) to be released for fall-through to word 64. Output data remains as valid A-Data while Shift-Out is HIGH.
- 3 Output Ready goes LOW.
- Shift-out goes LOW causing Output Ready to go HIGH and new data (B) to appear at the data outputs.
- 3 If the FIFO has only one word loaded (A-Data) then Output Ready stays LOW and the output data becomes invalid.

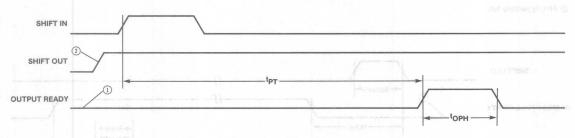


Figure 8. tpT and topH Specification

- ① FIFO initially empty.
- ② Shift-Out is held HIGH.

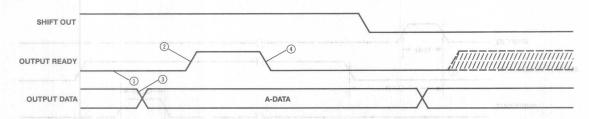


Figure 9. Data is Shifted Out Whenever Shift Out and Output Ready are Both HIGH

- ① Word 64 is empty.
- ② Output Ready goes HIGH indicating arrival of the new data.
- 3 New data (A) arrives at the outputs (word 64).
- Since Shift Out is held HIGH, Output Ready goes immediately LOW.
- (§) As soon as Shift Out goes LOW the Output Data is subject to change. Output Ready will go HIGH or LOW depending on whether there are any additional upstream words in the FIFO.

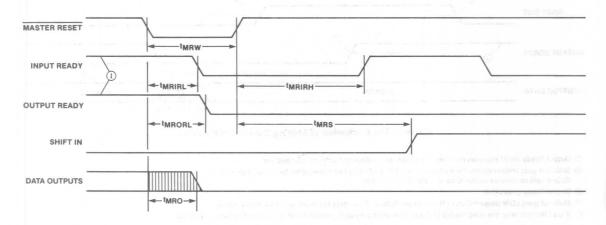


Figure 10. Master Reset Timing

① FIFO is partially full.

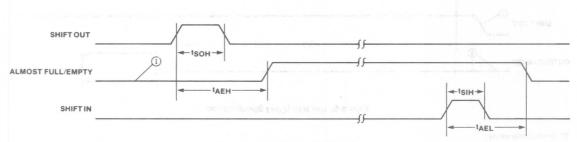


Figure 11. tAEH, tAEL Specifications

① FIFO contains 9 words (one more than almost empty).

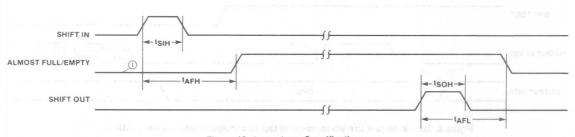


Figure 12. tafh, tafL Specifications

① FIFO contains 55 words (one short of almost full).



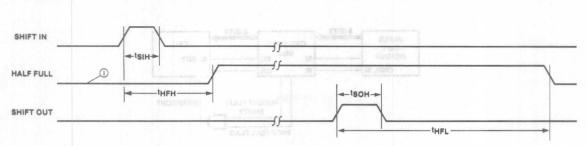
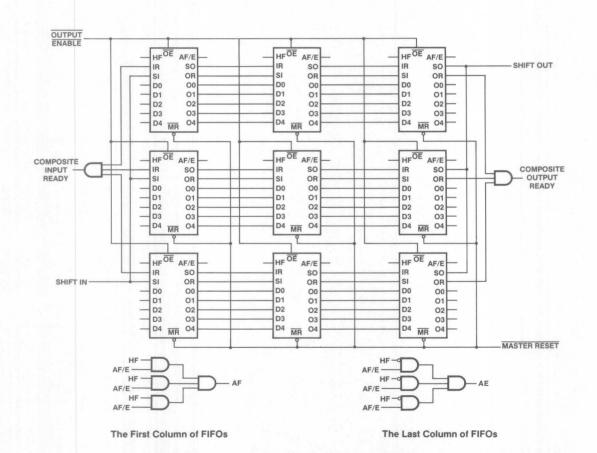


Figure 13. t_{HFL}, t_{HFH} Specifications

① FIFO contains 31 words (one short of half full).



Almost Full (AF) is eight words or less to FIFO full.

Almost Empty (AE) is eight words or less to FIFO empty

Figure 14. 192x15 FIFO with C67L4033D

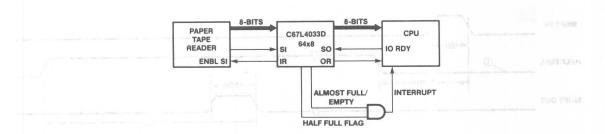
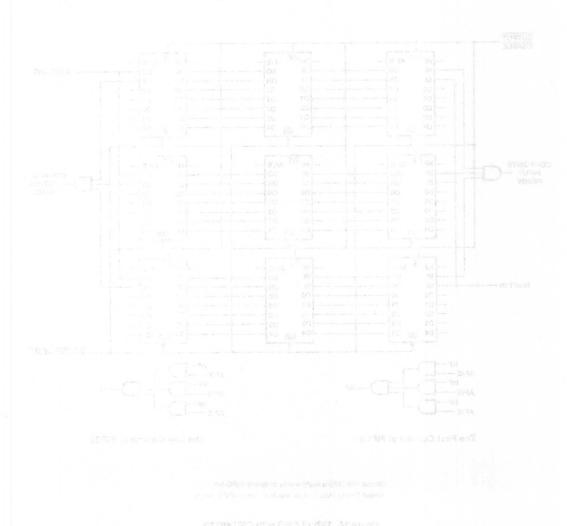


Figure 15. Application for C67L4033D "Slow and Steady Rate to Fast Blocked Rate"

Note: Cascading the FIFO's in word width is done by ANDing the IR and OR as shown in Figure 14.



First-In First-Out (FIFO) 64x4 Memory 15 MHz (Cascadable) **With Three-State Outputs**

C67L4013D

annited municall stuiceds

O/P

3-state

DESCRIPTION

15 MHz 64x4 FIFO

Ordering Information PART PKG TEMP

N, J

Com

NUMBER

C67L4013D

- High-speed 15-MHz shift-in/shift-out rates Low power consumption
- TTL inputs and outputs

Features/Benefits

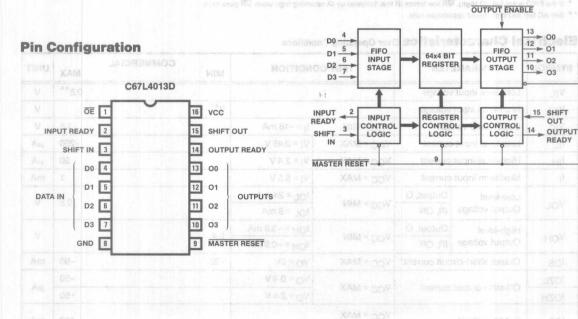
- · Readily expandable in word width and depth
- Structured pinouts, Output pins directly opposite corresponding input pins
- · High-drive capability
- Asynchronous operation
- Output Enable feature

Block Diagram

C67L4013D

Description

The C67L4013D is a "fall-through" high-speed First-In First-Out (FIFO) memory organized 64 words by 4 bits. The FIFO is expandable in word width and depth. The FIFO is attractive for many applications such as disk controllers, communication buffers, rate buffers, etc. The C67L4013D has three-state, highdrive (IOI = 24 mA) outputs.



SHIFT

OUT

OUTPUT

Absolute Maximum Ratings

Supply voltage V _{CC}	0.5 V to 7 V
Input voltage	
Off-state output voltage	0.5 V to 5.5 V
Storage temperature	

Operating Conditions Over Temperature Range

SYMBOL	PARAMETER	FIGURE	MIN TYP MAX	UNIT
Vcc	Supply voltage		4.75 5 5.25	V
TA	Operating free-air temperature		Open has a blue been at sublinear 70	°C .
fIN	Shift in rate	1 (4)	seque vironio reletatado espesa	MHz
tSIH	Shift in High time	1	24 stag tag it grabacy.	ns
tSIL	Shift in Low time	1	15	ns
tIDS	Input data setup to SI (Shift In)	1	0	ns
tIDH	Input data hold time to SI (Shift In)	1	26	ns
t _{RIDS}	Input data setup to IR (Input Ready)	4	0	ns
t _{RIDH}	Input data hold time to IR (Input Ready)	4	26	ns
four	Shift out rate	5	15	MHz
tsoH	Shift out High time	10 - 15 P nt-	L4013Disc "fall-timough" run-space 7nd	ns
tSOL	Shift out Low time	8 5 5	151 P vo - row tô basinagao yiomen	ns
tMRW	Master Reset pulse**	10	35 state them as disk controlled	ns
tMRS	Master Reset to SI*	10	ate buffers, etc. The C67C4013D has 35°	ns

^{*} If the FIFO is not full (IR High), $\overline{\text{MR}}$ low forces IR low, followed by IR returning high when $\overline{\text{MR}}$ goes high.

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMI	PARAMETER		TEST CONDITION		COMMERCIAL	MAX	UNIT
VIL	Low-level input	voltage	and the state of t			THE HOLD IN	0.8**	V
VIH	High-level input	voltage	TOTAL PORTS		2**	1115	5	V
ViC	Input clamp vol	tage	VCC = MIN	I _I = -18 mA	irena III	l'st v	-1.5	V
TIL	Low-level input	current	VCC = MAX	V _I = 0.45 V	Court 181		-250	μΑ
ΊΗ	High-level input	current	V _C C = MAX	V _I = 2.4 V	Accept provide	formal fo	50	μΑ
II	Maximum input	current	V _{CC} = MAX	V _I = 5.5 V	Parcel	ord ora	1	mA
V	Low-level	Output, O	V NAINI	I _{OL} = 24 mA	Acres (San A		V
VOL	Output voltage	IR, OR	VCC = MIN	IOL = 8 mA	so [fi]		0.5	V
V/0	High-level	Output, O	Voo - MINI	I _{OH} = -3.0 mA	2.4	1 E	0 }	V
VOH	Output voltage	IR, OR	VCC = MIN	I _{OH} = -0.9 mA	2.4			V
los	Output short-cir	cuit current*	V _{CC} = MAX	VO = 0V	-20	The second second second	-90	mA
IOZL	Off-state output current		VNAAY	V _O = 0.4 V			-50	
lozh			VCC = MAX	V _O = 2.4 V			+50	μΑ
ICC	Supply current V _{CC} = MAX All inputs low. All o		outputs open.			110	mA	

^{*} Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

** These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise.

^{**} See AC test and high-speed application note.

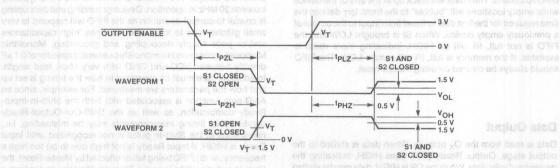
Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	FIGURE	COMMERCIAL MAX	UNIT	
tIRL† a od	Shift In 1 to Input Ready LOW		40	ns	
tIRH†	Shift In ↓ to Input Ready HIGH		197 \$ 26	ns	
tORL†	Shift Out † to Output Ready LOW	. 73	104 TEST (0-1-1-1-1-1-1-1-1-1-1-1-1-1-1-1-1-1-1-1	ns	
tORH†	Shift Out ↓ to Output Ready HIGH	5	14 06 75 SR \$ 50	ns	
tODH†	Output Data Hold (previous word)	7 5	12	ns	
tods	Output Data Shift (next word)		40	ns	
tpT	Data throughput	4,8	1600	ns	
†MRORL	Master Reset ↓ to Output Ready LOW		V S = abudilomA - Muq 60	ns	
†MRIRH	Master Reset ↑ to Input Ready HIGH*		In 061 Rise and Fall Time (10%-60%) = 2 6		
^t MRIRL	Master Reset ↓ to Input Ready LOW*	10	V C.1 18 Obert 211 (1911) 50	ns	
^t MRO	Master Reset ↓ to Outputs LOW		60	ns	
tIPH	Input ready pulse HIGH	4	17	ns	
tOPH	Output ready pulse HIGH	8	24	ns	
tORD	Output ready † to Data Valid	5	-3	ns	
tPHZ	Output Disable Delay CC71 4012D		30	no	
tPLZ	Output Disable Delay, C67L4013D		30	ns	
tpZL	Output Facilia Dalay, C67I 4012D	- A	30	lonu!	
tPZH	Output Enable Delay, C67L4013D		40	ns	

Note: Typicals at 5V VCC and 25°C TA.

* If the FIFO is not full (IR High), MR low forces IR low, followed by IR returning high when MR goes high.

* See AC test and high-speed application note.

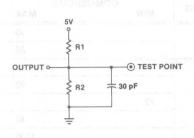


HOIH price of the of sydular bat notice and or Figure A. Enable and Disable and Request WO. Interior of OS narry, HOIH at

Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

Waveform 2 is for an output with internal conditions such that the output is high as HO possible at OHH safety HEIH except when disabled by the output control.

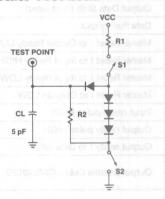
Standard Test Load



Input Pulse Amplitude = 3 V Input Rise and Fall Time (10%-90%) = 2.5 ns Measurements made at 1.5 V All Diodes are 1N916 or 1N3064

loL	R1	R2
24 mA	200 Ω	300 Ω
8 mA	600 Ω	1200 Ω

Three-State Test Load



Functional Description

Data Input

After power up the Master Reset is pulsed low (Figure 10) to prepare the FIFO to accept data in the first location. Master reset must be applied prior to use to ensure proper operation. When Input Ready (IR) is HIGH the first location is ready to accept data from the D_X inputs. Data then present at the data inputs is entered into the first location when the Shift-In (SI) is brought HIGH. An SI HIGH signal causes the IR to go LOW. Once data is entered into the first cell, the transfer of data from any full cell to the adjacent (downstream) empty cell is automatic, activated by an on-chip control. Thus data will stack up at the end of the device while empty locations will "bubble" to the front. tpT defines the time required for the first data to travel from input to the output of a previously empty device. When SI is brought LOW and the FIFO is not full, IR will go HIGH, indicating more room is available. If the memory is full, IR will remain LOW. The FIFO should always be cleared by using master reset.

Data Output

Data is read from the O_X outputs. When data is shifted to the output stage, Output Ready (OR) goes HIGH, indicating the presence of valid data. When the OR is HIGH, data may be shifted out by bringing the Shift Out (SO) HIGH. A HIGH signal at SO causes the OR to go LOW. Valid data is maintained while the SO is HIGH. When SO is brought LOW the upstream data, provided the upstream stage has valid data, is shifted to the output stage. When new valid data is shifted to the output stage, OR goes HIGH. If the FIFO is emptied, OR stays LOW and Data output will not be valid.

Input Ready and Output Ready may also be used as status signals indicating that the FIFO is completely full (Input Ready stays LOW for at least tp_T) or completely empty (Output Ready stays LOW for at least tp_T).

AC Test and High-Speed App. Notes

Since the FIFO is a very-high-speed device, care must be exercised in the design of the hardware and the timing utilized within the design. The internal shift rate of the FIFO typically exceeds 20 MHz in operation. Device grounding and decoupling is crucial to correct operation as the FIFO will respond to very small glitches due to long reflective lines, high capacitances and/or poor supply decoupling and grounding. Monolithic Memories recommends a monolithic ceramic capacitor of 0.1 μF directly between VCC and GND with very short lead length. In addition, care must be exercised in how the timing is set up and how the parameters are measured. For example, since an AND gate function is associated with both the Shift-In-Input-Ready combination, as well as the Shift-Out-Output-Ready combination, timing measurements may be misleading, i.e., rising edge of the Shift-In pulse is not recognized until Input Ready is HIGH. If Input Ready is not high due to (a) too high a frequency, or (b) FIFO being full or effected by Master Reset, the Shift-In activity will be ignored. This will affect the device from a functional standpoint, and will also cause the "effective" timing of Input Data Hold time (TIDH) and the next activity of Input Ready (TIRL) to be extended relative to shift-in going HIGH. This same type of situation occurs with TORL and TORH as related to Shift-Out. For high-speed applications, proper grounding technique is essential.

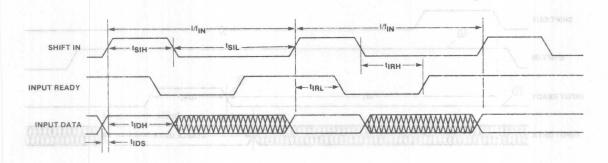


Figure 1. Input Timing

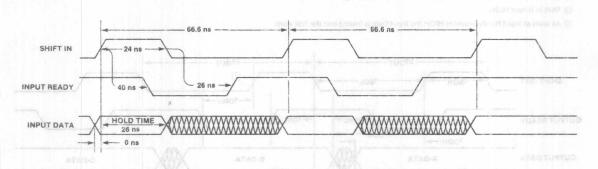


Figure 2. Typical Waveforms for 15 MHz Shift-In Rate

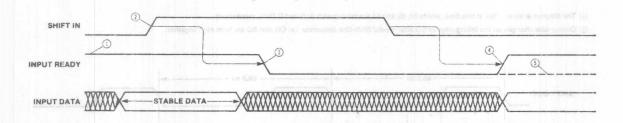


Figure 3. The Mechanism of Shifting Data into the FIFO

- ① Input Ready HIGH indicates space is avialable and a Shift-In pulse may be applied.
- ② Input Data is loaded into the first word. The Data from the first word is released for "fall-through" to second word.
- ① Input Ready goes LOW indicating the first word is full.
- Shift-In going LOW allows Input Ready to sense the status of first word. The first word is now empty as indicated by Input Ready HIGH.
- (3) If the second word is already full then the data remains at the first word. Since the FIFO is now full Input Ready remains low. Note: Shift-in pulses applied while Input Ready is LOW will be ignored (See Figure 5).

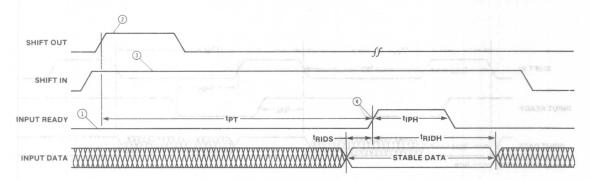


Figure 4. Data is Shifted in Whenever Shift In and Input Ready are Both HIGH

- ① FIFO is initially full.
- ② Shift Out pulsed is applied. An empty location starts "bubbling" to the front.
- 3 Shift In is held HIGH.
- (4) As soon as Input Ready becomes HIGH the Input Data is loaded into the first word.

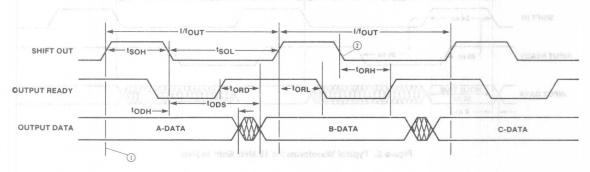


Figure 5. Output Timing

- ① The diagram assumes that at this time, words 63, 62 and 61 are loaded with A, B and C Data, respectively.
- ② Output data changes on the falling edge of SO after a valid Shift-Out Sequence, i.e. OR and SO are both high together.

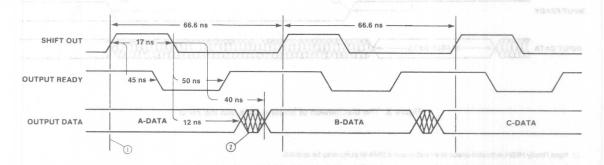


Figure 6. Waveforms for 15 MHz Shift-Out Data Rate

- ① The diagram assumes that at this time words 63, 62 and 61 are loaded with A, B and C Data, respectively.
- Data in the first crosshatched region may be A or B Data.



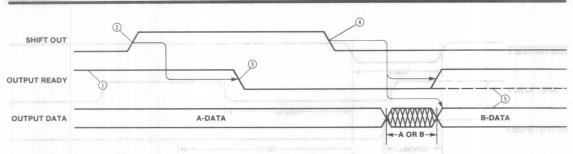


Figure 7. The Mechanism of Shifting Data Out of the FIFO

- ① Output Ready HIGH indicates that data is available and a Shift-Out pulse may be applied.
- ③ Shift-Out goes HIGH causing the contents of word 62 (B-Data) to be released for fall-through to word 63. Output data remains as valid A-Data while Shift-Out is HIGH.
- 3 Output Ready goes LOW.
- (4) Shift-Out goes LOW causing Output Ready to go HIGH and new data (B) to appear at the data outputs.
- (3) If the FIFO has only one word loaded (A-Data) then Output Ready stays LOW and the output data becomes invalid.

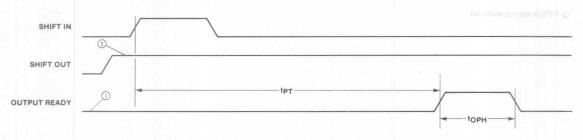


Figure 8. tpT and topH Specification

- ① FIFO initially empty.
- ② Shift Out held HIGH.

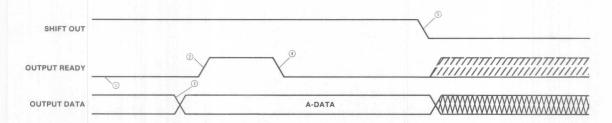


Figure 9. Data is Shifted Out Whenever Shift Out and Output Ready are Both HIGH.

- ① Word 63 is empty.
- Output Ready goes HIGH indicating arrival of the new data.
- 3 New data (A) arrives at the outputs (word 63).
- Since Shift Out is held HIGH, Output Ready goes immediately LOW.
- As soon as Shift Outgoes LOW the Output Data is subject to change. Output Ready will go HIGH or LOW depending on whether there are any additional upstream words in the FIFO.

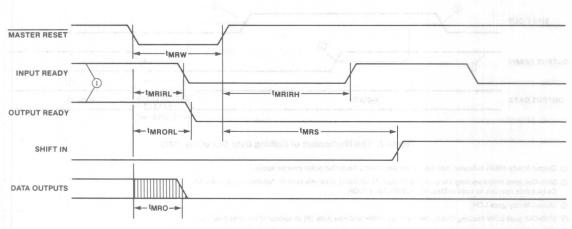


Figure 10. Master Reset Timing

© FIFO initially partially full.

RETHER AND TRANSPORT AND TRANSPORT

Introduction **Military Products Division** PROM PLE™ Devices **PAL®** Devices HAL®/ZHAL™ Devices System Building Blocks/HMSI™ FIFO **Memory Support Arithmetic Elements and Logic** Multipliers 8-Bit Interface **Double-Density PLUS™ Interface** ECL10KH 14 **Logic Cell Array** General Information 16 **Advance Information** Package Drawings 18 Representatives/Distributors

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8-Bit Dynamic-RAM Driver with Three-state Outputs SN54/74S730/-1

SN54/74S734/-1

Features/Benefits

- Provides MOS voltage levels for 16K and 64K DRAMs
- Undershoot of low-going output is less than -0.5 V
- Large capacitive drive capability
- · Symmetric rise and fall times due to balanced output impedence
- · Glitch-free outputs at power-up and power-down
- 20-pin SKINNYDIP®saves space
- 'S730/734 are exact replacement for the Am2965/66
- 'S730/734 are pin-compatible with 'S240/244, and can replace them in many applications
- 'S730-1/734-1 have a larger resistor in the output stage for better undershoot protection
- Commercial devices are specified at V_{CC} ± 10%

Description

The 'S730 and 'S734 are buffers that can drive multiple address and control lines of MOS dynamic RAMs. The 'S730 is an inverting driver, and the 'S734 is a non-inverting driver. The 'S730 is pin-compatible with the 'S240 and an exact replacement for the Am2965. The 'S734 is pin-compatible with the 'S244 and an exact replacement for the Am2966.

These devices have been designed with an additional internal resistor in the lower output driver transistor circuit, unlike regular 8-bit buffers. This resistor serves two purposes: it causes a slower fall time for a high-to-low transition, and it limits the undershoot without the use of an external series resistor.

Ordering Information

PART NUMBER	PKG	ТЕМР	ENABLE	POLARITY	POWER	
SN54S730/-1	J,W,L	Mil		Invert	14	
SN74S730/-1	N,J,NL	Com	Low	invert	S	
SN54S734/-1	J,W,L	Mil	i X	Non-	3	
SN74S734/-1	N,J,NL	Com	Low	Invert		

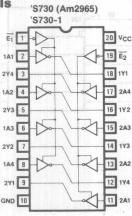
The 'S730 and 'S734 have been designed to drive the highlycapacitive input lines of dynamic RAMs. The drivers provide a guaranteed VOH of VCC-1.15 V, limit undershoot to 0.5 V, and exhibit a rise time symmetrical to their fall time by having balanced outputs. These features enhance dynamic RAM performance.

For a better-controlled undershoot for lightly capacitive-loaded circuits the 'S730-1 and 'S734-1 provide a larger resistor in the lower output stage. Also an improved undershoot voltage of -0.3 V is provided in the 'S730-1 and 'S734-1.

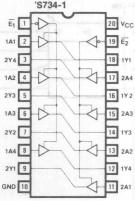
A typical fully-loaded-board dynamic-RAM array consists of four banks of dynamic-RAM memory. Each bank has its own RAS and CAS, but has identical address lines. The RAS and CAS inputs to the array can come from one driver, reducing the skew between the RAS and CAS signals. Also, only one driver is needed to drive eight address lines of a dynamic RAM. The propagation delays are specified for 50 pF and 500 pF load capacitances, and the commercial-range specifications are extended to VCC ±10%.

All of the drivers are available in 20-pin/DIP and 20-pin PLCC packages.





S734 (Am2966)



SKINNYDIP® is a registered trademarkof Monolithic Memories

TWX: 910-338-2376



Function Tables

'S730/-1

THE PROPERTY.	4960	31	30/-1	Total Million	uncurrent da monto
E1	E2	1A	2A	1Y	2Y
	L		L	Н	Н
onk on	rnd-Jod	a Laur	H-	Howe	TRAS
L	L	Н	L	L	HERE AN
L	L	Н	Н	L.L.	SNETS
L	Harri	L	X	H	Z
L	Н	Н	X	MILL F	SMIZSISS
Н	L	X	L	Z	Н
Н	L	X	H	Z	L
H	H	X	X	Z	ZMA

'S734/-1

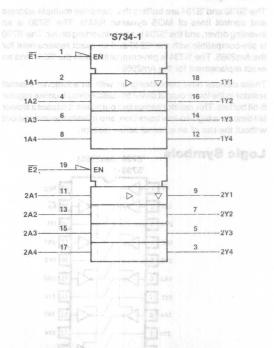
E1	E2	1A	2A	1Y	2Y
L	L.	L	1	L	1
L	MINNO DUN P	um vici io	H and	DIOS COM	H
L	V 8.0 Last	seaH ha	duo briog	wolfts to	derah
L	L	H vit	School over	Hinn	H
L	H	L	X	L	1 Z
L	nd no beone	SO HOUR	carry list		
Н	L	X	L	Z	pedent
Н	awab-awa	00 X	-iseHig is	elucZio e	HILLI
H	Н		X	-	

- ASSESSMENT and and and incommentation because one ASTICATE
- P 'S730/734 are pin-compatible with 'S140/2A4, and our
- '8730-1/734-1 have a larger rasis or in the output slage for botter understood erotection.
 - APO2 is now With National and applicable following applicable following

IEEE Symbol nii bevoromi ne osta, legate tugtuo vawot

'S730-1 EN 2 18 1Y1 1A1- ∇ ___1Y2 6 14 1Y3 1A3---12 1A4-----1Y4 19 11 ∇ -2Y1 13 15 243-17 2A4--

noliginoseC



Absolute Maximum Ratings

Supply voltage V _{CC}	0.5 V to 7 V
Input voltage	
Off-state output voltage	0.5 V to +V _{CC} max
Storage temperature range	65°C to +150°C
Output current	200 mA

Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN TYP MAX		COMMERCIAL MIN TYP MAX			UNIT	
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
TA	Operating free-air temperature	-55	uses str	125	0	115	75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMET	ERVAATUIA	TEST CONDITIONS			ITARY TYP MAX	COMMERC MIN TYP		UNIT
V _{IL} * XA	Low-level input v	oltage	\$1 MR			0.8		0.8	V
V _{IH} *	High-level input	voltage	4 tepa	= 0	2		2		V
VIC	Input clamp volta	age	V _C C = MIN	I _I = -18 mA		-1.2	anne e Lamel	-1.2	V
1.41	Low-level	Any A	P teda	V = 0.4 V		-0.2		-0.2	A
JIL SE	input current	Any E	VCC = MAX	V _I = 0.4 V		-0.4		-0.4	mA
Iн	High-level input	current	V _{CC} = MAX	V _I = 2.7 V	8.6	20	Idens tudtuč	20	μΑ
h 188	Maximum input of	current	VCC = MAX	V _I = 7 V		0.1		0.1	mA
V	95		VCC = MIN	IOL = 1 mA	80	0.5	dsait legs. C	0.5	KJ9
V _{OL} an	Low-level output	voitage	V _{IL} = 0.8 V V _{IH} = 2 V	IOL = 12 mA		0.8		0.8	V
Vон	High-level output	t voltage	V _{CC} = MIN V _{IL} = 0.8 V V _{IH} = 2 V	0.8 V IOH = -1 mA		VCC -0.7	VCC VCC -1.15 -0.7	o soram	V
lozL			VCC = MAX	V _O = 0.4 V		-200	P. Cifet · reck v	-200	μΑ
lozh	Off-state output of	current	V _{IL} = 0.8 V V _{IH} = 2 V	V _O = 2.7 V		100	La area (1891)	100	μΑ
los	Output short-circ	cuit current †	VCC = MAX	100 - 100 -	-60	-200	-60	-200	mA
TIMU XA	S NYT MIM	NYT MIN CHOT		'S7XX	50	11.0 / 3/44.41	50	-13	ESTATE OF
OL	Output sink curre	ent	V _{OL} = 2.0 V	'S7XX-1	40		40		mA
ГОН	Output source cu	urrent	V _{OH} = 2.0 V	ltai	-35	yaleb tuq	-35		mA
91		Outputs	106 = JO	'S730/-1		24 50	24	50	19/97
02		high	102 = _O	'S734/-1		53 75	53	75	
20 02	Sr	Outputs	VCC = MAX	'S730/-1		86 125	86	125	124
lcc ·	Supply current	low	Outputs open	'S734/-1		92 130	92	130	mA
20 85		Outputs	1= 8	'S730/-1		86 125	86	125	214
Sr		disabled	5 = 3	'S734/-1		116 150	116	150	744

[†] Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

^{*} These are absolute voltages with respect to pin 10 on the device and includes all overshoots due to system and/or test noise. Do not attempt to test these values without suitable equipment.

Absolute Maximum Rati

Switching Characteristics V_{CC} = 5 V, T_A = 25°C For the 'S730 and 'S734

SYMBOL	PARAMETER	FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
Orden d	5 % Sec.		C _L = 50pf	6	9	15	IDETOIS	
^t PLH	Data to output delay	1 & 3	C _L = 500pf	18	22	30	diadinic	
	Data to output delay	1.00	C _L = 50pf	5	7	15	ns	
^t PHL			C _L = 500pf	18	22	30		
tPZL			S = 1	2 3 5 6 7 5	12	20	acrel o	
t _{PZH}	Output enable delay 2 & 4 S = 2	2 & 4	2 & 4	S = 2		12	20	ns
t _{PLZ}	Output disable delay	2 & 4	S = 1		- 11	20		
t _{PHZ}	Output disable delay	204	S = 2	Reston	6.5	12	ns	
tSKEW	Output-to-output skew	1 & 3	C _L = 50pf	संबंधिता	±0.5	±3.0	ns	
VONP	Output voltage undershoot	1 & 3	C _L = 50pf		0	-0.5	V	

^{*}The SKEW timing specification is guaranteed by design, but not tested.

Switching Characteristics Over Operating Range** For the 'S730 and 'S734 and Sanda Balance Sanda Sanda

SYMBOL	PARAMETER 971	FIGURE	TEST CONDITIONS		LITARY †† = 5.0V ±10% TYP MAX	COMMERC V _{CC} = 5.0V MIN TYP	±10%	UNIT	
+2	3	0	C _L = 50pf	4	20	4 levst-dgiM	17	1-0-V	
^t PLH	Data ta a da	100	om 8r C _{Li} = 500pf	18	40	18 sta turni	35	ns	
	Data to output delay	Data to output delay	1 & 3	C _L = 50pf	4	A yr. 20	4 toyst-art	17	
^t PHL			C _L = 500pf	18	3 VA 40	118 tuo lugra	35	311	
†PZL	Output enable delay	2 & 4	V TS S N= 1+ XAM = 0	ov I	ton 13 28	ini isvel-rigirl	28	ns	
t _{PZH}	Output enable delay	204	V S = 2+ XAM = 0	oV	28	Maximum ind	28	ris	
t _{PLZ}	Output disable delay	2 & 4	S = 1+ MM = 3	OV	24		24	ns	
t _{PHZ}	Output disable delay	2 0. 4 A	S = 2†	IIIV	16	t.o lever-wo.i	16	115	
VONP	Output voltage undershoot	1 & 3	C _L = 50pf	m. L.	-0.5		-0.5	V	

[&]quot;AC performance over the operating temperature is guaranteed by testing as defined in Group A, Subgroup 9, Mill Std 883B. W 300 loss 4 10 lb.

Switching Characteristics V_{CC} = 5 V, T_A = 25°C For the 'S730 and 'S734

SYMBOL	PARAMETER	FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Am	40 40	870(-1	C _L = 50pf	6	9	15	70,
^t PLH	Data to output delay	1 & 3	C _L = 500pf	18	22	30	ns
+ 03	NG 50 Bg	1-70828,	C _L = 50pf	5	7	15	HIS
^t PHL	ga pa	1 1 0 0 0 0	C _L = 500pf	18	22	40	
tPZL	0.4.4.4.4.1.23	0.0012	S = 1		12	20	
t _{PZH}	Output enable delay	2 & 4	S = 2	ineriua	12	20	ns
tPLZ	Output disable delay	2 & 4	S = 1		11	20	
tPHZ	Output disable delay	1.0.000	S = 2		6.5	12	ns
tSKEW	Output-to-output skew	1 & 3	C _L = 50pf		±0.5	±3.0	ns
VONP	Output voltage undershoot	1 & 3	C ₁ = 50pf	no House to	0	-0.3	V

^{*}The SKEW timing specification is guaranteed by design, but not tested.

^{†&}quot;S = 1" and "S = 2" refer to the switch setting in Figure 2.

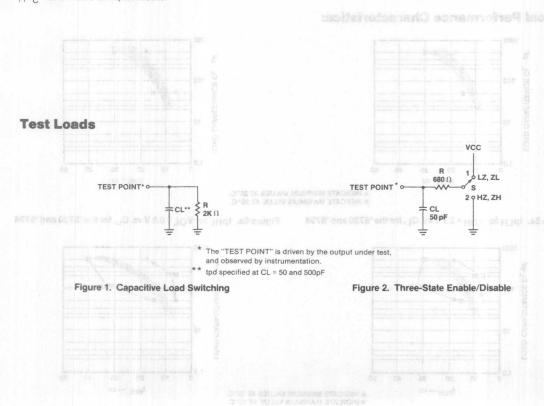
^{††}T_C = -55 to + 125° C for flatpack versions.

Switching Characteristics Over Operating Range** For the 'S730 and 'S734

SYMBOL	PARAMETER	FIGURE	TEST CONDITIONS	$\begin{array}{c} \text{MILITARY } \uparrow \uparrow \\ \text{V}_{\text{CC}} = 5.0 \text{V} \pm 10 \% \\ \text{MIN} \text{TYP} \text{MAX} \end{array}$		UNIT
1959		(149)	C _L = 50pf	4 20	4 17	
^t PLH	Date to sutant delay		C _L = 500pf	18 40	18 35	ns
W.	Data to output delay	1 & 3	C _L = 50pf	4 20	4 17	ns
^t PHL			C _L = 500pf	18 50	18 45	
t _{PZL}	Output enable delay	2 & 4	S = 1†	28	28	
t _{PZH}	Output enable delay	2 0.4	S = 2†	9/5/ 28	28	ns
tPLZ	Output disable delay	2 & 4	S = 1†	24	24	-
tPHZ	Output disable delay	204	S = 2†	16	16	ns
VONP	Output voltage undershoot	1 & 3	C _L = 50pf	-0.3	-0.3	V

^{**}AC performance over the operating temperature is guaranteed by testing as defined in Group A, Subgroup 9, Mil Std 883B.

^{††}T_C = -55 to + 125° C for flatpack versions.



^{†&}quot;S = 1" and "S = 2" refer to the switch setting in Figure 2.

Typical Switching Characteristics

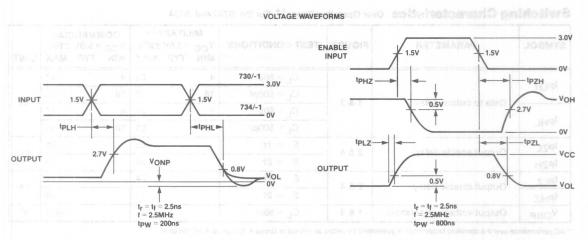
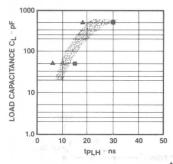
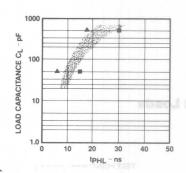


Figure 3. Output Voltage Levels

Figure 4. Three-State Control Levels

Typical Performance Characteristics:

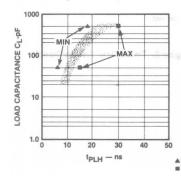




▲ INDICATE MINIMUM VALUES AT 25°C.
■ INDICATE MAXIMUM VALUE AT 25°C.

Figure 5a. tpLH for VOH = 2.7 V vs. CL, for the 'S730 and 'S734

Figure 6a. tpHL for VOL = 0.8 V vs. CL, for the 'S730 and 'S734



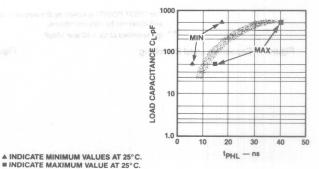


Figure 5b. tpLH for VOH = 2.7 V vs. CL, for the 'S730-1 and 'S734-1

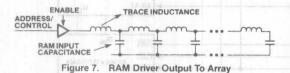
Figure 6b. tpHL for V_{OL} = 0.8 V vs. C_L, for the 'S730-1 and 'S734-1

9

Applications

The 'S730 and 'S734 are 8-bit bipolar dynamic RAM drivers and are pin-compatible with the 'S240 and 'S244 respectively.

The actual circuit conditions that arise for driving dynamic RAM memories are as follows: Typically, in dynamic RAM arrays address lines and control lines, RAS, CAS, and WE have a fair amount of "daisy chaining." The daisy chaining causes an inductive effect due to the traces in the printed circuit board; the dominant factor in the RAM loading is input capacitance, and these two conditions contribute to the actual driver conditions shown in Figure 7. The result is a transmission line with distributed inductance and capacitance connected to the driver outputs.



The transmission line effect can imply reflections, which in turn cause ringing, and it takes some time before the output settles from the low-to-high transition. On the high-to-low transition, along with ringing, a voltage undershoot can occur, and the circuit takes even longer to settle to an acceptable zero level. The main cause for the shorter high-to-low transition as compared to the low-to-high transition is the output impedance of typical Schottky drivers. Figure 8, shows a typical Schottky driver output stage and Figure 9 shows the output impedance for high and low output states.

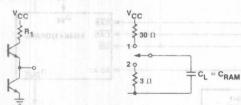


Figure 8. Typical Schottky Driver Output

Figure 9. Driver-Output Impedance

In Figure 9 when S=1, the output is high and the driver output impedance is approximately 30 Ω . When S=2, the output is low and the driver output impedance is approximately 3 Ω . There is a 10:1 ratio for the output impedances for the low and high states. The high-to-low transition causes a problem as the output transistor turns on fast due to the low impedance and undershoot results at the RAM inputs.

$$V_{CC}$$
 R_1
 R_1
 R_2
 R_3
 R_4
 R_5
 R_5
 R_5
 R_5
 R_6
 R_6
 R_7
 R

Figure 10. 'S730 and 'S734 Output Stage

Figure 11. Driver Output Impedence For the 'S730 and 'S734

The 'S730 and 'S734 have a modification in their output stage, in that an internal resistor is added to the lower output stage as shown in Figure 10.

The 'S730-1 and 'S734-1 have a larger resistor, R2, comparted to the "non-dash" parts, which give better undershoot protection at a slightly slower switching performance.

The structure in Figure 10 provides a driver output impedence of approximately 18 Ω to 25 Ω in either high (S = 1) or low (S = 2) states as shown in Figure 11. In addition, this circuit limits undershoot to -0.5 V, essentially eliminating that problem; provides a symmetrical rise and fall time; and guarantees output levels of VCC-1.15 V needed for MOS High levels. Also, when using the 'S730 asnd 'S734, no external resistors are needed. 'S240-series parts used with external resistors to provide drive capability, but the rise times and fall times are unsymmetrical due to higher impedance for low-to-high transitions.

Figure 12 shows the undershoot problem using a 'S240 without external resistors and the elimination of the problem by using the 'S730. Thus from a dynamic-RAM system-design viewpoint, the 'S730 and 'S734 are very effective RAM drivers.

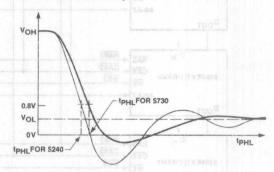


Figure 12. Comparison of Undershoots and town

An application using these 8-bit drivers to interface address and control lines (and data lines) to a dynamic RAM array using 64K DRAMs is discussed. The signals needed for the controls are RAS, CAS, and WE. The address lines are A0-A7 and the data lines are shown as the high and low byte. The array is shown in Figure 13. It consists of four rows of DRAMs; each row has individual RAS, CAS, and WE lines. However, all four rows have common address lines A0-A7. The RAM capacitive loading for RAS, CAS, and WE is about 10 pf per input. The loading of the address lines is about 5 to 7 pf per input. The loading of the RAS; CAS; and WE; inputs to each row of memories is 160 pf. Note that RAS; and CAS; come from the same driver, which reduces timings skews which might arise if they were output from separate drivers. The address lines are outputs from another driver, and the loading on each line is 320 pf (5 pf loading times 64 DRAMs). At this point it is worth noting that if a 320-pf loading affects performance unduly, then the address lines can be split between two drivers with each having a load of 160 pf, reducing overall signal delay.

If an error-detection-and-correction scheme is used, then typically the row size expands to 22 bits from the 16 bits shown in the example. The 'S730 and 'S734 drivers lend themselves to such expansion, as their propagation delays are specified at 50 pF and also at 500 pF.

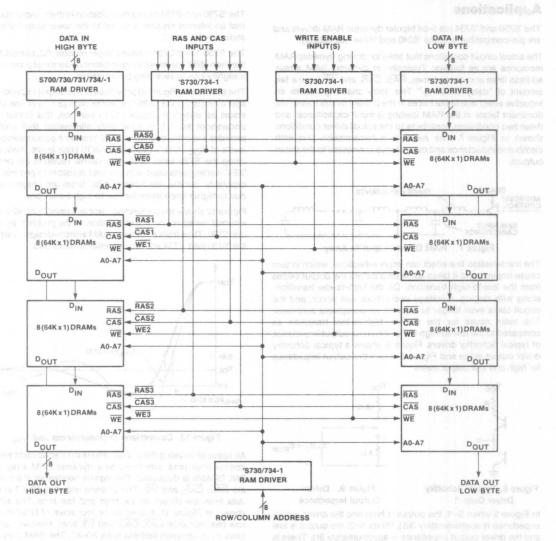


Figure 13. 256K X 16 Dynamic RAM Array with RAM Drivers

48 AUTO

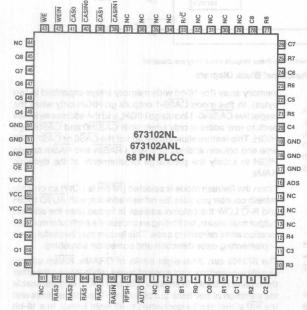
47 RFSH

Features/Benefits

- Supports 16K, 64K, and 256K DRAMs
- Capable of addressing up to 2 M 16-bit words or 2 M bytes
- On-chip capacitive-load drivers are capable of driving up to 88 DRAMs with 30-nsec typical address propagation delay and 128 DRAMs with 35-nsec typical address propagation delay
- RASIN to RAS delay of 20 nsec max (RAS driving 22 DRAMs)
- . Max and Min skews are specified to simplify system design
- Two CASIN inputs and two CAS outputs simplify byte
- An Auto-Access mode with extended CAS capability takes advantage of full performance of 120 and 150 nsec DRAMs
- · An output series resistor reduces undershoot

Modes of Operation

- Externally Controlled Access (ECA)
- Auto Access (AA)
- Refresh

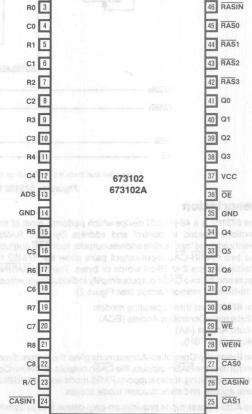


Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
673102	48D, 48N, 68NL,	C
673102A	68NP	Com

Pin Configurations

B1 2



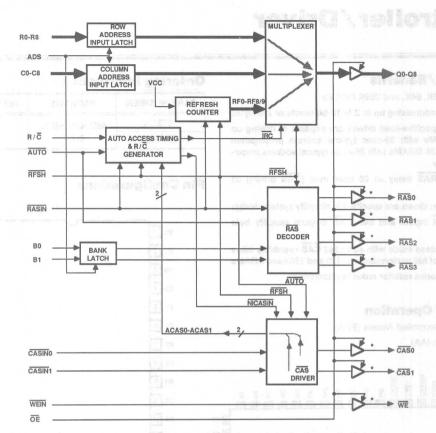
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* Indicates that there is a 3-K Ω pull-up resistor on these outputs when they are disabled

Figure 1. 673102 Functional Block Diagram

Description

The 673102 is a 48-pin LSI device which performs most of the functions needed to control and address Dynamic RAMs. Twenty address inputs, nine address outputs, four RAS outputs, and two CASIN-CAS input-output pairs allow the 673102 to directly address 2 M 16-bit words or bytes. The two CASINn inputs and the two CAS noutputs simplify individual byte access in 16-bit wide memory arrays (see Figure 2).

The 673102 has three operating modes:

- Externally Controlled Access (ECA)
- Auto Access (AA)
- · Refresh (RFSH).

The Externally-Controlled-Access mode gives the system direct control over the RASm outputs, the CASn outputs, and Row/Column multiplexing. It also supports PAGE mode access, NIBBLE mode access, and static column mode access.

The Auto-Access mode provides on-chip delays that automatically control the timing delays between RASm signals, address multiplexing, and CASn signals. In the Auto-Access mode CASIN0-1 inputs serve as enables for the respective CAS0-1 outputs, allowing the access of either or both bytes of the

memory array (for 16-bit wide memory arrays organized in two bytes). In this mode CAS0-1 outputs go HIGH only when the respective CASIN0-1 inputs go HIGH, and the address switches back to row address only when both CASIN0 and CASIN1 go HIGH. This feature allows extension of the CAS0 or CAS1 LOW time and column address time while RASIN and RASm can go HIGH to satisfy the precharge requirements of the dynamic RAMs.

When the Refresh mode is selected (RFSH is LOW) an on-chip refresh counter provides the refresh address; with AUTO HIGH and R/C LOW the column address is forced onto the address output multiplexer, facilitating an access of a particular memory location while refreshing a row. This feature may be useful when implementing error detection and correction scrubbing.

The 673102 can drive eight banks of DRAMs. \overline{RASm} control signals are used to select a pair of banks, while leaving the other three pairs of banks in standby. The two \overline{CASn} outputs enable the selection of one bank out of the pair. The address lines and the \overline{WE} signal can be connected to all eight banks. In a 16-bit wide, byte-oriented, memory array the \overline{RASm} signals select one out of four banks while the CASn signals select the bytes as shown in Figure 2.

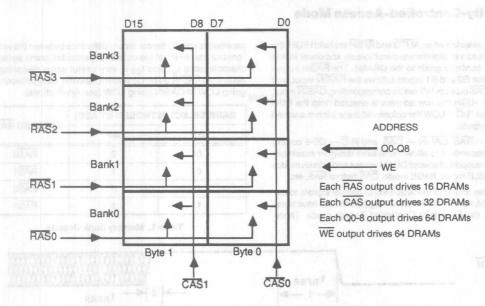


Figure 2. 673102 Addressing Four Banks of 16-bit Memory Array Organized in Two Bytes

Pin Definitions

VCC, GND: VCC-GND = 5 V ±10%. The supply pins have been assigned to the center of the package to reduce voltage drops, both DC and AC. A low-inductance connection between the ground pin and a solid ground plane will minimize fluctuations in the ground level of the device that may occur when the address outputs switch from HIGH to LOW simultaneously. A 1 μF multilayer ceramic capacitor in parallel with a low-voltage tantalum capacitor, both connected close to the VCC and GND pins, will properly decouple the device.

R0-R8: Row Address Inputs

C0-C8: Column Address Inputs

B0-B1: Bank-Pair Select Inputs — Strobed by ADS. Decoded to enable one of the RAS outputs when RASIN goes LOW in the access modes.

Q0-Q8: Multiplexed Address Outputs — Selected from the row address input latch, the column address input latch, or the refresh counter.

RASIN: Row Address Strobe Input — Drives the selected RASm output in the access modes and all RAS outputs in the Refresh mode.

ADS: Address (Latch) Strobe Input — Strobes input row address, column address and Bank Select inputs into the respective latches when HIGH; latches on HIGH-to-LOW transition.

OE: Output Enable — When OE is LOW the address and control outputs are enabled. When OE is HIGH the address outputs are in high-impedance and the control outputs are pulled HIGH.

R/C: Row/Column Select Input — In the Externally-Controlled-Access mode it is used to select either the row address input latch or the column address input latch onto the address outputs. In the Refresh mode, when AUTO is HIGH, it is used to select between the refresh address (R/C HIGH) and the column address (R/C LOW). When AUTO is LOW R/C is disabled.

CASINO-1: Column Address Strobe Inputs — In the Externally-Controlled-Access mode the CASINn directly drives CASn output. In the Auto-Access mode each is used to enable the corresponding CASn output (See CAS0-1 description).

WEIN: Write Enable Input.

WE: Write Enable Output.

CAS0-1: Column Address Strobe Outputs — In the Externally-Controlled-Access mode the CAS outputs follow the CASIN inputs. In the Auto-Access mode the CASIN inputs are used to enable the CAS outputs. The CAS outputs are asserted LOW, with proper delay from the RAS output, by the RASIN signal via the Auto-Access timing generator. In the Auto-Access mode, the CASn goes HIGH only when the corresponding CASIN goes HIGH. Extending the CASn LOW duration while RASIN and RASIN go HIGH satisfies the precharge requirement of the dynamic RAMs.

RAS0-3: Row Address Strobe Outputs — When RFSH is HIGH the selected row address strobe output (decoded from signals B0, B1) follows the RASIN input. When RFSH is LOW all RAS outputs go LOW together following RASIN going LOW.

AUTO: Auto-Access Input — When AUTO is LOW and RFSH is HIGH the Auto-Access mode is selected (see Auto-Access mode description).

 $\overline{\text{RFSH}}$: Refresh Input — When $\overline{\text{RFSH}}$ is LOW the Refresh mode is selected (see Refresh mode description).

Externally-Controlled-Access Mode (ECA)

In this mode, selected when $\overline{\text{AUTO}}$ and $\overline{\text{RFSH}}$ are held HIGH, the 673102 serves as a straightforward multiplexer and driver for the address and control signals to the DRAMs. The $\overline{\text{RAS}}$ m output selected by the B0 and B1 inputs follows the $\overline{\text{RAS}}$ IN input, and each of the $\overline{\text{CAS}}$ outputs follows its corresponding $\overline{\text{CASIN}}$ input. When $\overline{\text{R/C}}$ is HIGH the row address is enabled onto the Q0-8 outputs. When $\overline{\text{R/C}}$ is LOW the column address latch is enabled onto Q0-8 outputs.

The RASIN — RAS, CASIN — CAS, and R/C — Q0-8 control paths are independent to allow the system designer maximum flexibility and support of special DRAM access and refresh modes such as NIBBLE mode, PAGE mode, CAS before RAS, etc.

To allow tighter timing of the sequence of control signals to the Dynamic RAM, several difference timing parameters have been specified for the Externally Controlled Access mode. These

parameters specify the maximum difference between the various "control channels" of the device. In particular, using switching characteristics t_{d7} and t_{d8} is very useful when designing the delay from RASIN going LOW to R/C and the delay between R/C going LOW to CASIN going LOW (see Applications).

BANK SELECT (S	ENABLED RASh		
B1	В0	ENABLED RASI	
0	0	RAS0	
0	1	RAS1	
	0	RAS2	
1	1	RAS3	

Table 1. Memory Bank Decode

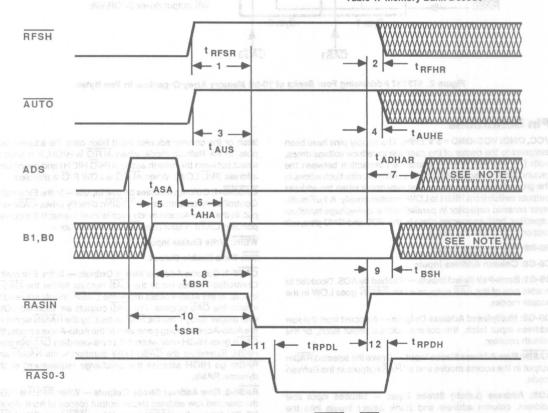


Figure 3. Externally-Controlled-Access—RASIN-to-RAS Timing

Note: To prevent glitches on the RAS0-3 outputs, operating conditions tash or tables must be satisfied.

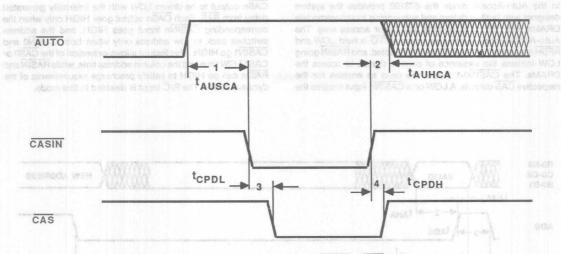


Figure 4. Externally-Controlled-Access-CASIN to CAS Timing

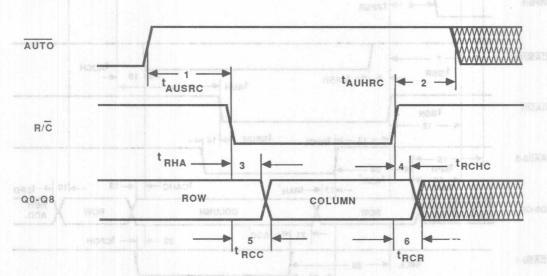


Figure 5. Externally-Controlled-Access R/C Timing

Note: t_{RCC} will be met only if the column address is available t_{APD} before it appears on Q0-8 outputs or if it is latched by ADS.

Auto-Access Mode (AA)

In the Auto-Access mode the 673102 provides the system designer with built-in delays and sequencing to accommodate DRAMs with 150 nanoseconds and faster access time. The Auto-Access mode is selected when AUTO is held LOW and RFSH is held HIGH. The R/C input is disabled, and RASIN going LOW initiates the sequence of control signals to access the DRAMs. The CASIN0-1 inputs are used as enables for the respective CAS outputs. A LOW on a CASINn input enables the

CASn output to be driven LOW with the internally generated delay from RAS. Each CASn output goes HIGH only when the corresponding CASINn input goes HIGH, and the address switches back to row address only when both CASIN0 and CASIN1 go HIGH. This feature allows extension of the CAS0 or CAS1 LOW time and the column address time, while RASIN and RASm can go HIGH to satisfy precharge requirements of the dynamic RAMs. The R/C input is disabled in this mode.

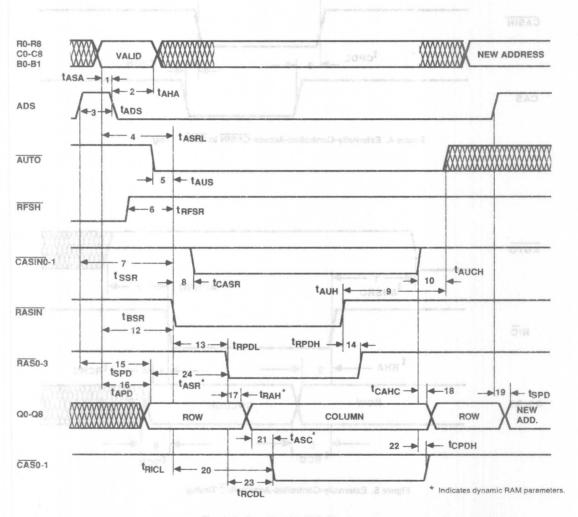


Figure 6. Auto-Access (AA) Timing

9

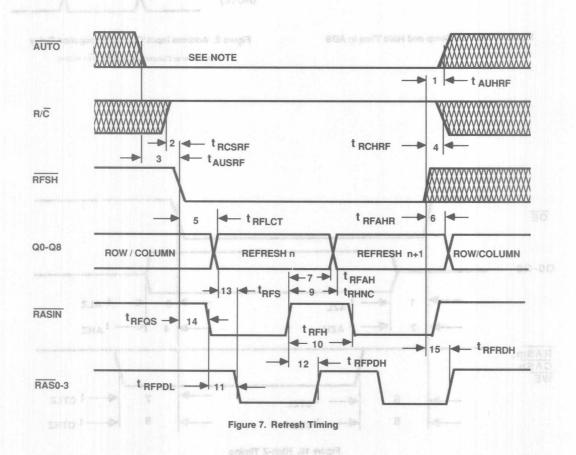
Refresh Mode (RFSH)

When $\overline{\text{RFSH}}$ is held LOW the refresh counter contents are enabled onto the Q0-8 address outputs, provided either R/\overline{C} is held HIGH, or $\overline{\text{AUTO}}$ is held LOW, or both conditions exist. In this mode all four $\overline{\text{RAS}}$ outputs follow the $\overline{\text{RASIN}}$ input signal. The refresh counter increments the refresh address when either $\overline{\text{RASIN}}$ or $\overline{\text{RFSH}}$ goes HIGH while the other is LOW. When $\overline{\text{AUTO}}$ is LOW the $\overline{\text{CASIN}}$ 0-1 inputs are isolated and $\overline{\text{CASO}}$ -1 are held HIGH. Also, when $\overline{\text{AUTO}}$ is LOW the R/\overline{C} input is isolated from the output multiplexer, and the refresh address appears at the Q0-8 outputs.

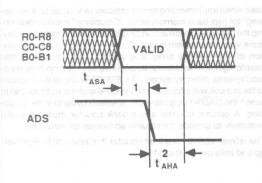
When AUTO is HIGH, pulling R/C LOW enables the column address onto the Q0-8 outputs. Also, each of the CAS outputs follows its corresponding CASIN input. This feature may be

used when implementing error correction and detection "scrubbing" for two-bank memory array. "Scrubbing" is a term describing the cyclic error correction of soft errors in the memory array, done within the refresh cycles. On every refresh cycle one location of the memory array is accessed, and the data in that location goes, if necessary, through a correction cycle (a readmodify-write memory cycle). The 673102 provides the facilities to force a column address onto the Q0-8 address outputs and to assert the CASO-1 outputs within a refresh cycle to allow scrubbing. A column counter and a bank counter must be added externally to provide the column addresses for scrubbing.

The refresh counter is a 9-bit counter that resets to 0 on power-up and rolls over to 0 at 511.



Note: In the REFRESH mode, AUTO must be LOW or R/C must be HIGH to guarantee the refresh address on the Q0-8 outputs.



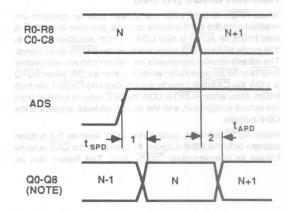


Figure 8. Address Setup and Hold Time to ADS

Figure 9. Address Input/Output Propagation Delay

Note: Row or Column address (RFSH = HIGH).

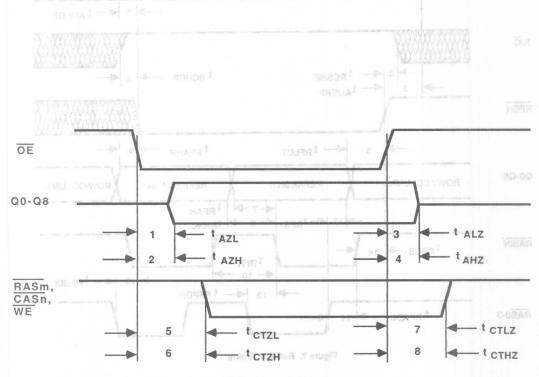


Figure 10. High-Z Timing

Electrical Characteristics V_{CC} = 5 V \pm 10%, 0°C \leq T_A \leq 75°C. Typicals are for V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER SHUSS	CONDITIONS	FIGURE/ NUMBER	MIN TYP MAX	UNIT
VIC	Input clamp voltage	I _{IN} = -18 mA, V _{CC} = MIN	lieb WO 15	-0.8 -1.2	V
TIH.	Input high current	V _{IN} = 2.7 V, V _{CC} = MAX	veleb WO.I	50	μΑ
ICTL 0	Output load current for RAS, CAS, WE	VOUT = 0.4 V, VCC = MAX Chip deselect	S LOW dela	-1.5 -2.5	mA
IIER IE	Input low current except for RFSH	VIN = 0.4 V, VCC = MAX	ep Hoin a	-20 -250	μΑ
ILRF	Input low current for RFSH	V _{IN} = 0.4 V, V _{CC} = MAX	indino of tr	-80 -500	μА
VIL	Input low threshold (Note 1)	LIBOURE	Valsb WOJ	0.8	O V
VIH	Input high threshold (Note 1)	E MUMBER BAN	I Stab HAIH	2.0	V
VOL1	Output low voltage	IOUT = 1 mA, VCC = MIN	eb HOIE P	O 61 ARAO 0.5	V
VOL2	Output low voltage	IOUT = 12 mA, VCC = MIN	Hemit blow	8.0 Row at tres	HV
VOH	Output high voltage	IOUT = -1 mA, VCC = MIN	at to output	2.4 3.0	Vo
Іон 📑	Output source current (Note 2)	VOUT = 0.8 V, VCC = MIN	o address of	-50 -140	mA
IOL	Output sink current (Note 2)	VOUT = 2.4 V, VCC = MIN	order see	40 100	mA
loz	Three-state output current (address output)	0.4 V ≤ V _{OUT} ≤ 2.7 V V _{CC} = MAX, Chip deselect	diamin,eco	-50 50	μΑ
lcc	Supply current	VCC = MAX		150 240	mA
CIN	Input capacitance	T _A = 25° C	IN TRACT	10	pF

Switching Characteristics (See Note 3)

SYMBOL	EXTERNALLY CONTROLLED ACCESS PARAMETER	FIGURE/ NUMBER	673102A MIN TYP MAX	673102 MIN TYP MAX	UNIT
t _{RHA}	Row addresses remaining valid from R/C LOW	5/3	Our of blood base	0	ns
tRPDL	RASIN to RAS LOW delay	3/11	20	20	ns
tRPDH	RASIN to RAS HIGH delay	3/12	of HOTH SA 31	HOIH HEAR 31	ns
tAPD 8	Address input to output delay	9/2	1-1vslsb Hon 50	50 Alexandr 50	ns
tWPDL	WEIN to WE LOW delay	PARKAMETE	45	45	ns
tWPDH	WEIN to WE HIGH delay	W	40	40	ns
tCPDL	CASIN to CAS LOW delay	4/3	28	011/01/30 28	ns
tCPDH	CASIN to CAS HIGH delay	4/4	40	August 40	ns
tRCC	Column select to column address valid	5/5	41	41	ns
tRCR	Row select to row address valid	5/6	45	45	ns
t _{d1}	(CASIN to CAS LOW delay)-(RASIN to RAS LOW delay)	6/8/10	-2 13	-2 13	ns
t _{d2}	(Address input to output delay)-(RASIN to RAS LOW delay)	100	30	30	ns
t _{d3}	(Address input to output delay)-(CASIN to CAS LOW delay)	105,110113	-5 23	-5 23	ns
t _{d4}	Skew between address output lines	zale mon a	10	10	ns
t _{d5}	(RASIN to RAS HIGH delay)-(RASIN to RAS LOW delay)	Linuage and at I	-7 13 13 13 13 I	10-7 lulosda ena 137	ns
t _{d6}	(CASIN to CAS HIGH delay)-(CASIN to CAS LOW delay)	annops ortens	-12 12	-12 12	ns
tSPD	ADS HIGH to address output valid	9/1	55	55	ns
tRCHC	Column addresses remaining valid from R/C HIGH	5/4	0	0	ns
t _{d7}	tRPDL - tRHA	7/10	13	13	ns
t _{d8}	tRCC - tCPDL	2714	20	20	ns

SYMBOL	AUTO ACCESS PARAMETER	FIGURE/ NUMBER	673102A MIN TYP MAX	673102 MIN TYP MAX	UNIT
tRICL **	RASIN to CAS LOW delay	6/20	75	85	ns
tRCDL	RAS to CAS LOW delay	6/23	30 65	30 75	ns
tRPDL	RASIN to RAS LOW delay	6/13	20 a	bselfected 20	ns
tRPDH	RASIN to RAS HIGH delay	6/14	31	31	ns
tAPD	Address input to output delay	6/16	50	50	ns
tWPDL	WEIN to WE LOW delay		45	45	ns
tWPDH	WEIN to WE HIGH delay		40	40	ns
tCPDH	CASIN to CAS HIGH delay	6/22	40	40	ns
tRAH	Row address hold time from RAS LOW	6/17	15 apolio	15 Jugino	ns
t _{d2}	(Address input to output delay)-(RASIN to RAS LOW delay)		30	right telephic 30	ns
tSPD	ADS HIGH to address output valid	6/19	3 eto/4) 55	muca highe 55	ns
tASC	Column address setup to CAS LOW	6/21	oS edi. A trismino	Oils flugtinO	ns
tCAHC	Column address remaining valid from CASIN0-1 HIGH	6/18	5 manus tustin	5	ns
tASR	Row address valid before RAS LOW	6/24	0	0	ns
t _{d5}	(RASIN to RAS HIGH delay)-(RASIN to RAS LOW delay)		-7 13	-7 13	ns
na na tito (tilano no se	REFRESH PARAMETER	Chippen de l'annun ma	The Control of the Co		- Company
^t RFLCT	RFSH LOW to refresh address valid (AUTO LOW or R/C HIGH)	7/5	40	40	ns
tRFPDL	RASIN LOW to RAS LOW delay during refresh	7/11	23	23	ns
tRFPDH	RASIN HIGH to RAS HIGH delay during refresh	7/12	38	38	ns
tRFAH	Refresh address held from RASIN HIGH (RFSH LOW)	7/7	0	0	ns
tRHNC	RASIN HIGH to new refresh address valid	7/9	66	66	ns
treahr.	Refresh address held from RFSH HIGH	7/6	0	0	ns
tRFS	Refresh address valid to RAS LOW (provided tRFQS is satisfied)	7/13	o yalab WOJ &	Flow address FASIN to A	ns
tRFRDH	RFSH HIGH to RAS HIGH (for 3 banks, RASIN = LOW)	7/15	Valentie 40	A 01 11 2 40	ns
t _d 9	(RASIN to RAS HIGH delay)-(RASIN to RAS LOW delay)		-915 Justice 16	-9 49 DA 16	ns
av ga	THREE-STATE PARAMETER		LOW duay	WEIN to Wi	Odw
t _{AZL}	OE LOW to address output LOW	10/1	45	W of 1/13/1/ 45	ns
t _{AZH}	OE LOW to address output HIGH	10/2	60	O OT 1/18 AO 60	ns
tALZ	OE HIGH to address output HI-Z from LOW	10/3	35	35 A MICAU	ns
tAHZ	OE HIGH to address output HI-Z from HIGH	10/4	25	25	ns
tCTZL	OE LOW to control output LOW	10/5	40	40	ns
tCTZH	OE LOW to control output HIGH	10/6	50	50	ns
tCTLZ	OE HIGH to control output HI-Z from LOW	10/7	30	30	ns
tCTHZ	OE HIGH to control output HI-Z from HIGH	10/8	25	25	ns.

Note 1: These are absolute voltage levels with respect to the ground pins on the device and includes all overshoots due to system or tester noise.

Do not attempt to test these values without suitable equipment.

Note 2: This test is provided as a monitor of driver output source and sink current capability. Caution should be exercised in testing this parameter.

One output should be tested at a time and test duration should not exceed one second.

Note 3: Output load capacitance is typical for four banks of 22 DRAMs with trace capacitance,
The values are: Q0-8 C_L = 500 pF, RAS0-3 C_L = 150 pF, WE C_L = 500 pF, CAS0-1 C_L = 300 pF.

2

Absolute Maximum Ratings (See Note)

Supply voltage, VCC	-0.5 V to 7 V
Storage temperature range	C to +150°C
Input voltage	.5 V to 5.5 V
Output current	
Lead temperature (soldering, 10 seconds)	300°C

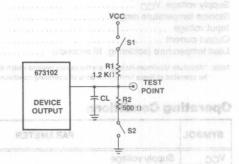
Note: "Absolute Maximum Ratings" are the values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of operating conditions provides conditions for actual device operation.

Operating Conditions

SYMBOL	PARAMETER		673102A MIN TYP MAX		673102 MIN TYP MAX		UNIT
VCC	Supply voltage		4.5	5.5	4.5	5.5	V
TA	Ambient temperature		0	75	0	75	C
tASA	Address setup time to ADS LOW	8/1	18		18		ns
tADS	Address strobe pulse width HIGH		26		26	0	ns
tAHA	Address hold time from ADS LOW	8/2	10		10		ns
	EXTERNALLY CONTROLLED ACCESS PARAMETER						
†ADHAR	ADS LOW hold from RASIN HIGH	3/7	0	o Delaw	0	S ol one	ns
tBSR	Bank select setup to RASIN LOW (ADS = HIGH)	3/8	10	arive to t	10	Capacil	ns
tBSH	Bank select hold from RASIN HIGH (ADS = HIGH)	3/9	10		10		ns
tssr	Address strobe HIGH setup to RASIN LOW (B0, B1 STABLE)	3/10	20		20	O nee	ns
†AUHE	AUTO hold from RASIN HIGH	3/4	55		55		ns
†AUSRC	AUTO HIGH setup to R/C LOW	5/1	25	38	25		ns
tAUHRC	AUTO HIGH hold from R/C HIGH	5/2	10	besol	10	gO .	ns
†AUSCA	AUTO HIGH setup to CASIN LOW	4/1	45 008	bseol	45	6131	ns
tAUHCA	AUTO HIGH hold from CASIN HIGH	4/2	0	hetor	0	0	ns
tAUS	AUTO setup to RASIN LOW	3/3	0	hasel	0	ara T	ns
tRFSR	RFSH HIGH setup to RASIN LOW (to guarantee tASR)	3/1	10	1	10		ns
†RFHR	RFSH HIGH hold from RASIN HIGH	3/2	10		10	era-makaran	ns
	AUTOMATIC ACCESS PARAMETER						
tADHAR	ADS LOW hold from RASIN HIGH	3/7	0		0		ns
tBSR	Bank select setup to RASIN LOW (ADS = HIGH)	6/12	10		10		ns
tBSH	Bank select hold from RASIN HIGH (ADS = HIGH)	3/9	10	-5-5-4	10		ns
†ASRL	Address setup to RASIN LOW (ADS = HIGH) (tASRL = td2 max to guarantee tASR)	6/4	30	qhiO	30		ns
tAUS	AUTO setup to RASIN LOW	6/5	0		0		ns
†RFSR	RFSH HIGH setup to RASIN LOW (to guarantee tASR)	6/6	10	эру	10		ns
tSSR	Address strobe HIGH to RASIN LOW (B0, B1 STABLE)	6/7	20		20		ns
tCASR	CASIN0-1 setup to RASIN LOW	6/8	-30	- 1	-30		ns
tAUH	AUTO hold from RASIN HIGH	6/9	50	1	50		ns
tAUCH	AUTO LOW hold from CASIN HIGH	6/10	0	-	0		ns
	REFRESH PARAMETER			1			
†AUHRF	AUTO LOW hold from RFSH HIGH (R/C LOW)	7/1	10	1	10		ns
†RCSRF	R/C HIGH setup to RFSH LOW (AUTO HIGH)	7/2	20	A	20		ns
†AUSRF	AUTO LOW setup to RFSH LOW (R/C LOW)	7/3	20	1	20		ns
RCHRF	R/C HIGH hold from RFSH HIGH (AUTO HIGH)	7/4	10		10		ns
^t RFH	RASIN HIGH during refresh	7/10	30		30		ns
tRFQS	RFSH LOW setup to RASIN LOW (to guarantee tRFS)	7/14	30		30		ns

+15.0 +7.5 -7.5 -15.0 -300 -300 -100 0 100 300 500 ΔC-pF

673102 Test Loads (See Note)



Note: Input pulse 0 V to 3.0 V, t_R = t_F = 2.5 ns, f = 1 MHz, t_{PW} = 200 ns. Input reference point on AC measurements is 1.5 V.

Output reference points are 2.4 V for HIGH and 0.8 V for LOW.

Change in Propagation Delays vs. Change in Loading
Capacitance Relative to the Specified Load

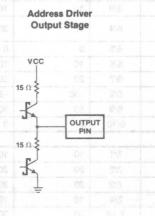
Address Outputs

TEST	S1	S2	CL	MEASURED AT
t _{PD}	Open	Closed	500 pF	0.8 V, 2.4 V
^t PZH	Closed	Closed	500 pF	2.4 V
t _{PHZ}	Open	Closed	15 pF	V _{OH} -0.5 V
tpzL	Closed	Closed	500 pF	0.8 V
t _{PLZ}	Closed	Open	15 pF	V _{OL} +0.5 V

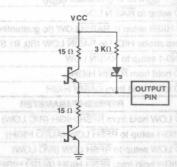
Control Outputs

TEST	S1	S2	CL	MEASURED AT			
^t PD	Open	Closed	or CLH	0.8 V, 2.4 V			
^t PZH	Open	Closed	S CLI	2.4 V			
^t PHZ	Open	Closed	15 pF	VOH -0.5 V			
tPZL	Open	Open	CL	0.8 V			
t _{PLZ}	Open	Open	15 pF	V _{OL} +0.5 V			

Where CL = 150 pF for RAS, 300 pF for CAS, and 500 pF for WE.







9

Applications

Microprocessor Interface

The 673102 Dynamic RAM Controller provides the address and control signals required to access and refresh dynamic RAMs. When interfaced to a 16-bit microprocessor, some external logic is required to generate a refresh clock as well as to perform access/refresh arbitration and interface handshake functions. Two PAL® devices may be used to perform these functions, as

shown in Figure 1. One PAL device is used to generate the refresh clock, while the other performs all arbitration and handshake functions. A hidden refresh (refresh which is transparent to the system) scheme is implemented in the interface PAL device which takes advantage of "free" system time to refresh the memory, and falls back to "forced" refresh when hidden refresh cannot be performed.

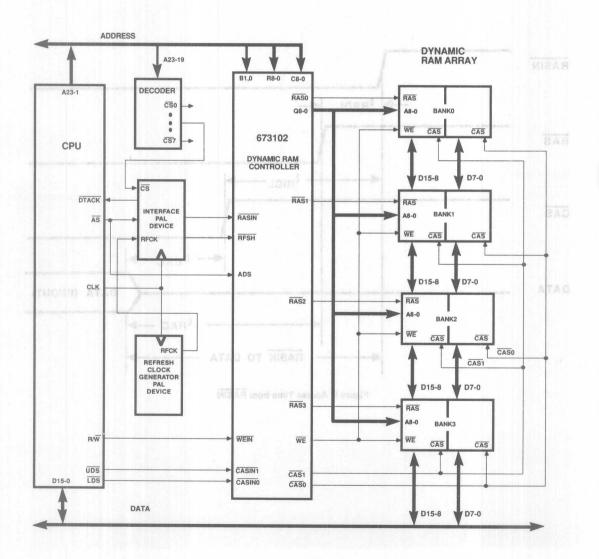
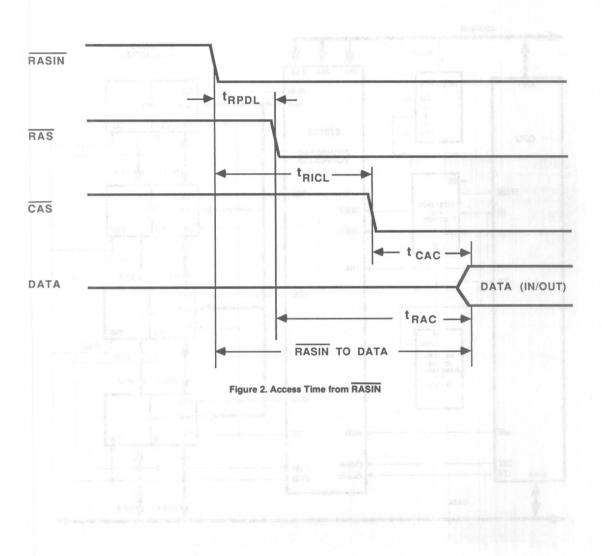


Figure 1. A CPU Interfaced to the 673102 Driving 2 M Bytes of Dynamic Memory

Determining System Performance (Auto-Access)

When determining system performance the dynamic RAM parameters must be considered as well as the controller's propagation delays. For both read and write cycles the access time for the dynamic RAM is trace (Data access time from RAS going LOW) or trace (Data access time from CAS going LOW), which-

ever results in the later appearance of Data at the dynamic RAM output. Since the RAS and CAS coming out of the controller are initiated by the RASIN, the controller-memory performance is measured from the RASIN HIGH-to-LOW transition (See Figure 2).



The time from RASIN to data is calculated to be the longer of:

tricl + tcac (RASIN to CAS + CAS to data)

t_{RPDL} + t_{RAC} (RASIN to RAS + RAS to data)

Table 1 illustrates the access times from $\overline{\text{RASIN}}$ achieved for various dynamic RAM speeds.

	PARAMETER						
CONTROLLER/MEMORY	tRAC	tRPDL	tCAC	tRICL	ACCESS TIME FROM RASIN		
673102/HM256-12	120	20	60	85	145		
673102A/HM256-12	120	20	60	75	140		
673102/HM256-15	150	20	75	85	170		
673102A/HM256-15	150	20	75	75	170		
673102/MB8265A-10	100	20	50	85	135		
673102A/MB8265A-10	100	20	50	75	125		
673102/MB8265A-12	120	20	60	85	145		
673102A/MB8265A-12	120	20	60	75	140		
673102/IMS2620-10	100	20	60	85	145		
673102A/IMS2620-10	100	20	60	75	135		
673102/IMS2620-12	120	20	70	85	155		
673102A/IMS2620-12	120	20	70	75	145		

Table 1. Access Times from RASIN for Various Memory Speeds

673102 Parameters

tRPDL - RASIN LOW to RAS LOW delay

tRICL - RASIN TO CAS LOW delay

DRAM Parameters

 $t_{\mbox{RAC}}$ — Access time from $\overline{\mbox{RAS}}$ LOW

 $t_{\mbox{CAC}}$ — Access time from $\overline{\mbox{CAS}}$ LOW

Using the Externally Controlled Access

In the Externally Controlled Access mode RASIN controls the selected RAS output, and the CASINO, 1 inputs control CASO, 1 outputs respectively. The R/C input controls the address multiplexer. The system designer may create, using the RASIN, CASIN and R/C inputs, the required control signal sequence for the specific system being designed. Special dynamic RAM access

modes such as Nibble mode, Page mode, and static column mode access cycles may be performed simply by toggling the appropriate control inputs. Special skew timing specifications have been specified to allow tighter timing control as outlined in the following examples. Both following examples relate to the scheme depicted in Figure 3.

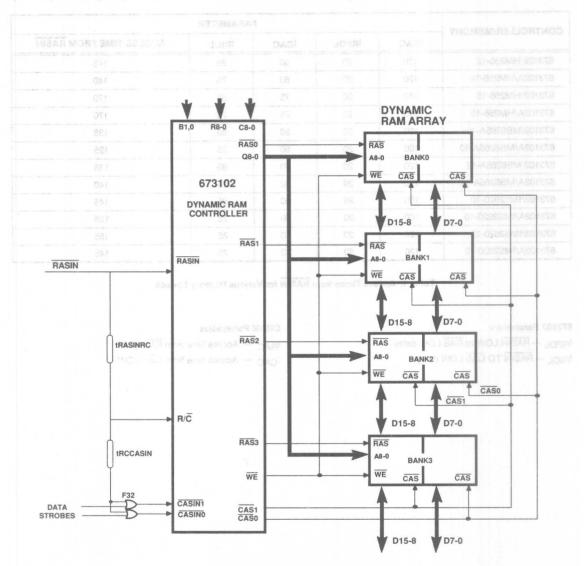


Figure 3. The 673102 in the Externally-Controlled Access Mode

9

Externally Controlled Access (ECA) (Continued)

Example 1: Computing RASIN to R/C Delay

The delay between $\overline{\text{RASIN}}$ going LOW to $\overline{\text{R/C}}$ going LOW (translation) which is required in order to satisfy the dynamic RAMs' row address hold time (translation) is computed as follows:

tRASINRC = t_{RAH}(min) + t_{d7}
Where:

t_{RAH}(min) — Row address hold time (dynamic RAM parameter)

td7(max) = tRPDL-tRHA

tRPDL - RASIN to RAS LOW delay

t_{RHA} — Row address held valid from R/C LOW

The state of the second

Example 2: Computing R/C to CASIN Delay

The delay between R/C going LOW and CASIN going LOW (tRCCASIN) which is required in order to satisfy the dynamic RAMs' column address setup (tASC) is computed as follows:

tRCCASIN = tASC(min) + td8 + tpDF32(max)

Where:

t_{ASC}(min) — Column address setup (dynamic RAM parameter)

td8(max) = tRCC-tCPDL

t_{BCC} — R/C low to column address valid

tCPDL - CASIN to CAS LOW delay

t_{PD}F32(max) — Propagation delay of the OR gate used to validate CASIN

Better system performance may be achieved using the t_{d7}, t_{d8}

switching parameters to calculate trasing and traccasin than when using the tRPDL, tRCDL, tRCC and tRHA parameters (see td7, td8 in Externally Controlled Access switching parameters). An Auto-Access more with extended CAS can RASIN R/C TRASINEC CASIN TRCCASIN TRPDL RAS TRAH -tRHA Q0-Q8 -tCPDL TASC CAS RASIN TO CAS * Indicates Dynamic RAM parameters.

Figure 4. Externally Controlled Access Timing

1-Megabit Dynamic RAM Controller/Driver

673103 673103A

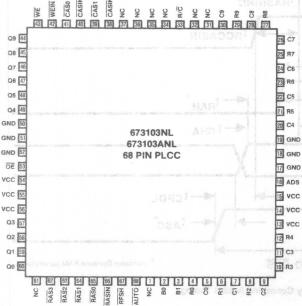
52 AUTO

Features/Benefits

- Supports up to 1 M DRAMs
- Capable of addressing up to 8 M 16-bit words or 8 M bytes
- On-chip capacitive-load drivers capable of driving up to 88 DRAMs with 30-nsec typical address propagation delay and 128 DRAMs with 35-nsec typical address propagation delay
- RASIN to RAS delay of 20 nsec max (RAS driving 22 DRAMs)
- Max and Min skews are specified to simplify system design
- Two CASIN inputs and two CAS outputs simplify byte addressing
- An Auto-Access mode with extended CAS capability takes advantage of full performance of 120 and 150 nsec DRAMs
- An output series resistor reduces undershoot

Modes of Operation

- Refresh
- Auto Access (AA)
- Externally Controlled Access (ECA)

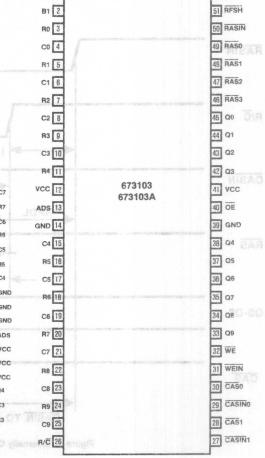


Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE		
673103	FOD CONU COND	Com		
673103A	52D, 68NL, 68NP			

Pin Configurations

B0 1



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TWX: 910-338-2376 2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2374

Switching Characteristics (Continued)

SYMBOL	AUTO ACCESS PARAMETER	FIGURE/ NUMBER	673103A MIN TYP MAX		673103 MIN TYP MAX		UNIT
†RICL	RASIN to CAS LOW delay			75	85		ns
tRCDL	RAS to CAS LOW delay	6/23	30	65	30	75	ns
tRPDL	RASIN to RAS LOW delay	6/13		20		20	ns
tredh	RASIN to RAS HIGH delay	6/14		31		31	ns
t _{APD}	Address input to output delay	6/16		50		50	ns
twppl	WEIN to WE LOW delay	91-1-		45		45	ns
twpdh	WEIN to WE HIGH delay	1252		40		40	ns
tCPDH	CASIN to CAS HIGH delay	6/22		40		40	ns
t _{RAH}	Row address hold time from RAS LOW	6/17	15	- UD	15		ns
t _{d2}	(Address input to output delay)-(RASIN to RAS LOW delay)	(9)	(0)	30		30	ns
tSPD	ADS HIGH to address output valid	6/19		55		55	ns
tASC	Column address setup to CAS LOW	6/21	0	dista dista	0	5	ns
tCAHC	Column address remaining valid from CASINO-1 HIGH	6/18	5	or. or.	5		ns
t _{ASR}	Row address valid before RAS LOW	6/24	0	how sow	0		ns
t _{d5}	(RASIN to RAS HIGH delay)-(RASIN to RAS LOW delay)	(9)	-7	13	-7	13	ns
	REFRESH PARAMETER	1					
†RFLCT	RFSH LOW to refresh address valid (AUTO LOW or R/C HIGH)	7/5	5	40		40	ns
tRFPDL	RASIN LOW to RAS LOW delay during refresh	7/11		23		23	ns
^t RFPDH	RASIN HIGH to RAS HIGH delay during refresh	7/12	-	38		38	ns
†RFAH	Refresh address held from RASIN HIGH (RFSH LOW)	7/7	0		0		ns
†RHNC	RASIN HIGH to new refresh address valid	7/9		66		66	ns
treals	Refresh address held from RFSH HIGH	7/6	0		0	Wilelan	ns
^t RFS	Refresh address valid to RAS LOW (provided tRFQS is satisfied)	7/13	0		0		ns
^t RFRDH	RFSH HIGH to RAS HIGH (for 3 banks, RASIN = LOW)	7/15		40		40	ns
t _d 9	(RASIN to RAS HIGH delay)-(RASIN to RAS LOW delay)		-9	16	-9	16	ns
	THREE-STATE PARAMETER						
t _{AZL}	OE LOW to address output LOW	10/1		45		45	ns
^t AZH	OE LOW to address output HIGH	10/2		60		60	ns
^t ALZ	OE HIGH to address output HI-Z from LOW	10/3		35		35	ns
^t AHZ	OE HIGH to address output HI-Z from HIGH	10/4		25		25	ns
tCTZL	OE LOW to control output LOW	10/5		40		40	ns
tCTZH	OE LOW to control output HIGH	10/6		50		50	ns
tCTLZ	OE HIGH to control output HI-Z from LOW	10/7		30		30	ns
tCTHZ	OE HIGH to control output HI-Z from HIGH	10/8		25		25	ns

Note 1: These are absolute voltage levels with respect to the ground pins on the device and includes all overshoots due to system or tester noise.

Do not attempt to test these values without suitable equipment.

Note 2: This test is provided as a monitor of driver output source and sink current capability. Caution should be exercised in testing this parameter.

One output should be tested at a time and test duration should not exceed one second.

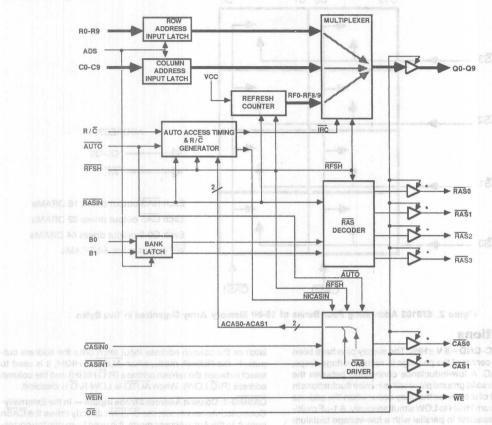
Note 3: Output load capacitance is typical for four banks of 22 DRAMs with trace capacitance.

The values are: Q0-8 C_L = 500 pF, RAS0-3 C_L = 150 pF, WE C_L = 500 pF, CAS0-1 C_L = 300 pF.

							. =	0							
			83	83	No.	2	CASIN1	CASINO	WEIN	WE					
			0		Z	Z	10	10	>	16					
	R8			R9	NC	S I	NC	CAST	CASO		NC				
			(19)			27) ((31)	_	(34)	[
CASIN to CAS HIGH		(a)	_	_		_									
The blod essential work	nate	10.00	(18)	(20)	(22)	26) (28)	30	32			Ø8			
R7			(15)			0400	VB C			38 37	Q7	Q6			
R6 of Heith ada	C5	(14)	13 (Т	3103 EGAE				40 39	Q5	Q4			
Column address s 68	C4	12	11)			MIC				42 41	GND	GND			
GND selebbs arrulo()	GND	10	9			ROL				(44) (43)	GND	OE			
GND lay assistos woR	ADS	(8)	7)			P VIE				(46) (45)	vcc	vcc			
VCC (EATION MEAN)	vcc	6	(5) ((48) (47)	vcc	Q3			
VCC	R4	(4)		0						50 (49)	Q2	Q1		-	
C3 Sing WOJ OTUA)	Senha	Laborator in	_	66	2) 64	60 ((58)	56	(54)	51 52	Q2	് വ			
RASIN LOW to TAS I	. WO.	elay d	68	67	3 65	61) (59	57	(55)	53					
	R3	Velsh	ากษุย (5	8	NC	馬	RASO	RAS2	51					
Refresh address haid					Har		RFSH	RA	RA		NC				
			3	72	5 25	B0	AUTO	RASIN	RAST	RAS3					
							A	RA	15	12					
3867															
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	i tuqiu														

Monolithic IIII Memories

Block Diagram



* Indicates that there is a 3-K(!) pull-up resistor on these outputs when they are disabled a ballocal document

Figure 1. 673103 Functional Block Diagram

Description

The 673103 is an LSI device, provided in 52-pin and 68-pin packages, which performs most of the functions needed to control and address Dynamic RAMs. Twenty-two address inputs, ten address outputs, four RAS outputs, and two CASIN-CAS input-output pairs allow the 673103 to directly address 8 M 16-bit words or bytes. The CASINn inputs and the CASn outputs simplify individual byte access in 16-bit wide memory arrays (see Figure 2).

The 673103 has three operating modes:

- Externally Controlled Access (ECA)
- Auto Access (AA)
- · Refresh (RFSH).

The Externally-Controlled-Access mode gives the system direct control over the RASm outputs, the CASn outputs, and Row/Column multiplexing. It also supports PAGE mode access, NIBBLE mode access, and static column mode access.

The Auto-Access mode provides on-chip delays that automatically control the timing delays between RASm signals, address multiplexing, and CASn signals. In the Auto-Access mode CASIN0-1 inputs serve as enables for the respective CAS0-1

outputs, allowing the access of any byte of the memory array (for 16-bit wide memory arrays organized in two bytes). In this mode CASO-1 outputs go HIGH only when the respective CASINO-1 inputs go HIGH, and the address switches back to row address only when both CASINO-1 go HIGH. This feature allows extension of the CAS LOW time, and column address time while RASIN and RASm can go HIGH to satisfy the precharge requirements of the dynamic RAMs.

When the Refresh mode is selected (RFSH is LOW) an on-chip refresh counter provides the refresh address; with AUTO HIGH and R/C LOW the column address is forced onto the address output multiplexer, facilitating an access of a particular memory location while refreshing a row. This feature may be useful when implementing error detection and correction scrubbing.

The 673103 can drive eight banks of DRAMs. RASm control signals are used to select a pair of banks, while leaving the other banks in standby. The two CASn outputs enable the selection of one bank out of two. The address lines and the WE signal can be connected to all eight banks. In a 16-bit wide, byte-oriented, memory array the RASm signals select the banks while the CASn signals select the bytes, as shown in Figure 2.

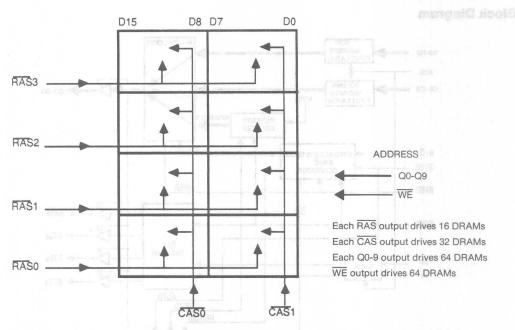


Figure 2. 673103 Addressing Four Banks of 16-bit Memory Array Organized in Two Bytes

Pin Definitions

VCC, GND: VCC-GND = 5 V \pm 10%. The supply pins have been assigned to the center of the package to reduce voltage drops, both DC and AC. A low-inductance connection between the ground pin and a solid ground plane will minimize fluctuations in the ground level of the device that may occur when the address outputs switch from HIGH to LOW simultaneously. A 1- μ F multilayer ceramic capacitor in parallel with a low-voltage tantalum capacitor, both connected close to the VCC and GND pins, will properly decouple the device.

R0-R9: Row Address Inputs

C0-C9: Column Address Inputs

B0-B1: Bank-Pair Select Inputs — Strobed by ADS. Decoded to enable one of the RAS outputs when RASIN goes LOW in the access modes

Q0-Q9: Multiplexed Address Outputs — Selected from the row address input latch, the column address input latch, or the refresh counter.

RASIN: Row Address Strobe Input — Drives the selected RASm output in the access modes, and all RAS outputs in the Refresh mode

ADS: Address (Latch) Strobe Input — Strobes input row address, column address, and Bank Select inputs into the respective latches when HIGH; latches on HIGH-to-LOW transition.

OE: Output Enable — When \overline{OE} is LOW the address and control outputs are enabled. When \overline{OE} is HIGH the address outputs are in high-impedance and the control outputs are pulled HIGH.

R/C: Row/Column Select Input — In the Externally-Controlled-Access mode, it is used to select either the row address input latch or the column address input latch onto the address outputs. In the Refresh mode, when $\overline{\text{AUTO}}$ is HIGH, it is used to select between the refresh address (R/ $\overline{\text{C}}$ HIGH) and the column address (R/ $\overline{\text{C}}$ LOW). When $\overline{\text{AUTO}}$ is LOW R/ $\overline{\text{C}}$ is disabled.

CASINO-1: Column Address Strobe Inputs — In the Externally-Controlled-Access mode, the CASINn directly drives the CASn output. In the Auto-Access mode, it is used to enable the corresponding CASn output (See CAS0-1 description).

WEIN: Write Enable Input.

WE: Write Enable Output.

CAS0-1: Column Address Strobe Outputs — In the Externally-Controlled-Access mode the CAS outputs follow the CASIN inputs. In the Auto-Access mode the CASIN inputs are used to enable the CAS outputs. The CAS outputs are asserted LOW, with proper delay from the RAS output, by the RASIN signal via the Auto-Access timing generator. In the Auto-Access mode, the CASn goes HIGH only when the corresponding CASINn goes HIGH. Extending the CASn LOW duration while RASIN and RASm go HIGH to satisfy precharge requirements of the dynamic RAMs.

RAS0-3: Row Address Strobe Outputs — When RFSH is HIGH the selected row address strobe output (decoded from signals B0, B1) follows the RASIN input. When RFSH is LOW all RAS outputs go LOW together following RASIN going LOW.

AUTO: Auto-Access Input — When AUTO is LOW and RFSH is HIGH the Auto-Access mode is selected (see Auto-Access mode description).

RFSH: Refresh Input — When RFSH is LOW the Refresh mode is selected (see Refresh mode description).

Externally-Controlled-Access Mode (ECA)

In this mode, selected when $\overline{\text{AUTO}}$ and $\overline{\text{RFSH}}$ are held HIGH, the 673103 serves as a straightforward multiplexer and driver for the address and control signals to the DRAMs. The $\overline{\text{RAS}}$ m output selected by the B0 and B1 inputs follows the $\overline{\text{RAS}}$ IN input, and each of the $\overline{\text{CAS}}$ outputs follows its corresponding $\overline{\text{CAS}}$ IN input. When $\overline{\text{R/C}}$ is HIGH the row address is enabled onto the Q0-9 outputs. When $\overline{\text{R/C}}$ is LOW the column address latch is enabled onto Q0-9 outputs.

The RASIN — RAS, CASIN — CAS, and R/C — Q0-9 control paths are independent to allow the system designer maximum flexibility and support of special DRAM access and refresh modes such as NIBBLE mode, PAGE mode, CAS before RAS, etc.

To allow tighter timing of the sequence of control signals to the Dynamic RAM, several difference timing parameters have been specified for the Externally Controlled Access mode. These

parameters specify the maximum difference between the various "control channels" of the device. In particular, using switching characteristics t_{d7} and t_{d8} is very useful when designing the delay from \overline{RASIN} going LOW to R/\overline{C} and the delay between R/\overline{C} going LOW to \overline{CASIN} going LOW (see Applications).

BANK SELECT (STR	ENABLED RASh	
B1	В0	ENABLED HASI
0	0	RAS0
0	1	RAS1
1	0	RAS2
1.1090 ^f	1	RAS3

Table 1. Memory Bank Decode

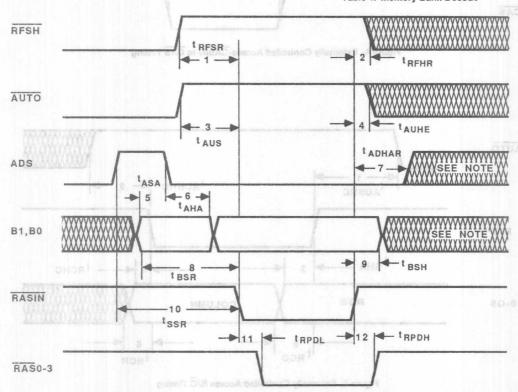


Figure 3. Externally Controlled Access-RASIN-to-RAS Timing

Note: To prevent glitches on the RAS0-3 outputs, operating conditions tBSH or tADHAR must be satisfied.

9

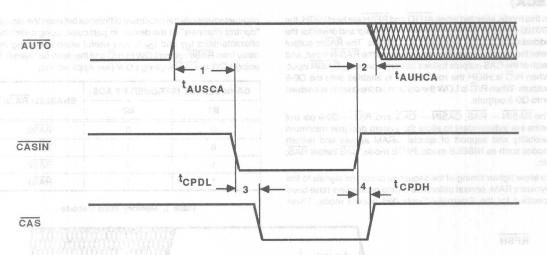


Figure 4. Externally Controlled Access-CASIN to CAS Timing

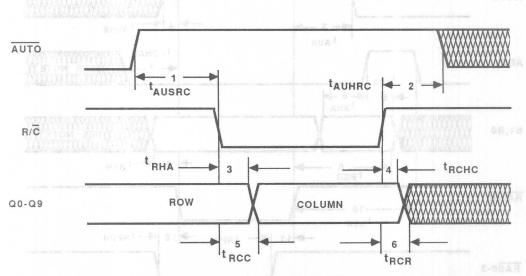


Figure 5. Externally Controlled Access R/C Timing

Note: t_{RCC} will be met only if the column address is available t_{APD} before it appears on Q0-9 outputs or if it is latched by ADS.

9

Auto-Access Mode (AA)

In the Auto-Access mode the 673103 provides the system designer with built-in delays and sequencing to accommodate DRAMs with 150 nanoseconds and faster access time. The Auto-Access mode is selected when AUTO is held LOW and RFSH pin is held HIGH. The R/C input is disabled, and RASIN goes LOW initiating the sequence of control signals to access the DRAMs. The CASINO-1 inputs are used as enables for the respective CAS outputs. A LOW on a CASIN in input enables the

CASn output to be driven LOW with the internally-generated delay from RAS. Each CASn output goes HIGH only when the corresponding CASINn input goes HIGH, and the address switches back to row address only when all CASIN go HIGH. This feature allows extension of the CAS LOW time and the column address time, while RASIN and RASm can go HIGH to satisfy precharge requirements of the dynamic RAMs. The R/C input is disabled in this mode.

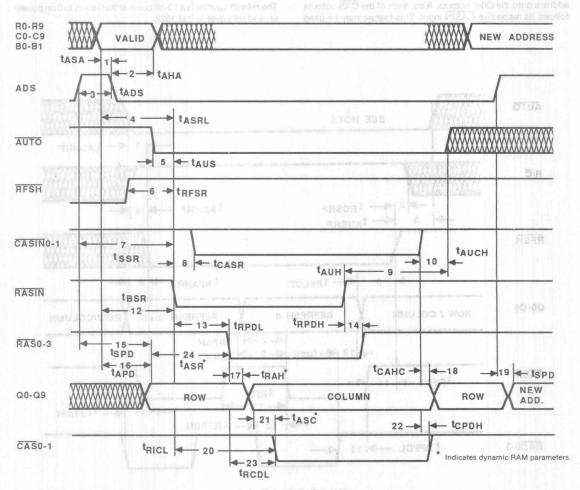


Figure 6. Auto-Access (AA) Timing

Refresh Mode (RFSH)

When $\overline{\text{RFSH}}$ is held LOW the refresh counter contents are enabled onto the Q0-9 address outputs, provided either R/\overline{C} is held HIGH, or $\overline{\text{AUTO}}$ is held LOW, or both conditions exist. In this mode all four $\overline{\text{RAS}}$ outputs follow the $\overline{\text{RASIN}}$ input signal. The refresh counter increments the refresh address when either $\overline{\text{RASIN}}$ or $\overline{\text{RFSH}}$ goes HIGH while the other is LOW. When $\overline{\text{AUTO}}$ is LOW the $\overline{\text{CASIN0-1}}$ inputs are isolated and $\overline{\text{CAS0-1}}$ are held HIGH. Also, when $\overline{\text{AUTO}}$ is LOW the R/\overline{C} input is isolated from the output multiplexer, and the refresh address appears at the Q0-9 outputs.

When $\overline{\text{AUTO}}$ is HIGH, pulling $\overline{\text{R/C}}$ LOW enables the column address onto the Q0-9 outputs. Also, each of the $\overline{\text{CAS}}$ outputs follows its respective $\overline{\text{CASIN}}$ input. This feature may be used

when implementing error correction and detection "scrubbing" for two-bank memory arrays. "Scrubbing" is a term describing a cyclic error correction of soft errors in the memory array, done within the refresh cycles. On every refresh cycle one location of the memory array is accessed, and the data in that location goes, if necessary, through a correction cycle (a read-modify-write memory cycle). The 673103 provides the facilities to force a column address onto the Q0-9 address outputs and to assert the CASO-1 outputs within a refresh cycle to allow scrubbing. A column counter and a bank counter need to be added externally to provide the column address for scrubbing.

The refresh counter is a 10-bit counter that resets to 0 on powerup and rolls over to 0 at 1023.

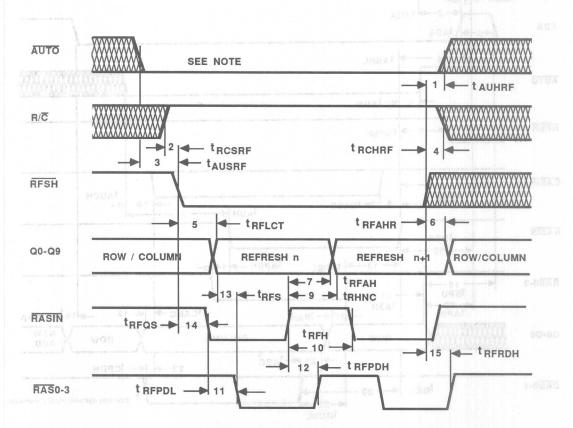


Figure 7. Refresh Timing

Note: In the REFRESH mode, AUTO must be LOW or R/C must be HIGH to guarantee the refresh address on the Q0-8 outputs.



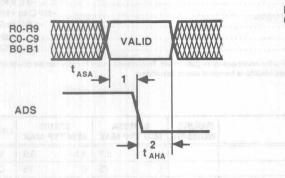


Figure 8. Address Setup and Hold Time to ADS

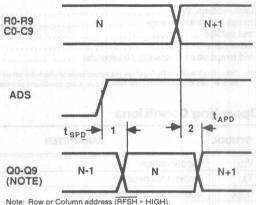
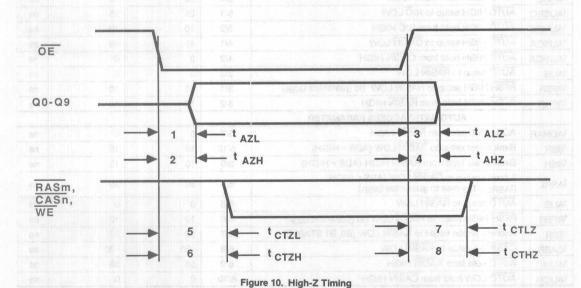


Figure 9. Address Input/Output Propagation Delay



Monolithic III Memories

Absolute Maximum Ratings (See Note)

Supply voltage, VCC	0.5 V to 7 V
Storage temperature range	65°C to +150°C
Input voltage	1.5 V to 5.5 V
Output current	150 mA
Lead temperature (soldering, 10 seconds)	300° C

Note: "Absolute Maximum Ratings" are the values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of operating conditions provides conditions for actual device operation.

Operating Conditions

SYMBOL	PARAMETER	FIGURE/ NUMBER	673103A MIN TYP MAX	673103 MIN TYP MAX	UNIT
Vcc	Supply voltage		4.5 5.5	4.5 5.5	V
TA	Ambient temperature		0 75	0 75	С
tASA	Address setup time to ADS LOW	8/1	18	18	ns
tADS	Address strobe pulse width HIGH		26	26	ns
tAHA	Address hold time from ADS LOW	8/2	10.11	3 10 blad if equal	ns
7 11 10 11 11 11 11	EXTERNALLY CONTROLLED ACCESS PARAMETER				
†ADHAR	ADS LOW hold from RASIN HIGH	3/7	0	0	ns
tBSR	Bank select setup to RASIN LOW (ADS = HIGH)	3/8	10	10	ns
tBSH	Bank select hold from RASIN HIGH (ADS = HIGH)	3/9	10	10	ns
tssr	Address strobe HIGH setup to RASIN LOW (B0, B1 STABLE)	3/10	20	20	ns
†AUHE	AUTO hold from RASIN HIGH	3/4	55	55	ns
tAUSRC	AUTO HIGH setup to R/C LOW	5/1	25	25	ns
tAUHRC	AUTO HIGH hold from R/C HIGH	5/2	10	10	ns
tAUSCA	AUTO HIGH setup to CASIN LOW	4/1	45	45	ns
tAUHCA	AUTO HIGH hold from CASIN HIGH	4/2	0	0	ns
taus	AUTO setup to RASIN LOW	3/3	0	0	ns
tRFSR	RFSH HIGH setup to RASIN LOW (to guarantee tASR)	3/1	10	10	ns
tRFHR	RFSH HIGH hold from RASIN HIGH	3/2	10	10 80	ns
	AUTOMATIC ACCESS PARAMETER				
t _{ADHAR}	ADS LOW hold from RASIN HIGH	3/7	0	0	ns
tBSR	Bank select setup to RASIN LOW (ADS = HIGH)	6/12	10	10	ns
tBSH	Bank select hold from RASIN HIGH (ADS = HIGH)	3/9	10	10	ns
†ASRL	Address setup to RASIN LOW (ADS = HIGH) (tASRL = t _{d2} max to guarantee t _{ASR})	6/4	30	30 018	ns
taus	AUTO setup to RASIN LOW	6/5	0	0	ns
tRFSR	RFSH HIGH setup to RASIN LOW (to guarantee tASR)	6/6	10	10	ns
tssr	Address strobe HIGH to RASIN LOW (B0, B1 STABLE)	6/7	20	20	ns
tCASR	CASIN0-1 setup to RASIN LOW	6/8	-30	-30	ns
tAUH	AUTO hold from RASIN HIGH	6/9	50	50	ns
^t AUCH	AUTO LOW hold from CASIN HIGH	6/10	0	0	ns
	REFRESH PARAMETER		La Ri		
^t AUHRF	AUTO LOW hold from RFSH HIGH (R/C LOW)	7/1	10	10	ns
^t RCSRF	R/C HIGH setup to RFSH LOW (AUTO HIGH)	7/2	20	20	ns
†AUSRF	AUTO LOW setup to RFSH LOW (R/C LOW)	7/3	20	20	ns
^t RCHRF	R/C HIGH hold from RFSH HIGH (AUTO HIGH)	7/4	10	10	ns
^t RFH	RASIN HIGH during refresh	7/10	30	30	ns
tRFQS	RFSH LOW setup to RASIN LOW (to guarantee tRFS)	7/14	30	30	ns

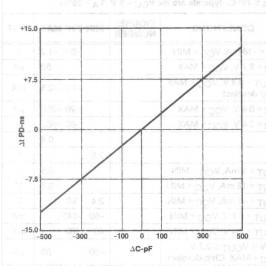
Electrical Characteristics V_{CC} = 5 V ±10%, 0°C ≤ T_A ≤ 75°C. Typicals are for V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	CONDITIONS	FIGURE/ NUMBER	MIN TYP MAX	UNIT
VIC	Input clamp voltage	I _{IN} = -18 mA, V _{CC} = MIN		-0.8 -1.2	V
IH	Input high current	V _{IN} = 2.7 V, V _{CC} = MAX		50	μΑ
ICTL	Output load current for RAS, CAS, WE	VOUT = 0.4 V, VCC = MAX Chip deselect		-1.5 -2.5	mA
IIL	Input low current except for RFSH	V _{IN} = 0.4 V, V _{CC} = MAX		-20 -250	μΑ
ILRF	Input low current for RFSH	V _{IN} = 0.4 V, V _{CC} = MAX		-80 -500	μΑ
VIL	Input low threshold (Note 1)			0.8	V
VIH	Input high threshold (Note 1)			2.0	V
V _{OL1}	Output low voltage	IOUT = 1 mA, VCC = MIN		0.5	V
V _{OL2}	Output low voltage	IOUT = 12 mA, VCC = MIN		0.8	V
VOH	Output high voltage	IOUT = -1 mA, VCC = MIN		2.4 3.0	V
ЮН	Output source current (Note 2)	VOUT = 0.8 V, VCC = MIN		-50 -140	mA
OL	Output sink current (Note 2)	VOUT = 2.4 V, VCC = MIN	0 (0)	40 100	mA
loz	Three-state output current (address output)	$0.4 \text{ V} \le \text{V}_{OUT} \le 2.7 \text{ V}$ V _{CC} = MAX, Chip deselect	19-04	-50 50	μА
Icc	Supply current	VCC = MAX	er avefaC a	170 260	mA
CIN	Input capacitance	TA = 25°C has it to thoo ?			pF

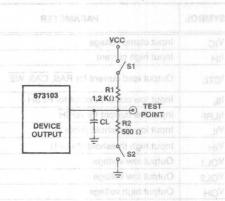
Switching Characteristics (See Note 3)

SYMBOL	EXTERNALLY CONTROLLED ACCESS PARAMETER	FIGURE/ NUMBER	67310 MIN TYP	- 3.F DID WIT	673103 MIN TYP MAX	UNIT
tRHA	Row addresses remaining valid from R/C LOW	5/3	0		0	ns
tRPDL	RASIN to RAS LOW delay	3/11	110.01	20	20	ns
tRPDH.	RASIN to RAS HIGH delay	3/12		31	31	ns
tAPD	Address input to output delay	9/2		50	50	ns
tWPDL	WEIN to WE LOW delay			45	45	ns
tWPDH	WEIN to WE HIGH delay		savisC som	40	40	ns
tCPDL	CASIN to CAS LOW delay	4/3	allers mil	28	28	ns
tCPDH	CASIN to CAS HIGH delay	4/4		40	40	ns
tRCC	Column select to column address valid	5/5		41	41	ns
tRCR	Row select to row address valid	5/6		45	45	ns
t _{d1}	(CASIN to CAS LOW delay)-(RASIN to RAS LOW delay)		-2	13	-2 13	ns
t _{d2}	(Address input to output delay)-(RASIN to RAS LOW delay)			30	30	ns
t _{d3}	(Address input to output delay)-(CASIN to CAS LOW delay)	The state of the s	-5	23	-5 23	ns
t _{d4}	Skew between address output lines	1		10	10	ns
t _{d5}	(RASIN to RAS HIGH delay)-(RASIN to RAS LOW delay)		-7	13	-7 13	ns
t _{d6}	(CASIN to CAS HIGH delay)-(CASIN to CAS LOW delay)		-12	12	-12 12	ns
tSPD	ADS HIGH to address output valid	9/1	FIG.	55	55	ns
tRCHC	Column addresses remaining valid from R/C HIGH	5/4	0		0	ns
t _{d7}	tRPDL - tRHA			13	13	ns
t _{d8}	tRCC - tCPDL			20	20	ns

673103 Test Loads (See Note)



Change in Propagation Delays vs. Change in Loading Capacitance Relative to the Specified Load



Note: input pulse 0 V to 3.0 V, t_R = t_F = 2.5 ns, f = 1 MHz, t_{PW} = 200 ns. Input reference point on AC measurements is 1.5 V. Output reference points are 2.4 V for HIGH and 0.8 V for LOW.

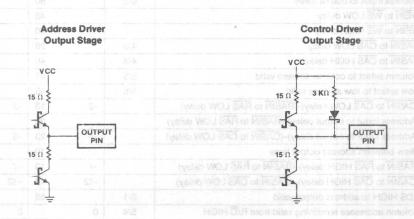
Address Outputs

TEST	S1	S2	CL	MEASURED AT
t _{PD}	Open	Closed	500 pF	0.8 V, 2.4 V
^t PZH	Closed	Closed	500 pF	2.4 V
^t PHZ	Open	Closed	15 pF	VOH -0.5 V
t _{PZL}	Ciosed	Closed	500 pF	0.8 V
[†] PLZ	Closed	Open	15 pF	V _{OL} +0.5 V

Control Outputs

TEST	S1	S2	CL	MEASURED AT
t _{PD}	Open	Closed	CL	0.8 V, 2.4 V
^t PZH	Open	Closed	CL	2.4 V
t _{PHZ}	Open	Closed	15 pF	VOH -0.5 V
t _{PZL}	Open	Open	CL	0.8 V
t _{PLZ}	Open	Open	15 pF	V _{OL} +0.5 V

Where C₁ = 150 pF for RAS, 300 pF for CAS, and 500 pF for WE.



Applications

Microprocessor Interface

The 673103 Dynamic RAM controller provides the address and control signals required to access and refresh dynamic RAMs. When interfaced to a 16-bit microprocessor, some external logic is required to generate a refresh clock as well as to perform access/refresh arbitration and interface handshake functions. Two PAL® devices may be used to perform these functions, as shown in Figure 1. One PAL device is used to generate the

refresh clock, while the other performs all arbitration and handshake functions. A hidden refresh (refresh which is transparent to the system) scheme is implemented in the interface PAL device which takes advantage of "free" system time to refresh the memory, and falls back to "forced" refresh when hidden refresh cannot be performed.

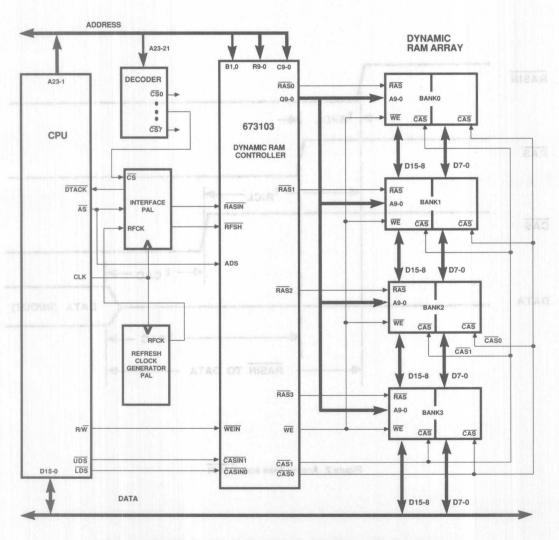
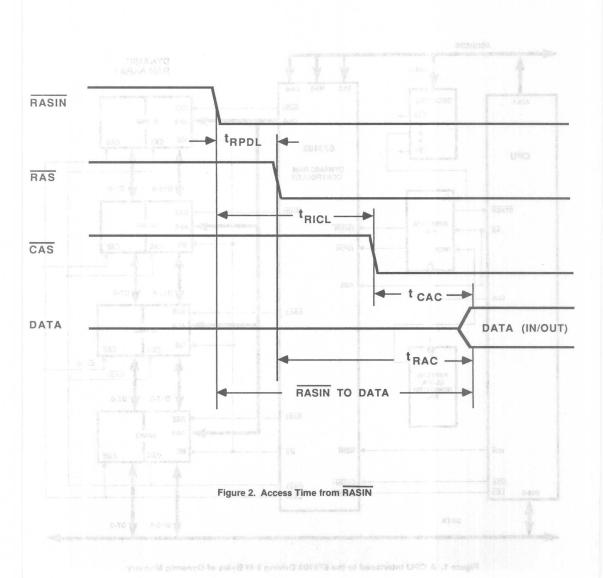


Figure 1. A CPU Interfaced to the 673103 Driving 8 M Bytes of Dynamic Memory

Determining System Performance (Auto-Access)

When determining system performance the dynamic RAM parameters must be considered as well as the controller's propagation delays. For both read and write cycles the access time for the dynamic RAM is t_{RAC} (Data access time from RAS going LOW) or t_{CAC} (Data access time from CAS going LOW), which-

ever results in the later appearance of data at the Dynamic RAM output. Since the RAS and CAS coming out of the controller are initiated by the RASIN, the controller-memory performance is measured from the RASIN HIGH-to-LOW transition (see Figure 2).





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The time from RASIN to data is calculated to be the longer of:

tricl + tcac (RASIN to CAS + CAS to data)

trend + trac (RASIN to RAS + RAS to data)

Table 1 illustrates the access times from $\overline{\text{RASIN}}$ achieved for various dynamic RAM speeds.

		PARAMETER								
CONTROLLER/MEMORY	tRAC	tRPDL	tCAC	tRICL	ACCESS TIME FROM RASIN					
673103/HM256-12	120	20	60	85	145					
673103A/HM256-12	120	20	60	75	140					
673103/HM256-15	150	20	75	85	170					
673103A/HM256-15	150	20	75	75	170					
673103/MB8265A-10	100	20	50	85	135					
673103A/MB8265A-10	100	20	50	75	125					
673103/MB8265A-12	120	20	60	85	145					
673103A/MB8265A-12	120	20	60	75	140					
673103/IMS2620-10	100	20	60	85	145					
673103A/IMS2620-10	100	20	60	75	135					
673103/IMS2620-12	120	20	70	85	155					
673103A/IMS2620-12	120	20	70	75	145					

Table 1. Access Times from RASIN for Various Memory Speeds

673103 Parameters

 $t_{RPDL} - \overline{RASIN}$ LOW to \overline{RAS} LOW delay

tRICL - RASIN TO CAS LOW delay

DRAM Parameters

trac — Access time from RAS LOW

 t_{CAC} — Access time from \overline{CAS} LOW

Using the Externally Controlled Access

In the Externally Controlled Access mode \overline{RASIN} controls the selected \overline{RAS} output, $\overline{CASIN0}$ -1 control $\overline{CAS0}$ -1 outputs respectively and $\overline{R/C}$ controls the address multiplexer. The system designer may create, using the \overline{RASIN} , \overline{CASIN} and $\overline{R/C}$ inputs, the required control signal sequence for the specific system being designed. Special dynamic RAM access modes such as

Nibble mode and Page mode access cycles may be performed simply by toggling the appropriate control inputs. Special skew timing specifications have been specified to allow tighter timing control as outlined in the following examples. Both following examples relate to the scheme depicted in Figure 3.

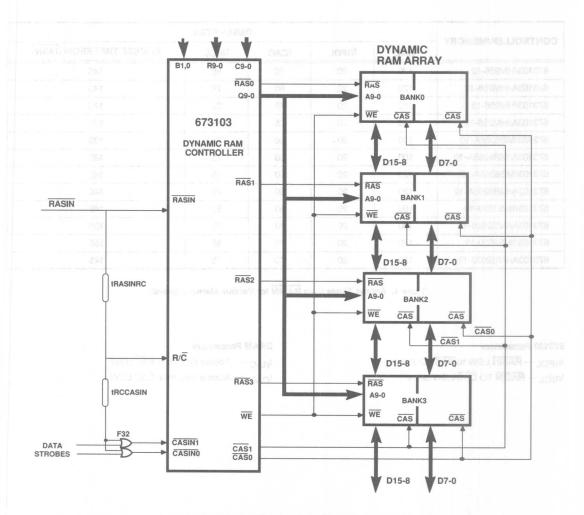


Figure 3. The 673103 in the Externally-Controlled Access Mode

Externally Controlled Access (ECA) (Continued)

Example 1: Computing RASIN to R/C Delay

The delay between RASIN going LOW to R/C going LOW (trasinro) which is required in order to satisfy the dynamic RAMs' row address hold time (tRAH) is computed as follows:

tRASINRC = tRAH(min) + td7 Where:

t_{RAH}(min) — Row address hold time (dynamic RAM parameter)

t_{d7}(max) = t_{RPDL}-t_{RHA}

t_{RPDL} — RASIN to RAS LOW delay

t_{RHA} — Row address held valid from R/C LOW

Example 2: Computing R/C to CASIN Delay

The delay between R/C going LOW to going CASIN LOW (tRCCASIN) which is required in order to satisfy the dynamic RAMs' column address setup (t_{ASC}) is computed as follows:

tRCCASIN = tASC(min) + td8 + tpDF32(max)

t_{ASC}(min) — Column address setup (dynamic RAM parameter) td8(max) = tBCC-tCPDL

t_{RCC} — R/C low to column address valid

tCPDL — CASIN to CAS LOW delay

tPDF32(max) - Propagation delay of the OR gate used to validate CASIN

Better system performance may be achieved using the td7, td8 switching parameters to calculate tRASINRC and tRCCASIN than when using the tRPDL, tRCDL, tRCC and tRHA parameters (see td7, td8 in Externally Controlled Access switching parameters).

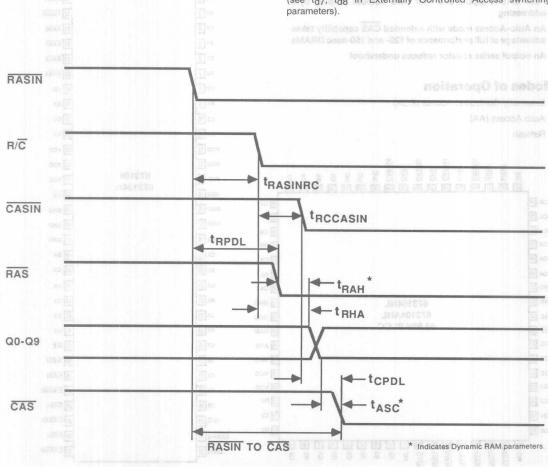


Figure 4. Externally Controlled Access Timing

1-Megabit Dynamic RAM Controller/Driver

64 AUTO

63 RFSH

62 RASIN

61 RASO

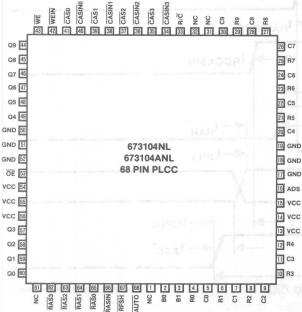
60 RAS1

Features/Benefits

- Supports up to 1 M DRAMs
- Capable of addressing up to 16 M bytes
- On-chip capacitive-load drivers capable of driving up to 88 DRAMs with 30-nsec typical address propagation delay and 128 DRAMs with 35-nsec typical address propagation delay
- RASIN to RAS delay of 23 nsec max (RAS driving 32 DRAMs)
- Max and Min skews are specified to simplify system design
- Four CASIN inputs and four CAS outputs simplify byte addressing
- An Auto-Access mode with extended CAS capability takes advantage of full performance of 120- and 150-nsec DRAMs
- An output series resistor reduces undershoot

Modes of Operation

- Externally Controlled Access (ECA)
- Auto Access (AA)
- Refresh



Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE	
673104	CAD CONIL CONID	Com	
673104A	64D, 68NL, 68NP		

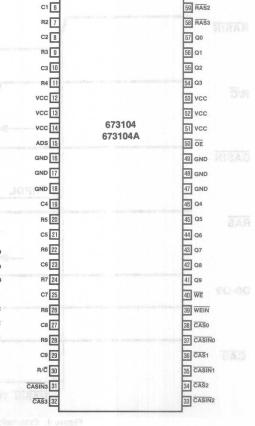
Pin Configurations

B1 2

R0 3

C0 4

R1 5

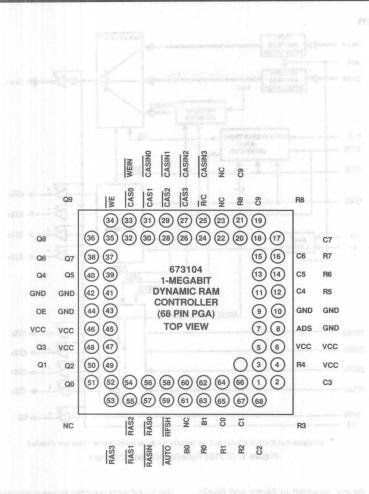


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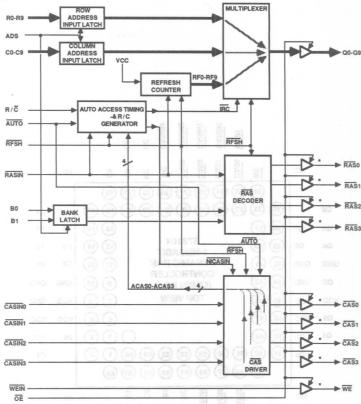
TWX: 910-338-2376

2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2374

Monolithic M Memories M



Block Diagram



* Indicates that there is a 3-K(1) pull-up resistor on these outputs when they are disabled

Figure 1. 673104 Functional Block Diagram

Description

The 673104 is an LSI device, provided in 64-pin and 68-pin packages, which performs most of the functions needed to control and address Dynamic RAMs. Twenty-two address inputs, ten address outputs, four RAS outputs, and four CASIN-CAS input-output pairs allow the 673104 to directly address 16 M bytes. The four CASINn inputs and the four CASIN outputs simplify individual byte access in 32-bit wide memory arrays (see Figure 2).

The 673104 has three operating modes:

- Externally Controlled Access (ECA)
- Auto Access (AA)
- · Refresh (RFSH).

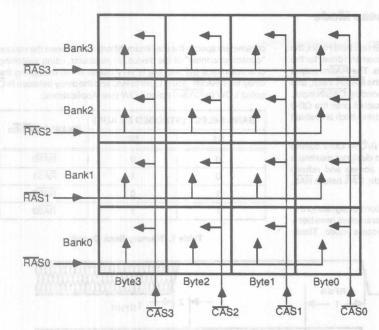
The Externally-Controlled-Access mode gives the system direct control over the RASm outputs, the CASn outputs, and Row/Column multiplexing. It also supports PAGE mode access, NIBBLE mode access and static column mode access.

The Auto-Access mode provides on-chip delays that automatically control the timing delays between RASm signals, address multiplexing, and CASn signals. In the Auto-Access mode CASIN0-3 inputs serve as enables for the respective CAS0-3 outputs, allowing the access of any byte of the memory array

(for 32-bit wide memory arrays organized in four bytes). In this mode $\overline{\text{CAS}0}$ -3 outputs go HIGH only when the respective $\overline{\text{CASIN0}}$ -3 inputs go HIGH, and the address switches back to row address only when $\overline{\text{CASIN0}}$ -3 go HIGH. This feature allows extension of the $\overline{\text{CAS}}$ LOW time and column address time while $\overline{\text{RASIN}}$ and $\overline{\text{RASm}}$ can go HIGH to satisfy the precharge requirements of the dynamic RAMs.

When the Refresh mode is selected (RFSH is LOW) an on-chip refresh counter provides the refresh address; with AUTO HIGH and R/C LOW the column address is forced onto the address output multiplexer, facilitating an access of a particular memory location while refreshing a row. This feature may be useful when implementing error detection and correction scrubbing.

The 673104 can drive sixteen banks of DRAMs. RASm control signals are used to select four banks, while leaving the other twelve banks in standby. The four CASn outputs enable the selection of one bank out of four. The address lines and the WE signal can be connected to all sixteen banks. In a 32-bit wide, byte-oriented, memory array the RASm signals select one out of four banks while the CASn signals select the bytes, as shown in Figure 2.



ADDRESS

Q0-Q9

WE

Each RAS output drives 32 DRAMs
Each CAS output drives 32 DRAMs
Each Q0-9 output drives 128 DRAMs
WE output drives 128 DRAMs

Figure 2. 673104 Addressing Four Banks of 32-bit Memory Array Organized in Four Bytes

Pin Definitions

VCC, GND: VCC-GND = 5 V ±10%. The supply pins have been assigned to the center of the package to reduce voltage drops, both DC and AC. A low inductance connection between the ground pin and a solid ground plane will minimize fluctuations in the ground level of the device that may occur when the address outputs switch from HIGH to LOW simultaneously. A 1- μ F multilayer ceramic capacitor in parallel with a low voltage tantalum capacitor, both connected close to the VCC and GND pins, will properly decouple the device.

R0-R9: Row Address Inputs

C0-C9: Column Address Inputs

B0-B1: Bank-Pair Select Inputs — Strobed by ADS. Decoded to enable one of the RAS outputs when RASIN goes LOW in the access modes.

Q0-Q9: Multiplexed Address Outputs — Selected from the row address input latch, the column address input latch, or the refresh counter.

RASIN: Row Address Strobe Input — Drives the selected RASm output in the access modes and all RAS outputs in the Refresh mode.

ADS: Address (Latch) Strobe Input — Strobes input row address, column address, and Bank Select inputs into the respective latches when HIGH; latches on HIGH-to-LOW transition.

OE: Output Enable — When \overline{OE} is LOW the address and control outputs are enabled. When \overline{OE} is HIGH the address outputs are in high-impedance and the control outputs are pulled HIGH.

R/C: Row/Column Select Input — In the Externally-Controlled-Access, it is used to select either the row address input latch or the column address input latch onto the address outputs. In the Refresh mode, when $\overline{\text{AUTO}}$ is HIGH, it is used to select between the refresh address (R/C HIGH) and the column address (R/C LOW). When $\overline{\text{AUTO}}$ is LOW R/C is disabled.

CASINO-3: Column Address Strobe Inputs — In the Externally-Controlled-Access mode the CASINn directly drives CASn output. In the Auto-Access mode, it is used to enable the corresponding CASn output (See CAS0-3 description).

WEIN: Write Enable Input.

WE: Write Enable Output.

CAS0-3: Column Address Strobe Outputs — In the Externally-Controlled-Access mode the CAS outputs follow the CASIN inputs. In the Auto-Access mode the CASIN inputs are used to enable the CAS outputs, but the CAS outputs are asserted LOW, with proper delay from the RAS output, by the RASIN signal via the Auto-Access timing generator. In the Auto-Access mode, the CASn goes HIGH only when the corresponding CASIN goes HIGH. Extending the CASn LOW duration while RASIN and RASIN go HIGH satisfies the precharge requirement of the dynamic RAMs.

RAS0-3: Row Address Strobe Outputs — When RFSH is HIGH the selected row address strobe output (decoded from signals B0, B1) follows the RASIN input. When RFSH is LOW all RAS outputs go LOW together following RASIN going LOW.

AUTO: Auto-Access Input — When AUTO is LOW the Auto-Access mode is selected (see Auto-Access mode description).

RFSH: Refresh Input — When RFSH is LOW the Refresh mode is selected (see Refresh mode description).

Externally-Controlled-Access Mode (ECA)

In this mode, selected when $\overline{\text{AUTO}}$ and $\overline{\text{RFSH}}$ are held HIGH, the 673104 serves as a straightforward multiplexer and driver for the address and control signals to the DRAMs. The $\overline{\text{RASM}}$ output selected by the B0 and B1 inputs follows the $\overline{\text{RASIN}}$ input, and each of the $\overline{\text{CAS}}$ outputs follows its corresponding $\overline{\text{CASIN}}$ input. When $\overline{\text{R/C}}$ is HIGH the row address is enabled onto the Q0-9 outputs. When $\overline{\text{R/C}}$ is LOW the column address latch is enabled onto Q0-9 outputs.

The RASIN — RAS, CASIN — CAS, and R/C — Q0-9 control paths are independent to allow the system designer maximum flexibility and support of special DRAM access and refresh modes such as NIBBLE mode, PAGE mode, CAS before RAS, etc.

To allow tighter timing of the sequence of control signals to the Dynamic RAM, several difference timing parameters have been specified for the Externally Controlled Access mode. These

parameters specify the maximum difference between the various "control channels" of the device. In particular, using switching characteristics t_{d7} and t_{d8} is very useful when designing the delay from RASIN going LOW to R/C and the delay between R/C going LOW to CASIN going LOW (see Applications).

BANK SELECT (S	ENABLED RASh	
B1	B0	ENABLED HASI
0	.0	RAS0
0	14	RAS1
1	0	RAS2
1	1	RAS3

Table 1. Memory Bank Decode

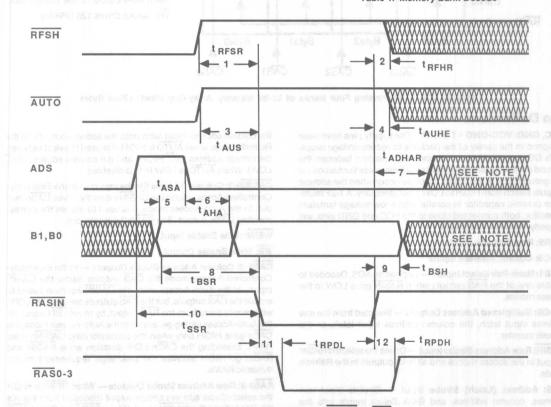


Figure 3. Externally-Controlled-Access—RASIN-to-RAS Timing

Note: To prevent glitches on the RAS0-3 outputs, operating conditions tagh or tagh must be satisfied.



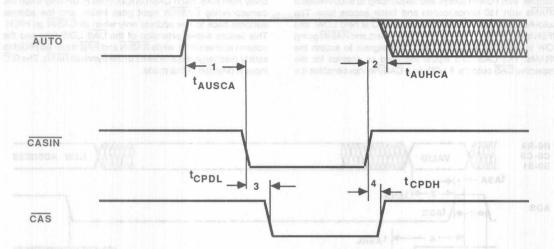


Figure 4. Externally-Controlled-Access-CASIN to CAS Timing

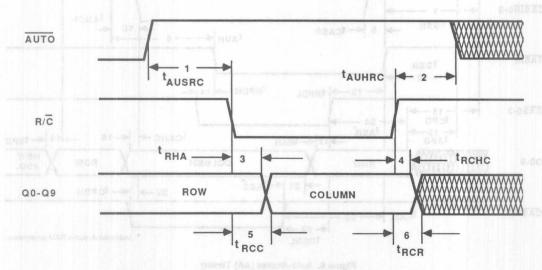


Figure 5. Externally-Controlled-Access R/C Timing

Note: t_{RCC} will be met only if the column address is available t_{APD} before it appears on Q0-9 outputs or if it is latched by ADS.

Auto-Access Mode (AA)

In the Auto-Access mode the 673104 provides the system designer with built-in delays and sequencing to accommodate \overline{DRAMs} with 150 nanoseconds and faster access time. The Auto-Access mode is selected when \overline{AUTO} is held LOW and RFSH is held HIGH. The R/\overline{C} input is disabled, and \overline{RASIN} going LOW initiates the sequence of control signals to access the DRAMs. The $\overline{CASIN0-3}$ inputs are used as enables for the respective \overline{CAS} outputs. A LOW on a \overline{CASIN} input enables the

CASn output to be driven LOW with the internally generated delay from RAS. Each CASn output goes HIGH only when the corresponding CASINn input goes HIGH, and the address switches back to row address only when all CASIN go HIGH. This feature allows extension of the CAS LOW time and the column address time, while RASIN and RASm can go HIGH to satisfy precharge requirements of the dynamic RAMs. The R/C input is disabled in this mode.

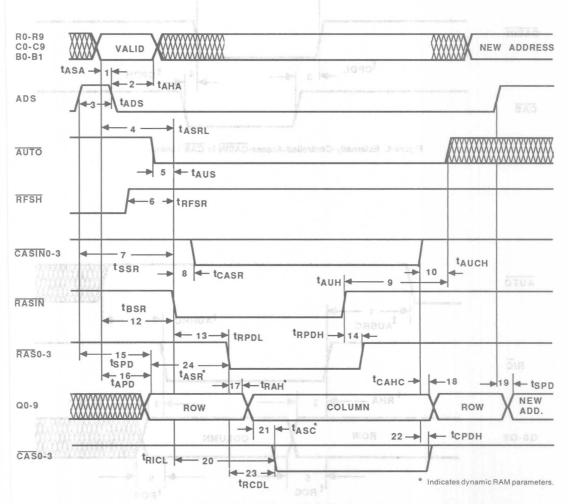


Figure 6. Auto-Access (AA) Timing

Refresh Mode (RFSH)

When $\overline{\text{RFSH}}$ is held LOW the refresh counter contents are enabled onto the Q0-9 address outputs, provided either R/ $\overline{\text{C}}$ is held HIGH, or $\overline{\text{AUTO}}$ is held LOW, or both conditions exist. In this mode all four $\overline{\text{RAS}}$ outputs follow the $\overline{\text{RASIN}}$ input signal. The refresh counter increments the refresh address when either $\overline{\text{RASIN}}$ or $\overline{\text{RFSH}}$ goes HIGH while the other is LOW. When $\overline{\text{AUTO}}$ is LOW the $\overline{\text{CASIN}}$ 0-3 inputs are isolated and $\overline{\text{CAS}}$ 0-3 are held HIGH. Also, when $\overline{\text{AUTO}}$ is LOW the R/ $\overline{\text{C}}$ input is isolated from the output multiplexer, and the refresh address appears at the Q0-9 outputs.

When $\overline{\text{AUTO}}$ is HIGH, pulling R/ $\overline{\text{C}}$ LOW enables the column address onto the Q0-9 outputs. Also, each of the $\overline{\text{CAS}}$ outputs follows its respective $\overline{\text{CASIN}}$ input. This feature may be used

when implementing error correction and detection "scrubbing" for four-bank memory arrays. "Scrubbing" is a term describing a cyclic error correction of soft errors in the memory array, done within the refresh cycles. On every refresh cycle one location of the memory array is accessed and the data in that location goes, if necessary, through a correction cycle (a read-modify-write memory cycle). The 673104 provides the facilities to force a column address onto the Q0-9 address outputs and to assert the CAS0-3 outputs within a refresh cycle to allow scrubbing. A column counter and a bank counter need to be added externally to provide the column addresses for scrubbing.

The refresh counter is a 10-bit counter that resets to 0 on power-up and rolls-over to 0 at 1023.

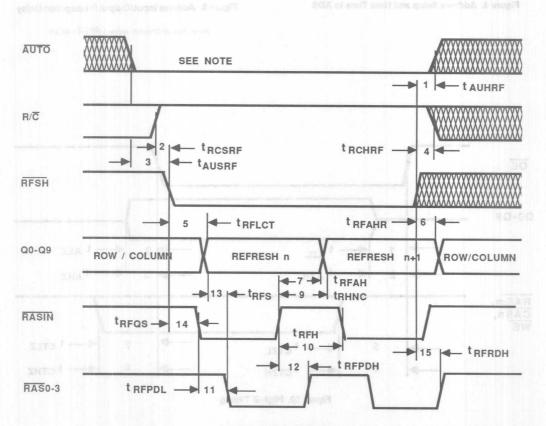
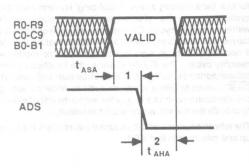


Figure 7. Refresh Timing

Note: In the REFRESH mode, AUTO must be LOW or R/C must be HIGH to guarantee the refresh address on the Q0-9 outputs.

9



ADS

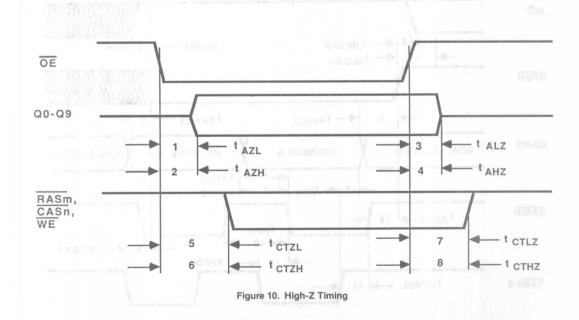
t_{SPD} 1 2 t_{APD}

Q0-Q9 (NOTE) N-1 N N+1

Figure 8. Address Setup and Hold Time to ADS

Figure 9. Address Input/Output Propagation Delay

Note: Row or Column address (RFSH = HIGH).



R0-R9 C0-C9

Absolute Maximum Ratings (See Note)

Supply voltage, VCC	0.5 V to 7 V
	65° C to +150° C
	1.5 V to 5.5 V
	co-St- = val. godlov sugn 150 mA
	300°C

Note: "Absolute Maximum Ratings" are the values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of operating conditions provides conditions for actual device operation.

Operating Conditions | KAM = 75V | V KD = MIV | Hithrot repose from a will pure | Hithrot increase with a paint | Hithrot increase will have a like the property | Hithrot increase will have a like the property | Hithrot increase will have a like the property | Hithrot increase will have a like the property | Hithrot increase will have a like the property | Hithrot increase will have a like the property | Hithrot increase will have a like the property | Hithrot increase will have a like the property | Hithrot increase will have a like the property | Hithrot increase will have a like the property | Hithrot increase will have a like the property | Hithrot increase will have a like the property | Hithrot increase will have a like the property | Hithrot increase will have a like the property | Hithrot increase will have a like the property | Hithrot increase will have a like the property | Hithrot increase will have a like the property | Hithrot increase will have a like the property | Hithrot increase will have a like the property | Hithrot increase will have a like the property | Hithrot increase will have a like the property | Hittory | Hithrot increase will have a like the property | Hittory | Hit

SYMBOL	PARAMETER	FIGURE/ NUMBER	673104A MIN TYP MAX	673104 MIN TYP MAX	UNIT
VCC	Supply voltage AMM SOUN AM TO THOSE		4.5 5.5	4.5 5.5	V
TA	Ambient temperature		0 75	0 75	C
tASA	Address setup time to ADS LOW	8/1	18	18	ns
tADS	Address strobe pulse width HIGH		26	26	ns
tAHA	Address hold time from ADS LOW	8/2	10 shold menus	10	ns
a I no	EXTERNALLY CONTROLLED ACCESS PARAMETER	Barbaran a decid	deal frantism facilia	ets viscosit I	257
t _{ADHAR}	ADS LOW hold from RASIN HIGH	3/7	0	0	ns
tBSR	Bank select setup to RASIN LOW (ADS = HIGH)	3/8	10	10	ns
tBSH	Bank select hold from RASIN HIGH (ADS = HIGH)	3/9	10	10	ns
tssr	Address strobe HIGH setup to RASIN LOW (B0, B1 STABLE)	3/10	20	20	ns
t _{AUHE}	AUTO hold from RASIN HIGH	3/4	55	55	ns
†AUSRC	AUTO HIGH setup to R/C LOW	5/1	25	25	ns
tAUHRC	AUTO HIGH hold from R/C HIGH	5/2	10	10	ns
tAUSCA	AUTO HIGH setup to CASIN LOW	4/1	45	45	ns
tAUHCA	AUTO HIGH hold from CASIN HIGH	4/2	0	0	ns
taus	AUTO setup to RASIN LOW	3/3	0000000	0	ns
tRFSR	RFSH HIGH setup to RASIN LOW (to guarantee tASR = 0)	3/1	10	10	ns
trehr.	RFSH HIGH hold from RASIN HIGH	3/2	10	10	ns
201	AUTOMATIC ACCESS PARAMETER		The state of the s		EKIDS.
t _{ADHAR}	ADS LOW hold from RASIN HIGH	3/7	0	0	ns
tBSR	Bank select setup to RASIN LOW (ADS = HIGH)	6/12	10	10	ns
tBSH	Bank select hold from RASIN HIGH (ADS = HIGH)	3/9	10	10	ns
tASRL	Address setup to RASIN LOW (ADS = HIGH) (tASRL = td2 max to guarantee tASR = 0)	6/4	34	34	ns
tAUS	AUTO setup to RASIN LOW	6/5	0	0	ns
tRFSR	RFSH HIGH setup to RASIN LOW (to guarantee tASR = 0)	6/6	10	10	ns
tssr	Address strobe HIGH to RASIN LOW (B0, B1 STABLE)	6/7	20	20	ns
tCASR	CASIN0-1 setup to RASIN LOW	6/8	-30	-30	ns
tAUH	AUTO hold from RASIN HIGH	6/9	50	50	ns
†AUCH	AUTO LOW hold from CASIN HIGH	6/10	0	0	ns
2 (49	REFRESH PARAMETER	E E E	Tugged stendbe n	ES 3 190 W63 2	110
t _{AUHRF}	AUTO LOW hold from RFSH HIGH (R/C LOW)	7/1	10	10	ns
trcsrf	R/C HIGH setup to RFSH LOW (AUTO HIGH)	7/2	20	20	ns
^t AUSRF	AUTO LOW setup to RFSH LOW (R/C LOW)	7/3	20	20	ns
tRCHRF.	R/C HIGH hold from RFSH HIGH (AUTO HIGH)	7/4	10	10	ns
tRFH	RASIN HIGH during refresh	7/10	30	30	ns
tRFQS	RFSH LOW setup to RASIN LOW (to guarantee tRFS)	7/14	34	34	ns

Electrical Characteristics V_{CC} = 5 V ±10%, 0°C ≤ T_A ≤75°C. Typicals are for V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	CONDITIONS	FIGURE/ NUMBER	MIN TYP MAX	UNIT
VIC	Input clamp voltage	I _{IN} = -18 mA, V _{CC} = MIN		-0.8 -1.2	V
ΉΗ	Input high current	V _{IN} = 2.7 V, V _{CC} = MAX	a. se 01 ge	50	μΑ
ICTL	Output load current for RAS, CAS, WE	V _{OUT} = 0.4 V, V _{CC} = MAX Chip deselect	ार्थः कर्णामस् १८ मोसीस स्था अ	-1.5 -2.5	mA
IIL	Input low current except for RFSH	V _{IN} = 0.4 V, V _{CC} = MAX		-20 -250	μΑ
ILRF	Input low current for RFSH	V _{IN} = 0.4 V, V _{CC} = MAX	89013	-80 -500	μΑ
VIL	Input low threshold (Note 1)		THE LABOR DE STREET	0.8	V
VIH	Input high threshold (Note 1)	ALI SMANA	(1)	2.0	V
VOL1	Output low voltage	IOUT = 1 mA, VCC = MIN	60	0.5	V
VOL2	Output low voltage	IOUT = 12 mA, VCC = MIN	muraneg	8.0 Amelded ten	V
VOH	Output high voltage	IOUT = -1 mA, VCC = MIN	JA of amilt o	2.4 3.0	V
ЮН	Output source current (Note 2)	VOUT = 0.8 V, VCC = MIN	aw adlag no	-50 -140	mA
IOL	Output sink current (Note 2)	VOUT = 2.4 V, VCC = MIN	kir of amid	40 100	mA
loz	Three-state output current (address output)	0.4 V ≤ V _{OUT} ≤ 2.7 V V _{CC} = MAX, Chip deselect	THE CONTRACT	-50 50	μΑ
ICC	Supply current	V _{CC} = MAX	rs mita	190 280	mA
CIN	Input capacitance	T _A = 25°C	S receipt later	10	pF

Switching Characteristics (See Note 3)

SYMBOL	EXTERNALLY CONTROLLED ACCESS PARAMETER	FIGURE/ NUMBER	673104A MIN TYP MAX	673104 MIN TYP MAX	UNIT
t _{RHA}	Row addresses remaining valid from R/C LOW	5/3	0	0	ns
tRPDL	RASIN to RAS LOW delay	3/11	23	23	ns
tRPDH	RASIN to RAS HIGH delay	3/12	33	33	ns
tAPD	Address input to output delay	9/2	60	60	ns
tWPDL	WEIN to WE LOW delay	1 - CA1A - 0	50	50	ns
tWPDH	WEIN to WE HIGH delay	LINE OF	45	45	ns
tCPDL	CASIN to CAS LOW delay	4/3	28	28	ns
tCPDH	CASIN to CAS HIGH delay	4/4	40	40	ns
tRCC	Column select to column address valid	5/5	50	50	ns
tRCR	Row select to row address valid	5/6	53	53	ns
^t d1	(CASIN to CAS LOW delay)-(RASIN to RAS LOW delay)		-5 10	-5 10	ns
t _{d2}	(Address input to output delay)-(RASIN to RAS LOW delay)		34	34	ns
t _{d3}	(Address input to output delay)-(CASIN to CAS LOW delay)	HOR	0 28	0 28	ns
t _{d4}	Skew between address output lines	ATTEMAN	12	12	ns
t _{d5}	(RASIN to RAS HIGH delay)-(RASIN to RAS LOW delay)	d dia ka	-10 10	-10 10	ns
td6	(CASIN to CAS LOW delay)-(CASIN to CAS HIGH delay)	abis OTUAL	-12 12	-12 12	ns
tSPD	ADS HIGH to address output valid	9/1	64	64	ns
†RCHC	Column addresses remaining valid from R/C HIGH	5/4	0	0	ns
t _d 7	tRPDL - tRHA		16	16	ns
t _{d8}	tRCC - tCPDL	apeus ch W	27	27	ns

Switching Characteristics (Continued)

SYMBOL	AUTO ACCESS PARAMETER	FIGURE/ NUMBER		3104A TYP MAX		73104 TYP MAX	UNIT
†RICL	RASIN to CAS LOW delay	6/20		83		90	ns
tRCDL	RAS to CAS LOW delay	6/23	30	73	30	80	ns
tRPDL	RASIN to RAS LOW delay	6/13		23		23	ns
tRPDH	RASIN to RAS HIGH delay	6/14	1	33		33	ns
tAPD	Address input to output delay	6/16		60		60	ns
tWPDL	WEIN to WE LOW delay			50		50	ns
tWPDH	WEIN to WE HIGH delay			45		45	ns
tCPDH	CASIN to CAS HIGH delay	6/22		40	1	40	ns
tRAH	Row address hold time from RAS LOW	6/17	15		15	K-1	ns
t _{d2}	(Address input to output delay)-(RASIN to RAS LOW delay)			34		34	ns
tSPD	ADS HIGH to address output valid	6/19		64		64	ns
tASC	Column address setup to CAS LOW	6/21	0		0		ns
tCAHC	Column address remaining valid from CASINO-3 HIGH	6/18	5	3e-07	5	000	ns
tASR	Row address valid before RAS LOW	6/24	0		0		ns
t _{d5}	(RASIN to RAS HIGH delay)-(RASIN to RAS LOW delay)	age in Loads	-10	10	-10	10	ns
	REFRESH PARAMETER	9694 DN	10895	OLD OF BARR	1977 199	nerrowqeu	
^t RFLCT	RFSH LOW to refresh address valid (AUTO LOW or R/C HIGH)	7/5		50	wil	50	ns
tRFPDL	RASIN LOW to RAS LOW delay during refresh	7/11		26		26	ns
tRFPDH	RASIN HIGH to RAS HIGH delay during refresh	7/12	-352	38		38	ns
tRFAH	Refresh address held from RASIN HIGH (RFSH LOW)	S.V7/7	0	38 beac	0	педО	ns
trhnc trhnc	RASIN HIGH to new refresh address valid	7/9	3g 00	8 572	0	72	ns
tRFAHR	Refresh address held from RFSH HIGH	7/6	0 0	t bsau	0	перС	ns
tres V 8	Refresh address valid to RAS LOW (provided tRFQS is satisfied)	7/13	0 00	DB been	0	Closec	ns
tRFRDH	RFSH HIGH to RAS HIGH (for three banks, RASIN = LOW)	7/15	100	45	land and the land	45	ns
t _d 9	(RASIN to RAS HIGH delay)-(RASIN to RAS LOW delay)		-9	16	-9	16	ns
300 1011 113 0	THREE-STATE PARAMETER						
t _{AZL}	OE LOW to address output LOW	10/1		50		50	ns
t _{AZH}	OE LOW to address output HIGH	10/2	109	60		60	ns
tALZ	OE HIGH to address output HI-Z from LOW	10/3	- 90	35		35	ns
^t AHZ	OE HIGH to address output HI-Z from HIGH	10/4		25		25	ns
tCTZL	OE LOW to control output LOW	10/5		50		50	ns
tCTZH	OE LOW to control output HIGH	10/6		50		50	ns
tCTLZ	OE HIGH to control output HI-Z from LOW	10/7		35		35	ns
tCTHZ	OE HIGH to control output HI-Z from HIGH	10/8	garden and	30	t	30	ns

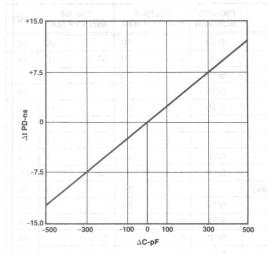
Note 1: These are absolute voltage levels with respect to the ground pins on the device and includes all overshoots due to system or tester noise.

Do not attempt to test these values without suitable equipment.

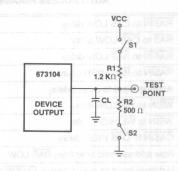
Note 2: This test is provided as a monitor of driver output source and sink current capability. Caution should be exercised in testing this parameter.

One output should be tested at a time and test duration should not exceed one second.

Note 3: Output load capacitance is typical for four banks of 32 DRAMs with trace capacitance. The values are: Q0-8 C_L = 800 pF, \overline{RAS} 0-3 C_L = 250 pF, \overline{WE} C_L = 800 pF, \overline{CAS} 0-3 C_L = 300 pF.



Change in Propagation Delays vs. Change in Loading Capacitance Relative to the Specified Load



Note: Input pulse 0 V to 3.0 V, t_R = t_F = 2.5 ns, f = 1.0 MHz, t_{PW} = 200 ns. Input reference point on AC measurements is 1.5 V. Output reference points are 2.4 V for HIGH and 0.8 V for LOW.

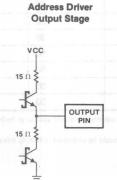
Address Outputs

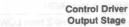
TEST	S1	S2	CL	MEASURED AT
t _{PD}	Open	Closed	800 pF	0.8 V, 2.4 V
^t PZH	Closed	Closed	800 pF	2.4 V
t _{PHZ}	Open	Closed	15 pF	VOH -0.5 V
^t PZL	Closed	Closed	800 pF	0.8 V
t _{PLZ}	Closed	Open	15 pF	V _{OL} +0.5 V

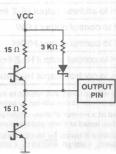
Control Outputs

TEST	S1	S2	CL	MEASURED AT
t _{PD}	Open	Closed	CL	0.8 V, 2.4 V
t _{PZH}	Open	Closed	CL	2.4 V
t _{PHZ}	Open	Closed	15 pF	V _{OH} -0.5 V
^t PZL	Open	Open	CL	0.8 V
^t PLZ	Open	Open	15 pF	V _{OL} +0.5 V

Where C₁ = 250 pF for RAS, 300 pF for CAS, and 800 pF for WE.







Applications

Microprocessor Interface

The 673104 Dynamic RAM Controller provides the address and control signals required to access and refresh dynamic RAMs. When interfaced to a 32-bit microprocessor, some external logic is required to generate a refresh clock as well as to perform access/refresh arbitration and interface handshake functions. For some microprocessors external logic is required also to

decode the address and control signal to arrive at four data strobes. A hidden refresh (refresh which is transparent to the system) scheme may be implemented in the interface circuitry taking advantage of "free" system time to refresh the memory, and falling back to "forced" refresh when hidden refresh cannot be performed.

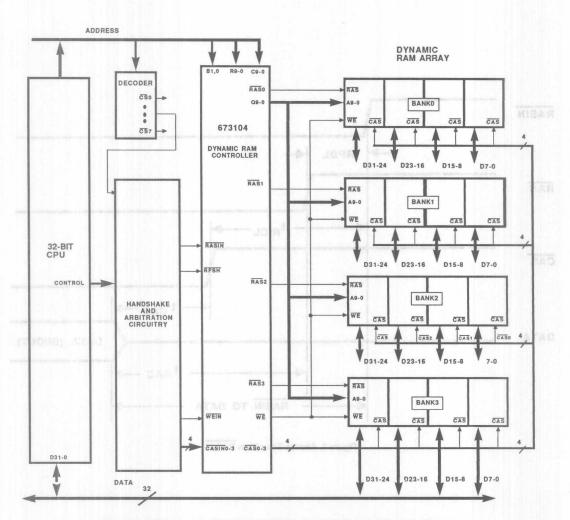
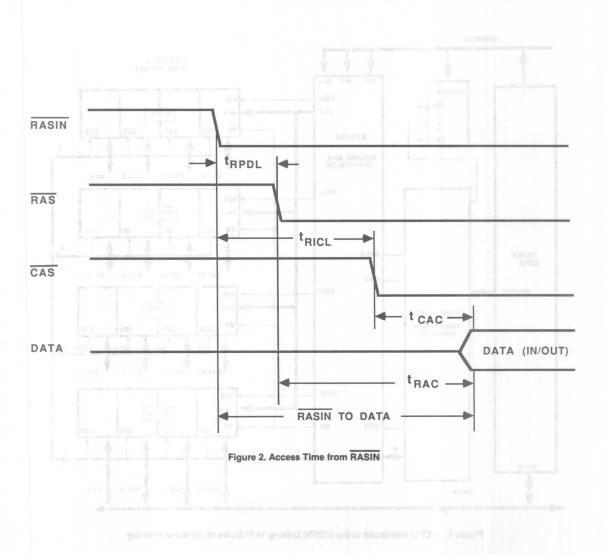


Figure 1. A CPU Interfaced to the 673104 Driving 16 M Bytes of Dynamic Memory

Determining System Performance (Auto-Access)

When determining system performance the dynamic RAM parameters must be considered as well as the controller's propagation delays. For both read and write cycles the access time for the dynamic RAM is t_{RAC} (RAS access time) from RAS

going LOW or t_{CAC} ($\overline{\text{CAS}}$ access time) from $\overline{\text{CAS}}$ going LOW. Since the $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ coming out of the controller are initiated by the $\overline{\text{RASIN}}$, the controller-memory performance is measured from the $\overline{\text{RASIN}}$ HIGH-to-LOW transition (see Figure 2).



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The time from RASIN to data is calculated to be the longer of:

trici + tcac (RASIN to CAS + CAS to data)

t_{RPDL} + t_{RAC} (RASIN to RAS + RAS to data)

Table 1 illustrates the access times from $\overline{\text{RASIN}}$ achieved for various dynamic RAM speeds.

CONTROL I ED MEMORY			1	PARAMETER		
CONTROLLER/MEMORY -	tRAC	tRPDL	tCAC	tRICL	ACCES	SS TIME FROM RASIN
673104/HM256-12	120	23	60	90		150
673104A/HM256-12	120	23	60	83		143
673104/HM256-15	150	23	75	90		173
673104A/HM256-15	150	23	75	83	613	173
673104/MB8265A-10	100	23	50	90	імажуо 1	140
673104A/MB8265A-10	100	23	50	83	STHOO	133
673104/MB8265A-12	120	23	60	90	1	150
673104A/MB8265A-12	120	23	60	83		143
673104/IMS2620-10	100	23	60	90		150
673104A/IMS2620-10	100	23	60	83		143
673104/IMS2620-12	120	23	70	90		160
673104A/IMS2620-12	120	23	70	83		153

Table 1. Access Times from RASIN for Various Memory Speeds

673104 Parameters

tRICL - RASIN LOW to CAS LOW delay

trepl - RASIN LOW to RAS LOW delay

DRAM Parameters

tRAC — Access time from RAS LOW

t_{CAC} — Access time from CAS LOW

Using the Externally Controlled Access

In the Externally Controlled Access mode \overline{RASIN} controls the selected \overline{RAS} output, $\overline{CASIN0}$ -3 control $\overline{CAS0}$ -3 outputs respectively and $\overline{R/C}$ controls the address multiplexer. The system designer may create, using the \overline{RASIN} , \overline{CASIN} and $\overline{R/C}$ inputs, the required control signal sequence for the specific system being designed. Special dynamic RAM access modes such as

Nibble mode and Page mode access cycles may be performed simply by toggling the appropriate control inputs. Special skew timing specifications have been specified to allow tighter timing control as outlined in the following examples. Both following examples relate to the scheme depicted in Figure 3.

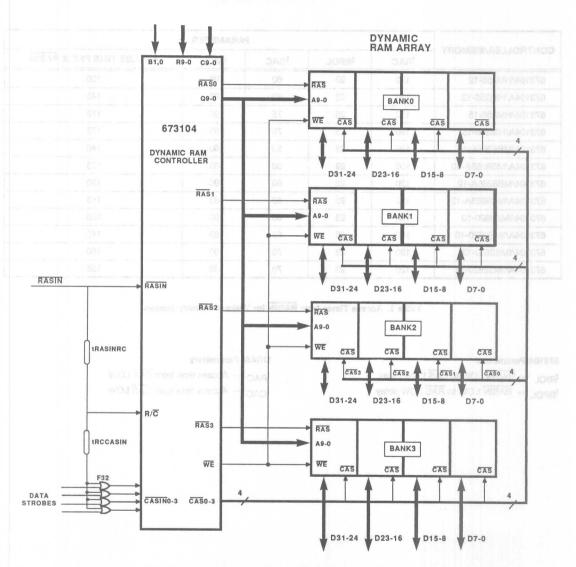


Figure 3. The 673104 in the Externally-Controlled Access Mode

9

Externally Controlled Access (ECA) (Continued)

Example 1: Computing RASIN to R/C Delay

The delay between RASIN going LOW to R/C going LOW (tRASINRC) which is required in order to satisfy the dynamic RAMs' row address hold time (tRAH) is computed as follows:

tRASINRC = tRAH(min) + td7

Where:

 $t_{\mbox{\footnotesize RAH}}(\mbox{min}) - \mbox{\footnotesize Row address hold time (dynamic RAM parameter)}$

td7(max) = tRPDI -tRHA

t_{RPDL} — RASIN to RAS LOW delay

t_{RHA} - Row address held valid from R/C LOW

Example 2: Computing R/C to CASIN Delay

The delay between R/C going LOW and CASIN going LOW (tracasin) which is required in order to satisfy the dynamic RAMs' column address setup (tasc) is computed as follows:

tRCCASIN = tASC(min) + td8 + tpDF32(max)

Where

 $t_{\mbox{\footnotesize ASC}}(\mbox{min}) - \mbox{\footnotesize Column address setup (dynamic RAM parameter)}$

td8(max) = tRCC-tCPDL

t_{RCC} — R/C low to column address valid

t_{CPDL} — CASIN to CAS LOW delay

t_{PD}F32(max) — Propagation delay of the OR gate used to validate CASIN

Better system performance may be achieved using the t_{d7}, t_{d8} switching parameters to calculate t_{RASINRC} and t_{RCCASIN} than when using the t_{RPDL}, t_{RCDL}, t_{RCC} and t_{RHA} parameters (see Externally Controlled Access switching parameters).

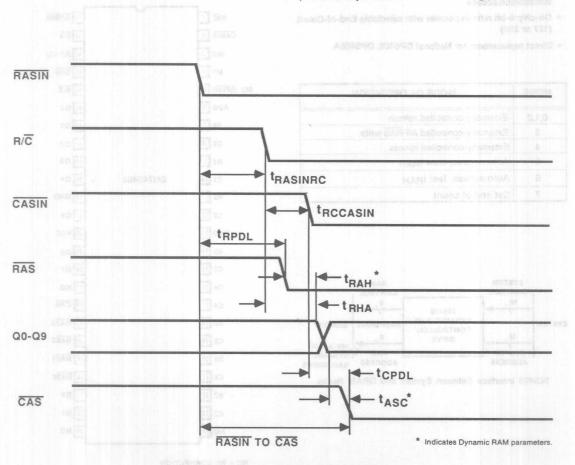


Figure 4. Externally Controlled Access Timing

64K Dynamic RAM Controller/Driver

SN74S408/DP8408A SN74S408-2/DP8408A-2

Features/Benefits

MODE

0,1,2

3

4

5

6

7

SYSTEM

SYSTEM

CONTROL

18

SYSTEM

- · All DRAM drive functions on one chip have on-chip highcapacitance-load drivers (specified up to 88 DRAMs)
- Drives directly all 16K and 64K DRAMs: Capable of addressing up to 256K words
- Propagation delays of 25 nsec typical at 500-pF load
- Supports READ, WRITE and READ-MODIFY-WRITE cycles
- Six operating modes support externally-controlled access and refresh, automatic access, as well as special memory initialization access
- · On-chip 8-bit refresh counter with selectable End-of-Count (127 or 255)
- Direct replacement for National DP8408, DP8408A

Externally-controlled refresh

Externally-controlled access

Auto access, slow tRAH

Auto access, fast tRAH

74\$408 DYNAMIC RAM

CONTROLLER/

DRIVE

Set end of count

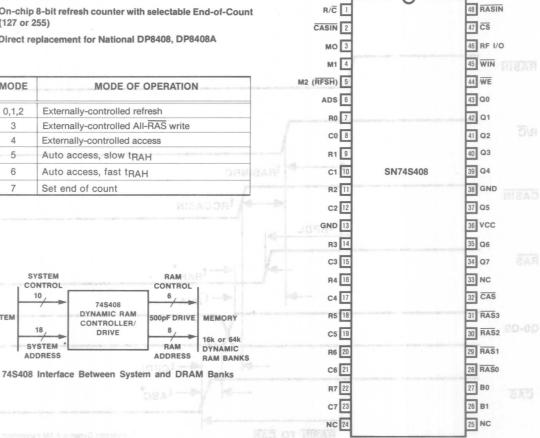
Externally-controlled All-RAS write

Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
SN74S408	48 N, D	AHRE Com (XEM)
SN74S408-2	48 N, D	Com, Speed Option

OLA - Pow address held valid to m RVC LOV

Pin Configuration



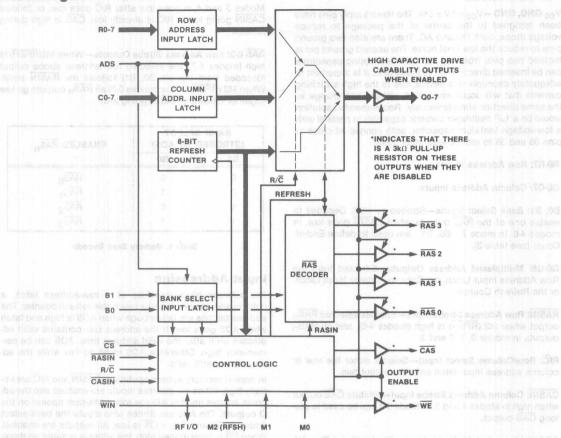
NC = NO CONNECTION

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RAM

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Block Diagram have privated that anotherent



mil sol a deac di styri en la Batantia la Figure 1. 74\$408 Functional Block Diagram I page 3 and 3 bres and 10 figure 1. 74\$408 Functional Block Diagram I page 3 and 3 bres and 10 figure 1.

Description

The 74S408 is a Multi-Mode Dynamic RAM Controller/Driver capable of driving directly up to 88 DRAMs. 18 address lines allow the 74S408 to drive all 16K and 64K DRAMs and addresses up to 256K words. Since the 74S408 is a one-chip solution (including capacitive-load drivers), it minimizes propagation delay skews, and saves board space.

The 74S408's 6 operating modes offer externally-controlled or on-chip automatic access and externally-controlled refresh. An on-chip refresh counter makes refreshing less complicated; and automatic memory initialization is both simple and fast.

The 74S408 is a 48-pin DRAM Controller/Driver with 8 multiplexed address outputs and 6 control signals. It consists of two 8-bit address latches, an 8-bit refresh counter,

and control logic. All address output drivers are capable of driving 500pf loads with propagation delays of 25nsec. The 74S408 timing parameters are specified driving the typical load capitance of 88 DRAMs, including trace capitance.

The 74S408 can drive up to 4 banks of DRAMs, with each bank comprised of 16Ks, or 64Ks. Control signal outputs $\overline{\text{RAS}}, \overline{\text{CAS}},$ and $\overline{\text{WE}}$ are provided with the same driving capability. Each $\overline{\text{RAS}}$ output drives one bank of DRAMs so that the four $\overline{\text{RAS}}$ outputs are used to select the banks, while $\overline{\text{CAS}}, \overline{\text{WE}}$ and the multiplexed addresses can be connected to all the banks of DRAMs. This leaves the nonselected banks in the standby mode (less than one tenth of the operating power) with the data output in three-state. Only the bank with its associated $\overline{\text{RAS}}$ low will be written to or read from, except in mode 3 where all $\overline{\text{RAS}}$ signals go low to allow fast memory initialization.

Pin Definitions

 V_{CC} GND, GND— $V_{CC}=5V\pm5\%$. The three supply pins have been assigned to the center of the package to reduce voltage drops, both DC and AC. There are also two ground pins to reduce the low level noise. The second ground pin is located two pins from V_{CC} , so that decoupling capacitors can be inserted directly next to these pins. It is important to adequately decouple this device, due to the high switching currents that will occur when all 8 address bits change in the same direction simultaneously. Recommended solution would be a $1\mu F$ multilayer ceramic capacitor in parallel with a low-voltage tantalum capacitor, both connected close to pins 36 and 38 to reduce lead inductance.

R0-R7: Row Address Inputs.

C0-C7: Column Address Inputs.

B0, B1: Bank Select Inputs—Strobed by ADS. Decoded to enable one of the RAS outputs when RASIN goes low, in modes 4-6. In mode 7 B0, B1 are used to define End-of-Count (see table 3).

Q0-Q8: Multiplexed Address Outputs—Selected from the Row Address Input Latch, the Column Address Input Latch, or the Refresh Counter.

RASIN: Row Address Strobe Input—Enables selected RAS_n output when M2 (RFSH) is high (modes 4-6), and all RAS_n outputs in modes 0, 1, 2 and 3.

R/C: Row/Column Select Input—Selects either the row or column address input latch onto the output bus.

CASIN: Column Address Strobe Input—Inhibits CAS output when high in Modes 4 and 3. In Mode 6 it can be used to prolong CAS output.

ADS: Address (Latch) Strobe Input—Strobes Input Row Address, Column Address, and Bank Select Inputs into respective latches when high; latches on High-to-Low transition.

CS: Chip Select Input—Three-state's the Address Outputs and puts the control signal into a high-impedance logic "1" state when high (unless refreshing in mode 0, 1, 2). Enables all outputs when low.

M0, M1, M2 (RFSH): Mode Control Inputs—These 3 control pins determine the 6 modes of operation of the 74S408 as depicted in Table 1.

RF I/O—The I/O pin functions as a Reset Counter Input when set low from an external open-collector gate, or as a flag output. The flag goes active (low) when M2 = 0 (modes 0, 1, 2 or 3) and the End-of-Count output is at 127 or 255 (see Table 3).

WIN: Write Enable Input.

WE: Write Enable Output-Buffered output from WIN.

CAS: Column Address Strobe Output-In Modes 5 and 6,

CAS transitions low following valid column address. In Modes 3 and 4, it goes low after R/C goes low, or follows CASIN going low if R/C is already low. CAS is high during refresh.

RAS 0-3: Row Address Strobe Outputs—When M2(RFSH) is high (modes 4-7), the selected row address strobe output (decoded from signals B0, B1) follows the RASIN input. When M2 (RFSH) is low (modes 0-3) all RAS_n outputs go low together following RASIN going low.

	SELECT D BY ADS)	ENABLED RAS
B1	В0	
0	0	RAS ₀
0	1	RAS ₁
1	0	RAS ₂
1	1	RAS ₃

Table 1. Memory Bank Decode

Input Addressing

The address block consists of a row-address latch, a column-address latch, and a resettable refresh counter. The address latches are fall-through when ADS is high and latch when ADS goes low. If the address bus contains valid addresses until after the valid address time, ADS can be permanently high. Otherwise ADS must go low while the addresses are still valid.

In normal memory access operation, $\overline{\text{RASIN}}$ and $\overline{\text{R/C}}$ are initially high. When the address inputs are enabled into the address latches (modes 4-6) the row addresses appear on the Q outputs. The Address Strobe also inputs the bank-select address, (B0 and B1). If $\overline{\text{CS}}$ is low, all outputs are enabled. When $\overline{\text{CS}}$ is transitioned high, the address outputs go three-state and the control outputs first go high through a low impedance, and then are held by an on-chip high impedance. This allows output paralleling with other 74S408s for multiaddressing. All outputs go active about 50ns after the chip is selected again. If $\overline{\text{CS}}$ is high, and a refresh cycle begins, all the outputs become active until the end of the refresh cycle

Drive Capability

The 74S408 has timing parameters that are specified with up to 600pF loads for \overline{CAS} , 500pF loads for Q_0 - Q_7 and \overline{WE} , and 150 pF loads for \overline{RAS}_n outputs. In a typical memory system this is equivalent to about 88 5V-only DRAMs, with trace lengths kept to a minimum. Therefore, the chip can drive four banks each of 16 or 22 bits, or two banks of 32 or 39 bits, or one bank of 64 or 72 bits.

Less loading will slightly reduce the timing parameters, and more loading will increase the timing parameters, according to the graph of Figure 6). The AC performance parameters are specified with the typical load capacitance of 88 DRAMs. This graph can be used to extrapolate the variations expected with other loading.

74S408 Driving Any 16K or 64K DRAMs

The 74S408 can drive any 16K or 64K DRAMs. The on-chip 8-bit counter with selectable End-of-Count can support refresh of 128 or 512 rows, while the 8 address and 4 $\overline{\text{RAS}}_n$ outputs can address 4 banks of 16K or 64K DRAMs.

Read, Write, and Read-Modify-Write Cycles

The output signal, \overline{WE} , determines what type of memory access cycle the memory will perform. If \overline{WE} is kept high while \overline{CAS} goes low, a read cycle occurs. If \overline{WE} goes low before \overline{CAS} goes low, a write cycle occurs and DATA at DI (DRAM input data) is written into the DRAM as \overline{CAS} goes low. If \overline{WE} goes low later than town after \overline{CAS} goes low, first a read occurs and DO (DRAM output data) becomes valid; then data DI is written into the same address in the DRAM when \overline{WE} goes low. In this read-modify-write case, DI and DO can-

not be linked together. The type of cycle is therefore controlled by \overline{WE} , which follows \overline{WIN} .

Power-Up Initialize

When V_{CC} is first applied to the 74S408, an internal pulse clears the refresh counter, the internal control flip-flops, and sets the End-of-Count of the refresh counter to 127 (which may be changed via Mode 7). As V_{CC} increases to about 2.3 volts, it holds the output control signals at a level of one Schottky diode-drop below V_{CC} , and the output address to three-state. As V_{CC} increases above 2.3 volts, control of these outputs is granted to the system.

74S408 Functional Mode Description

The 74S408 operates in 6 different functional modes. The operating mode is selected by signals M_0 , M_1 , M_2 . Selecting M_2 , M_1 , M_0 = 0,0,0 or 0,0,1 or 0,1,0 will result at the same operating mode designated as mode 0,1,2 (see Table 2).

	(RFSH)				\$11940
MODE	M2	M1	MO	MODE OF OPERATION	CONDITIONS
	0	0	0	The second section of the second seco	the second of the second
0,1,2	0	0	1	Externally-controlled refresh	RF I/O = EOC
	0	1	0		
3	0	1	1	Externally-controlled All-RAS write	AII-RAS active
4	1	0	0	Externally-controlled access	Active RAS defined by Table
5	1	0	1	Auto access, slow tRAH	Active RAS defined by Table :
6	1	1	0	Auto access, fast tRAH	Active RAS defined by Table
7	1	1	1	Set end of count	See Table 3 for Mode 7

Table 2. 74S408 Mode Select Options

74S408 Functional Mode Descriptions

Modes 0, 1, 2—Externally Controlled Refresh

In this mode, the input address latches are disabled from the address outputs and the refresh counter is enabled onto R_{o} -R, outputs, all $\overline{\text{RAS}}$ outputs are enabled following $\overline{\text{RASIN}}$, and $\overline{\text{CAS}}$ is inhibited. This refreshes the same row in all four banks. The refresh counter increments when either $\overline{\text{RASIN}}$ or $M_2(\overline{\text{RFSH}})$ goes low-to-high while the other is low. RF I/O goes low when the count is 127 or 255 with $\overline{\text{RASIN}}$ and RFSH as set by End-of-Count (see Table 3), low. To reset the counter to all zeroes, RF I/O is set low through an external open-collector driver.

During refresh, $\overline{\text{RASIN}}$ and $M_2(\overline{\text{RFSH}})$ can transition low simultaneously because the refresh counter becomes valid on the output but t_{RFLCT} . This means the counter address is valid on the Q outputs before $\overline{\text{RAS}}$ occurs on all $\overline{\text{RAS}}$ out-

puts, strobing the counter address into that row of all the DRAMS (see Figure 2). To perform externally controlled burst refresh $M_2(\overline{RFSH})$ initially can again have the same edge as \overline{RASIN} , but then can maintain a low state, since \overline{RASIN} going low-to-high increments the counter (performing the burst refresh).

Mode 3—Externally Controlled All-RAS Write

This mode is useful at system initialization. The memory address is provided by the processor, which also perform the incrementing. All four $\overline{\mbox{AS}}$ outputs follow $\overline{\mbox{RASIN}}$ (supplied by the processor), strobing the row address into the DRAMs. R/C can now go low, while $\overline{\mbox{CASIN}}$ may be used to control $\overline{\mbox{CAS}}$ (as in the Externally Controlled Access mode), so that $\overline{\mbox{CAS}}$ strobes the column address contents into the DRAMs. At this time $\overline{\mbox{WE}}$ should be low, causing the data to be written into all four banks of DRAMs. At the end of the write cycle, the input address is incremented and latched by the 74S408 for the next write cycle.

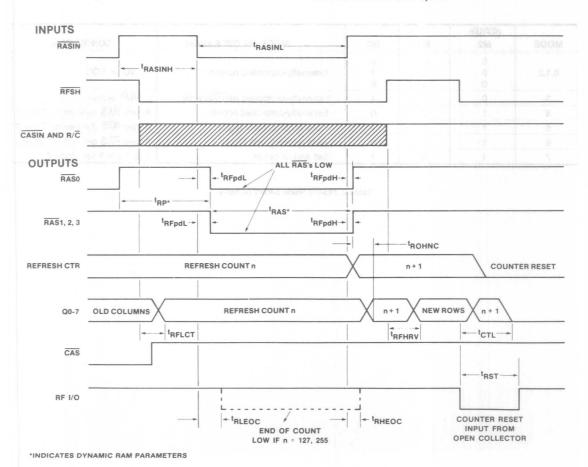


Figure 2. External Control Refresh Cycle (Modes 0, 1, 2)

Mode 4—Externally Controlled Access

This mode facilitates externally controlling all accesstiming parameters associated with the DRAMs. The application of modes 0 and 4 are shown in Figure 3.

Output Address Selection

Refer to Figure 4a. With M2 ($\overline{\text{RFSH}}$) and R/\overline{C} high, the row address latch contents are transferred to the multiplexed address bus output Q0-Q7, provided \overline{CS} is set low. The column address latch contents are output after R/\overline{C} goes low. $\overline{\text{RASIN}}$ can go low after the row addresses have been set up on Q0-Q7. This selects one of the $\overline{\text{RAS}}$ outputs, strobing the row address on the Q outputs into the desired bank of memory. After the row-address hold-time of the DRAMs, R/\overline{C} can go low so that about 40 ns later column addresses appear on the Q outputs.

Automatic CAS Generation

In a normal memory access cycle $\overline{\text{CAS}}$ can be derived from

inputs $\overline{\text{CASIN}}$ or R/C. If $\overline{\text{CASIN}}$ is high, then R/ $\overline{\text{C}}$ going low switches the address output drivers from rows to columns. $\overline{\text{CASIN}}$ then going low causes $\overline{\text{CAS}}$ to go low approximately 40 ns later, allowing $\overline{\text{CAS}}$ to occur at a predictable time (see Figure 4b). For maximum system speed, $\overline{\text{CASIN}}$ can be kept low, since $\overline{\text{CAS}}$ will automatically occur approximately 20 ns after the column addresses are valid, or about 60 ns after R/ $\overline{\text{C}}$ goes low (see Figure 4a). Most DRAMs have a column address set-up time before $\overline{\text{CAS}}$ (t_{ASC}) of 0 ns or - 10 ns. In other words, a t_{ASC} greater than 0 ns is safe. This feature reduces timing-skew problems, thereby improving access time of the system.

Fast Memory Access

For faster access time, R/ \overline{C} can go low a time delay ($t_{RPDL}+t_{RAH}-t_{RHA}$) after RASIN goes low, where t_{RAH} is the Row-Address hold-time of the DRAM.

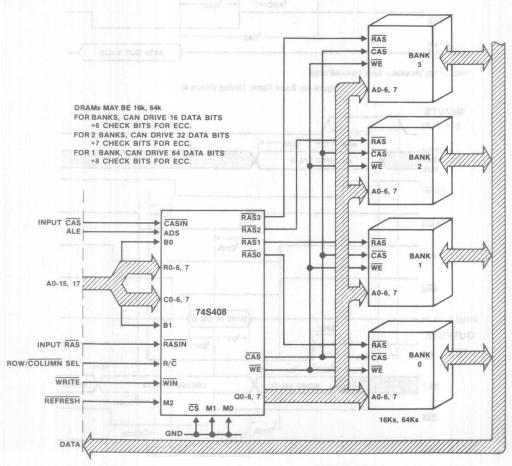
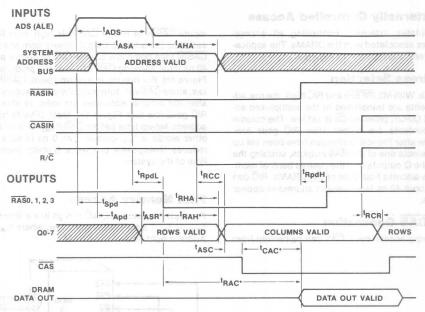
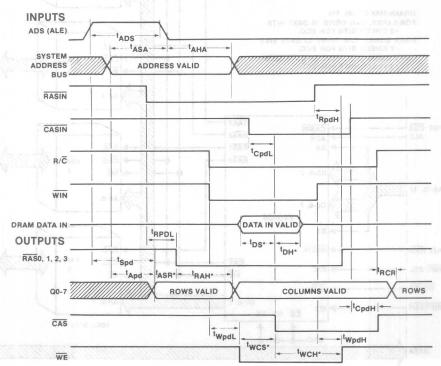


Figure 3. Typical Application of 74S408 Using Externally Controlled Access and Refresh in Modes 0 and 4



*INDICATES DYNAMIC RAM PARAMETERS

Figure 4a. Read Cycle Timing (Mode 4)



*INDICATES DYNAMIC RAM PARAMETERS

Figure 4b. Write Cycle Timing (Mode 4)

Mode 5—Automatic Access

In the Auto Access mode all outputs except \overline{WE} are initiated from \overline{RASIN} . Inputs R/\overline{C} and \overline{CASIN} are unnecessary and the output control signals are derived internally from one input signal (\overline{RASIN}) minimizing timing-skew problems, thereby reducing memory-access time substantially and allowing the use of slower DRAMs.

Automatic Access Control

The major disadvantage of DRAMs compared to static RAMs is the complex timing involved. First, a RAS must occur with the row address previously set up on the multiplexed address bus. After the row address has been held for $t_{\rm RAH}$, (the Row-Address hold-time of the DRAM), the column address is set up and then $\overline{\rm CAS}$ occurs. This is all performed automatically by the 74S408 in this mode.

Provided the input address is valid as ADS goes low, $\overline{\text{RASIN}}$ can go low any time after ADS. This is because the selected $\overline{\text{RAS}}$ occurs typically 27 ns later, by which time the row address is already valid on the address output of the 74S408. The Address Set-Up time (tASR), is 0 ns on $\overline{\text{most}}$ DRAMs. The 74S408 in this mode (with ADS and $\overline{\text{RASIN}}$ edges simultaneously applied) produces a minimum t_{ASR} of 0 ns. This is true provided the input address was valid t_{ASA} before ADS went low (see Figure 5a).

Next, the row address is disabled after t_{RAH} (30 ns minimum); in most DRAMs, t_{RAH} minimum is less than 30 ns. The column address is then set up and t_{ASC} later, \overline{CAS} occurs. The only other control input required is \overline{WIN} . When a write cycle is required, \overline{WIN} must go low at least 30 ns before \overline{CAS} Is output low.

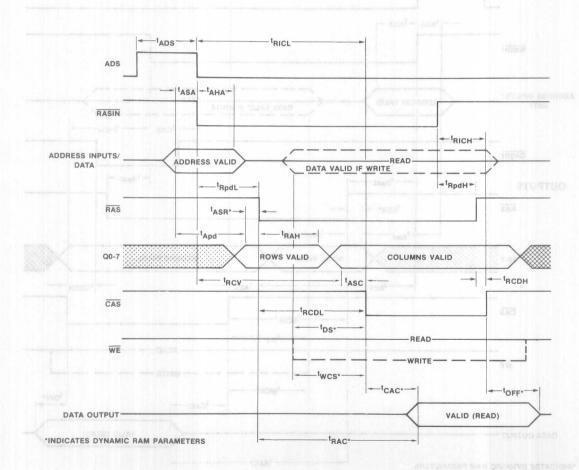


Figure 5a. Modes 5, 6 Timing (CASIN High in Mode 6)

This gives a total typical delay from: input address valid to RASIN (15 ns); to RAS (27 ns); to rows held (50 ns); to columns valid (25 ns); to CAS (23 ns) = 140 ns (that is, 125 ns from RASIN). All of these typical figures are for heavy capacitive loading, of approximately 88 DRAMs. This mode is therefore extremely fast. The external timing is greatly simplified for the memory system designer: the only system signal required is RASIN.

Mode 6—Fast Automatic Access

The Fast Access mode is similar to Mode 5, but has a faster $t_{\rm RAH}$ of 20 ns, minimum. It therefore can only be used with fast 16k or 64k DRAMs (which have a $t_{\rm RAH}$ of 10 ns to 15 ns)

in applications requiring fast access times; $\overline{\text{RASIN}}$ to $\overline{\text{CAS}}$ is typically 105 ns.

In this mode, the R/ \overline{C} pin is not used, but \overline{CASIN} is used to allow an extended \overline{CAS} after \overline{RAS} has already terminated. Refer to Figure 5b. This is desirable with fast cycle-times where \overline{RAS} has to be terminated as soon as possible before the next \overline{RAS} begins (to meet the precharge time, or t_{RP} , requirements of the DRAM). \overline{CAS} may then be held low by \overline{CASIN} to extend the data output valid time from the DRAM to allow the system to read the data. \overline{CASIN} subsequently going high ends \overline{CAS} . If this extended \overline{CAS} is not required, \overline{CASIN} should be set high in Mode 6.

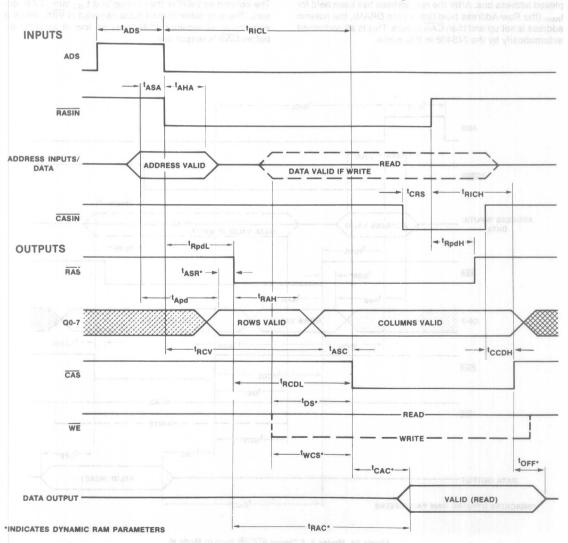


Figure 5b. Mode 6 Timing, Extended CAS

Mode 7—Set End-of-Count

The End-of-Count can be externally selected in Mode 7, using ADS to strobe in the respective value of B1 and B0 (see Table 3). With B1 and B0 the same EOC is 127; with B1 = 0

and B0 = 1, EOC is 255; and with B1 = 1 and B0 = 0, EOC is 127. This selected value of EOC will be used until the next Mode 7 selection. At power-up the EOC is automatically set to 127 (B1 and B0 set to 11).

BANK SE (STROBED		END OF COUNT
B1	В0	SELECTED
0	0	127
4.75 0	1	255
1 0	0	127
1 81	da.na.1(1, an an	127

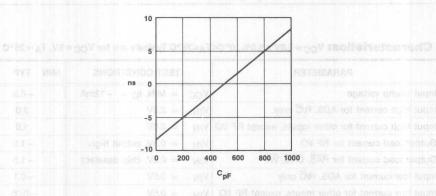


Figure 6. Change in Propagation Delay vs Loading Capacitance Relative to a 500pF Load

SN74S408/-2 Specifications:

Absolute Maximum Ratings (Note 1)

Supply voltage V _{CC} 0.5 V to 7.	.0 V
Storage temperature range65° to +150	0-0
Input voltage	.5 V
Output current	mA
Lead temperature (soldering, 10 seconds)	0°C

NOTE 1: "Absolute Maximum Ratings" are the values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of operating conditions provides conditions for actual device operation.

Operating Conditions

SYMBOL	PARAMETER	FIGURE	MIN	'S408 TYP	MAX	MIN	'S408-2 TYP	MAX	UNIT
Vcc	Supply voltage	r	4.75	0	5.25	4.25		5.25	V
TA	Operating free-air temperature	û.	0		+ 75	0		+ 75	°C
t _{ASA}	Address setup time to ADS	Figures 4a,4b,5a,5b	15	1		15			ns
^t AHA	Address hold time from ADS	Figures 4a,4b,5a,5b	15			15			ns
tADS	Address strobe pulse width	Figures 4a,4b,5a,5b	30			30			ns
^t RHA	Row address held from column select	Figure 4a	10			10			ns
trasinl,H	Pulse width of RASIN during refresh	Figure 2	50			50		Yahii	ns
tRST	counter reset pulse width	Figure 2	70			70	17143		ns

Electrical Characteristics: V_{CC} = 5.0V ± 5.0%, 0 °C≤T_A≤75 °C Typicals are for V_{CC} = 5V, T_A = 25 °C

SYMBOL	PARAMETER	TEST CONDITIONS	MIN TYP MAX	UNIT
VC	Input clamp voltage	V _{CC} = MIN, I _C = -12mA	-0.8 -1.2	V
lH1	Input high current for ADS. R/C only.	V _{IN} = 2.5V	2.0 100	μΑ
l _{IH2}	Input high current for other inputs, except RF I/O	V _{IN} = 2.5V	1.0 50	μΑ
I _I RSI	Output load current for RF I/O	VIN = 0.5V, output high	- 1.5 - 2.5	mA
I _I CTL	Output load current for RAS, CAS, WE	V _{IN} = 0.5V, chip deselect	-1.5 -2.5	mA
IL1	Input low current for ADS. R/C only	V _{IN} = 0.5V	-0.1 -1.0	mA
IL2	Input low current for other inputs, except RF I/O	V _{IN} = 0.5V	-0.05 -0.5	mA
VIL**	Input low threshold	Physical Destruction Patrice and	0.8	V
VIH**	Input high threshold		2.0 V	
V _{OL1}	Output low voltage, except RF I/O	IOL = 20mA	0.3 0.5	V
VOL2	Output low voltage for RF I/O	IOL = 10mA	0.3 0.5	V
VOH1	Output high voltage, except RF I/O	VOH = -1mA	2.4 3.5	V
VOH2	Output high voltage for RF I/O	$IOH = -100\mu A$	2.4 3.5	V
I _{1D}	Output high drive current except RF I/O	VOUT = 0.8V (Note 3)	- 200	mA
loD	Output low drive current, except RF I/O	VOUT = 2.7V (Note 3)	200	mA
loz	Three-state output current (address outputs)	0.4V≤V _{OUT} ≤2.7V, CS = 2.0V, Mode 4	-50 1.0 50	μΑ
ICC	Supply current	VCC = MAX	210 285	mA
CIN	Input capacitance ADS, R/C	T _A = 25 °C	8	pF
CIN	Input capacitance all other inputs	T _A = 25°C	5	pF

Switching Characteristics: $V_{CC} = 5.0V \pm 5.0\%$, 0°C T_A 75°C See Figure 7 for test load (switches S1 and S2 are closed unless otherwise specified) typicals are for $V_{CC} = 5V$, $T_{A} = 25$ °C.

SYMBOL	ACCESS PARAMETER	TEST CONDITIONS		S408 TYP	MAX	MIN	'S408-2 TYP	MAX	UNIT
†RICL	RASIN to CAS output delay (Mode 5)	Figure 5a	95	125	160	75	100	130	ns
tRICL	RASIN to CAS output delay (Mode 6)	Figures 5a,5b	80	105	140	65	90	115	ns
tRICH	RASIN to CAS output delay (Mode 5)	Figure 5a	50	63	80	50	63	80	ns
tRICH	RASIN to CAS output delay (Mode 6)	Figures 5a,5b	40	48	60	40	48	60	ns
tRCDL	RAS to CAS output delay (Mode 5)	Figure 5a		98	125		75	100	ns
tRCDL	RAS to CAS output delay (Mode 6)	Figures 5a,5b	100.111 111	78	105	DOB O	65	85	ns
tRCDH	RAS to CAS output delay (Mode 5)	Figure 5a	ar e si	27	40	ha a	27	40	ns
tRCDH	RAS to CAS output delay (Mode 6)	Figure 5a		40	65		40	65	ns
tCCDH	CASIN to CAS output delay (Mode 6)	Figure 5b	40	54	70	40	54	70	ns
tRCV	RASIN to column address valid (Mode 5)	Figure 5a	BINE :	90	120		30	105	ns
tRCV	RASIN to column address valid (Mode 6)	Figure 5a		75	105		70	90	ns
tRPDL	RASIN to RAS delay	Figures 4a,4b,5a,5b	20	27	35	20	27	35	ns
tRPDH	RASIN to RAS delay	Figures 4a,4b,5a,5b	15	23	32	15	23	32	ns
tAPDL	Address input to output low delay	Figures 4a,4b,5a,5b		25	40	10	25	40	ns
tAPDH	Address input to output high delay	Figures 4a,4b,5a,5b		25	40		25	40	ns
tSPDL	Address strobe to address output low	Figure 4b,4a	lgin S-r	40	60	ec es	40	60	ns
tSPDH	Address strobe to address output high	Fibure 4b,4a		40	60		40	60	ns
tWPDL	WIN to WE output delay	Figure 4b	15	25	30	15	25	30	ns
twpph	WIN to WE output delay	Figure 4b	15	30	60	15	30	60	ns
tCPDL	CASIN to CAS delay (RiC) low in Mode 4)	Figure 4b	32	41	58	32	41	58	ns
tCPDH	CASIN to CAS delay	Figure 4b	25	39	50	25	39	50	ns
tRCC	Column select to column address valid	Figure 4a	lose riba	40	58	16 05 mm	40	58	ns
tRCR	Row select to row address valid	Figure 4a,4b	196 5.5 a	40	58	Isl. VC	40	58	ns
tCTL	RF I/O low to counter outputs all low	Figure 2	byeaxe :	on bis	100	No sor	a (586 s)	100	ns
tRFPDL	RASIN to RAS delay during refresh	Figure 2	35	50	70	35	50	70	ns
tRFPDH	RASIN to RAS delay during refresh	Figure 2	30	40	55	30	40	55	ns
tRFLCT	RFSH low to counter address valid	CS = X, Figure 2		47	60		47	60	ns
tRFHRV	RFSH high to row address valid	Figure 2		45	60		45	60	ns
tROHNC	RAS high to new count valid	Figure 2		30	55	12	30	55	ns
tRLEOC	RASIN low to end-of-count low	C _L = 50pF, Figure 2	EOS TAS	6	80	indulper region		80	ns
tRHEOC	RASIN high to end-of-count high	C _L = 50pF, Figure 2			80		Year	80	ns
tRAHI	Row address hold time (Mode 5)	Figure 5a	30		1 9	20			ns
tRAH	Row address hold time (Mode 6)	Figures 5a,5b	20		100	12	1 19		ns
tASC	Column address setup time (Mode 5)	Figure 5a	8	WE	7	3			ns
tASC	Column address setup time (Mode 6)	Figures 5a,5b	6		1	3	E STATE		ns
tRHA	Row address held from column select	Figure 4a	10	- 50	Hoega as	10	15,0 1 28	13	ns
tCRS	Casin setup time to Rasin high (Mode 6)	Figure 5b	35		Film	35			ns

SN74S408/DP8408A SN74S408-2/DP8408A-2

Switching Characteristics: (Cont.)

SYMBOL	ACCESS PARAMETER	TEST CONDITIONS	916 916 754	108	'S408-2	zeelru	UNIT
	cledas and si		MIN TY	MAX	MIN TYP	MAX	
TOAN X 44	THREE-STATE PARAMETER	IONUO ESST	Halama	NAT ZZI	LUUA	1100	120110
^t ZH	CS low to address output high from HI—Z	Figure 7 R1 = 3.5k R2 = 1.5K	aboM) (si- aboM) (Mode	60	EAC of MEAS	60	ns
tHZ	CS high to address output Hi-Z from high	C _L = 15p, Figure 7 R2 = 1k, S1 open	20	40	20	40	ns
TZL	CS low to address output low from Hi-Z	Figure 7 R1 = 3.5k R2 = 1.5k	8 sbold, vs 8 sbold, vs 8 sbold, vs	60	0 8AO of 8AF	60	ns
tLZ 1/8-	CS high to address output Hi-Z from low	C _L = 15pF, Figure 7 R1 = 1k, S2 open	25	50	25	50	ns
THZH	CS low to control output high from Hi-Z high	Figure 7 R2 = 750Ω S1 open	aboM) vabo M) bilev su	80	50	80	ns
tHHZ	CS high to control output Hi-Z high from high	$C_L = 15pF$ Figure 7 $R2 = 750\Omega$, S1 open	vi) blisv aza		MOS OF MISAR	75	ns
tHZL	CS low to control output low from Hi-Z high*	Figure 7, S1, S2 open	45 Yuliab wal		45 tugn 32 9150 A	75	ns
^t LHZ	CS high to control output Hi-Z high from low*	$C_L = 15pF$ Figure 7 $R2 = 750\Omega$ S1 open	sieb dgin 50	80	Address input	80	ms

^{*}Internally the device contains a 3K resistor in series with a Schottky Diode to $V_{\mbox{\footnotesize{CC}}}$.

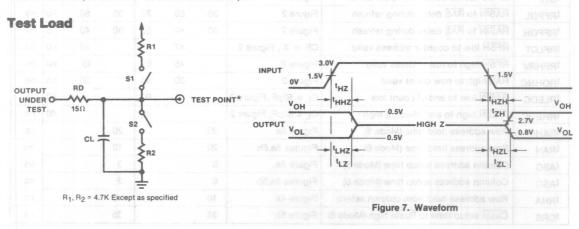
Note 1: Output load capacitance is typical for 4 banks of 22 DRAMs or 88 DRAMs including trace capacitance. These values are: Q0-Q8, WE C_L = 500 pF; RAS C_L = 150 pF; CAS C_L = 600pF unless otherwise noted.

Note 2: All typical values are for $T_A = 25^{\circ}$ and $V_C = 5.0V$.

Note 3: This test is provided as a monitor of driver output source and sink current capability. Caution should be exercised in testing this parameter. In testing these parameters a 15Ω resistor should be placed in series with each output under test. One output should be tested at a time and test time should not exceed 1 second.

Note 4: Input pulse 0V to 3.0V, $t_R = t_F = 2.5$ ns, f = 2.5 MHz, $t_{PW} = 200$ ns. Input reference point on AC measurements is 1.5V. Output reference points are 2.7V for High and 0.8V for Low.

Note 5: The load capacitance on RF I/O should not exceed 50 pF.



^{*} The "TEST POINT" is driven by the output under test, and observed by instrumentation.

256K Dynamic RAM Controller/Driver

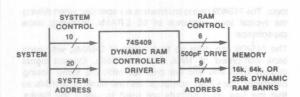
SN74S409-2/DP8409A-2 SN74S409/DP8409A

Features/Benefits

- All DRAM drive functions on one chip have on-chip highcapacitance load drivers (specified up to 88 DRAMs)
- Drives directly all 16K, 64K and 256K DRAMs; capable of addressing up to 1M words
- . Propagation delays of 25 nsec typical at 500 pF load
- Supports READ, WRITE and READ-MODIFY-WRITE cycles
- Eight modes of operation support externally-controlled and automatic access and refresh, as well as special memory initialization access
- On-chip 9-bit refresh counter with selectable End-of-Count (127, 255 or 511)
- Direct replacement for National DP8409, DP8409A

Operating Modes

Externally-controlled fresh
Auto refresh – forced
Automatic burst refresh
AII-RAS auto write
Externally-controlled All-RAS write
Externally-controlled access
Auto access, slow tRAH, hidden refresh
Auto access, fast tRAH
Set end of count

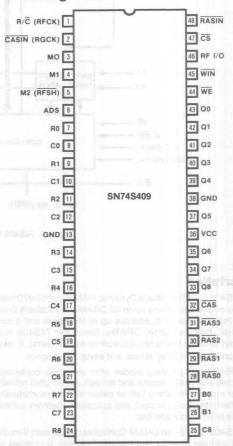


Interface Between System and DRAM Banks

Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
SN74S409	48 N, D	Com
SN74S409-2	48 N, D	Com, Speed Option

Pin Configuration



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TWX: 910-338-2376 TWX: 910-338-2374

Monolithic Memories

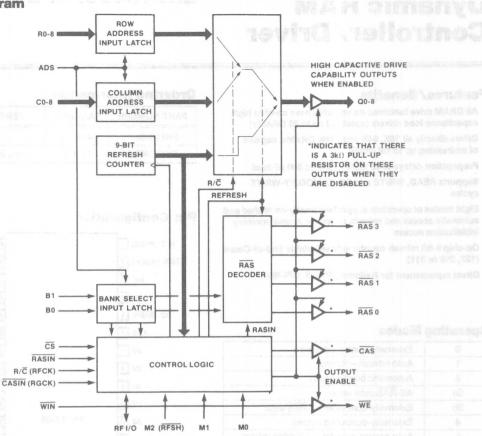


Figure 1. 74S409 Functional Block Diagram

Description

The 74S409 is a Multi-Mode Dynamic RAM Controller/Driver capable of directly driving up to 88 DRAMs. 20 address lines to the 74S409 allow it to address up to 1M words and it can drive 16K, 64K and 256K DRAMs. Since the 74S409 is a one-chip solution (including capacitive-load drivers), it minimizes propagation delay skews, and saves board space.

The 74S409's 8 operating modes offer externally-controlled or on-chip automatic access and refresh. An on-chip refresh counter makes refreshing (either externally or automatically controlled) less complicated; and automatic memory initialization is both simple and fast.

The 74S409 is a 48-pin DRAM Controller/Driver with 9 multiplexed address outputs and 6 control signals. It consists of two 9-bit address latches, a 9-bit refresh counter, and control logic. The 74S409 timing parameters are specified when driving the typical load capitance of 88 DRAMs, including trace capacitance.

The 74S409 can drive up to 4 banks of DRAMs, with each bank comprised of 16Ks, 64Ks or 256Ks. Control signal outputs $\overline{\text{CAS}}$ and $\overline{\text{WE}}$ are provided with the same driving capability. Each $\overline{\text{RAS}}$ output drives one bank of DRAMs so that the four $\overline{\text{RAS}}$ outputs are used to select the banks, while $\overline{\text{CAS}}$, $\overline{\text{WE}}$ and the multiplexed addresses can be connected to all the banks of DRAMs. This leaves the nonselected banks in the standby mode (less than one tenth of the operating power) with the respective data outputs in three-state. Only the bank with its associated $\overline{\text{RAS}}$ low will be written to or read from, except in mode 3 where all $\overline{\text{RAS}}$ signals go low to allow fast memory initialization.

Pin Definitions

 V_{CC} GND, GND – $V_{CC}=5V\pm5\%$. The three supply pins have been assigned to the center of the package to reduce voltage drops, both DC and AC. There are also two ground pins to reduce the low level noise. The second ground pin is located two pins from V_{CC} , so that decoupling capacitors can be inserted directly next to these pins. It is important to adequately decouple this device, due to the high switching currents that will occur when all 9 address bits change in the same direction simultaneously. A recommended solution is a $1\text{-}\mu\text{F}$ multilayer ceramic capacitor in parallel with a low-voltage tantalum capacitor, both connected close to pins 36 and 38 to reduce lead inductance.

DO D	Q. POW	Address	moute

C0-C8: Column Address Inputs.

B0, B1: Bank Select Inputs—Strobed by ADS. Decoded to enable one of the RAS outputs when RASIN goes low, in modes 4-6. In mode 7 B0, B1 are used to define End-of-Count (see table 3), and select mode 3a or 3b.

Q0-Q8: Multiplexed Address Outputs — Selected from the Row Address Input Latch, the Column Address Input Latch, or the Refresh Counter.

RASIN: Row Address Strobe Input — Enables selected RAS_n output when M2 (RFSH) is high (modes 4-6), and all RAS_n outputs in modes 0 and 3. RASIN input is disabled in modes 1 and 2

R/C (RFCK)—In Auto-Refresh Mode this pin is the external Refresh Clock Input: one refresh cycle has to be performed each clock period. In all other modes it is Row/Column Select Input, selecting either the row or column address input latch onto the output bus.

ADS: Address (Latch) Strobe Input – Strobes Input Row Address, Column Address, and Bank Select Inputs into respective latches when high; latches on High-to-Low transition.

CS: Chip Select Input—three-state's the Address Outputs and puts the control signal into a high-impedance logic "1" state when high (unless refreshing in one of the Refresh Modes). Enables all outputs when low.

M0, M1, M2 (RFSH): Mode Control Inputs — These 3 control pins determine the 8 major modes of operation of the 74S409 as depicted in Table 2.

RF I/O RFRQ — This I/O pin functions as a Reset Counter Input when set low from an external open-collector gate, or as a flag output. The flag goes active-low in Modes 0, 2 and

	SELECT D BY ADS)	ENABLED RAS
B1	В0	N. b. a. C. Divilation 3
0	0 0 0	RAS ₀
0	1 1 1	RAS ₁
1	0	RAS ₂
1	1	RAS ₃

Table 1. Memory Bank Decode

3a when the End-of-Count output is at 127, 255, or 511 (see Table 3). In Auto-Refresh Mode (mode 5) it is the $\overline{\text{Refresh}}$ Request (RFRQ) output.

WIN: Write Enable Input.

WE: Write Enable Output - Buffered output from WIN.

CAS: Column Address Strobe Output — In Modes 3a, 5, and 6, CAS transitions low following valid column address. In Modes 3b and 4, it goes low after R/C goes low, or follows CASIN going low if R/C is already low. CAS is high during refresh.

RAS 0-3: Row Address Strobe Outputs—When M2(RFSH) is high (modes 4-6), the selected row address strobe output (decoded from signals B0, B1) follows the RASIN input. When M2 (RFSH) is low (modes 0-3) all RAS_n outputs go low together following RASIN going low in modes 0 and 3 and automatically in modes 1 and 2.

Input Addressing

The address block consists of a row-address latch, a column-address latch, and a resettable refresh counter.

The address latches are fall-through when ADS is high and latch when ADS goes low. If the address bus contains valid address until after the valid address time, ADS can be permanently high. Otherwise ADS must go low while the address is still valid.

In normal memory-access operation, $\overline{\text{RASIN}}$ and $\overline{\text{R/C}}$ are initially high. When the address inputs are enabled into the address latches (modes 3-6) the row addresses appear on the Q outputs. The Address Strobe also inputs the bank-select address, (B0 and B1). If $\overline{\text{CS}}$ is low, all outputs are enabled. When $\overline{\text{CS}}$ goes high, the address outputs go three-state and the control outputs first go high through a low impedance, and then are held by an on-chip high impedance. This allows output paralleling with other 74S409s for multi-addressing. All outputs go active about 50ns after the chip is selected again. If $\overline{\text{CS}}$ is high, and a refresh cycle begins, all the outputs become active until the end of the refresh cycle.

Drive Capability

The 74S409 has timing parameters that are specified with up to 600pF loads for $\overline{\text{CAS}}$ and $\overline{\text{WE}}$, 500pF loads for Q_0 - Q_8 , and 150pF loads for $\overline{\text{RAS}}_n$ outputs. In a typical memory system this is equivalent to about 88 5V-only DRAMs, with trace lengths kept to a minimum. Therefore, the chip can drive four banks each of 16 or 22 bits, or two banks of 32 or 39 bits, or one bank of 64 or 72 bits.

Less loading will slightly reduce the timing parameters, and more loading will increase the timing parameters, according to the graph of Figure 14. The AC performance parameters are specified with the typical load capacitance of 88 DRAMs. This graph can be used to extrapolate the variations expected with other loading.

74S409 Driving Any 16K, 64K or 256K DRAMs

The 74S409 can drive any 16K, 64K, or 256K DRAMs. The on-chip 9-bit counter with selectable End-of-Count can support refresh of 128, 256 and 512 rows, while the 9 address and 4 $\overline{\text{AAS}}_{\text{n}}$ outputs can address 4 banks of 16K, 64K or 256K DRAMs.

Read, Write, and Read-Modify-Write Cycles

The output signal, \overline{WE} , determines what type of memory access cycle the memory will perform. If \overline{WE} is kept high while \overline{CAS} goes low, a read cycle occurs. If \overline{WE} goes low

before $\overline{\text{CAS}}$ goes low, a write cycle occurs and data at DI (DRAM input data) is written into the DRAM as $\overline{\text{CAS}}$ goes low. If $\overline{\text{WE}}$ goes low later than t_{CWD} after $\overline{\text{CAS}}$ goes low, first a read occurs and DO (DRAM output data) becomes valid; then data DI is written into the same address in the DRAM when $\overline{\text{WE}}$ goes low. In this read-modify-write case, DI and DO cannot be linked together. The type of cycle is therefore controlled by $\overline{\text{WE}}$, which follows $\overline{\text{WIN}}$.

Power-Up Initialize

When V_{CC} is first applied to the 74S409, an internal pulse clears the refresh counter, the internal control flip-flops, and sets the End-of-Count of the refresh counter to 127 (which may be changed via Mode 7). As V_{CC} increases to about 2.3 volts, it holds the output control signals at a level of one Schottky diode-drop below V_{CC} , and the output address to three-state. As V_{CC} increases above 2.3 volts, control of these outputs is granted to the system.

74S409 Functional Modes Description

The 74S409 operates in 8 different functional modes selected by signals M₀,M₁,M₂. Mode 3 splits further to modes 3a and 3b determined by signals B₀,B₁ in mode 7.

Mode 0 and mode 1 are generally used as Refresh modes for mode 4 and mode 5 respectively, and therefore will be described as mode-pairs 0,4 and 1,5.

Mode 6 is a fast access made for very fast DRAMs and mode 7 is used only to determine choice of mode 3a or 3b and for setting End-of-Count for the refresh modes.

MODE	(RFSH) M2	M1	МО	MODE OF OPERATION	CONDITIONS
0	0	0	0	Externally-controlled refresh	RF I/O = EOC
. Income	0	0	1	Auto refresh – forced	$RFI/O = Refresh request (\overline{RFRQ})$
2	ad A One	-1	0	Automatic burst refresh	$RFI/O = \overline{EOC}$
3a*	0	1	IA pate	All-RAS auto write	RF I/O = EOC; all RAS active
3b*	0	1	1	Externally-controlled All-RAS write	All-RAS active
4	1	0	0	Externally-controlled access	Active RAS defined by Table 2
5	ere e 1 hn w	0	1	Auto access, slow t _{RAH} , hidden refresh	Active RAS defined by Table 2
6	um ni 1 ,857 s	dent :	0	Auto access, fast tRAH	Active RAS defined by Table 2
7	that seattle de-	11	1	Set end of count; determines mode 3a or 3b	See Table 3 for Mode 7

^{*}Mode 3a is selected by setting B₀,B₁ to 01, 00, or 10 in mode 7.

*Mode 3b is selected by setting B₁,B₀ to 11 in mode 7.

Table 2. 74S409 Mode Select Options

Mode 0 — Externally-Controlled Refresh Mode 4 — Externally-Controlled Access

Modes 0 and 4 facilitate external control of all timing parameters associated with the DRAMs. These modes are independent modes of operation though generally used together in the same application as shown in Figure 2.

Mode O—Externally-Controlled Refresh

In this mode the input address latches are disabled from the address outputs and the refresh counter is enabled. All $\overline{\text{RAS}}$ outputs go low following $\overline{\text{RASIN}}$ and refresh the enabled row in all four banks. $\overline{\text{CASIN}}$ and $\overline{\text{R/C}}$ inputs are not used and $\overline{\text{CAS}}$ is inhibited. The refresh counter increments when either $\overline{\text{RASIN}}$ or M2 ($\overline{\text{RFSH}}$) switch high while the other is still low.

RF I/O goes low when the count equals End-of-Count (as set in mode 7), and $\overline{\text{RASIN}}$ is low. The 9-bit counter will always roll-over to zero at 512, regardless of End-of-Count. However, the counter can be reset at any time by driving RF I/O low through an external open-collector.

During refresh, $\overline{\text{RASIN}}$ and M2 (RFSH) can transition low simultaneously because the refresh counter becomes valid on the output bus t_{RFLCT} after $\overline{\text{RFSH}}$ goes low, which is a shorter time than t_{RFPDL} . This means the counter address is valid on the Q outputs before $\overline{\text{RAS}}$ occurs on all $\overline{\text{RAS}}$ outputs, strobing the counter address into that row of all the DRAMs (see Figure 2.). To perform externally-controlled burst refresh, $\overline{\text{RFSH}}$ initially can again have the same edge as $\overline{\text{RASIN}}$, but then maintains a low state, since $\overline{\text{RASIN}}$ going low-to-high increments the counter (performing the burst refresh).

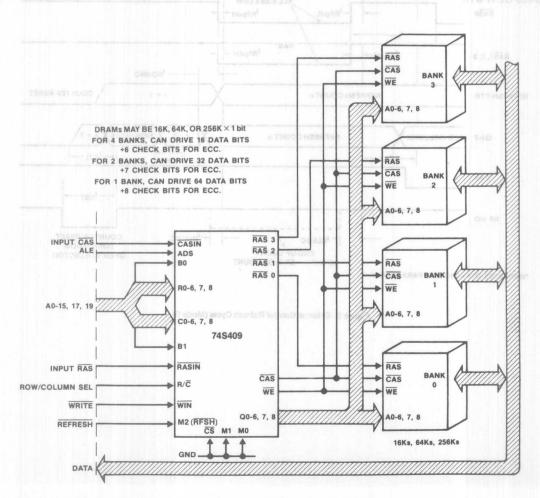


Figure 2. Typical Application of 74S409 Using Externally-Controlled Access and Refresh in Modes 0 and 4

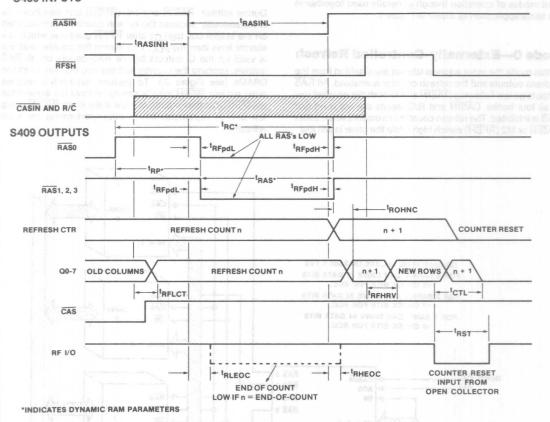


Figure 3. External Control Refresh Cycle (Mode 0)

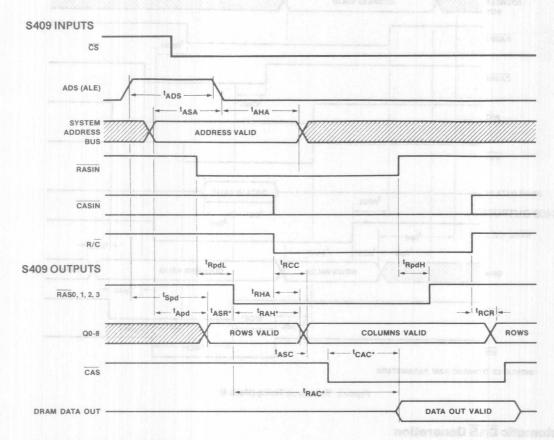
Mode 4 — Externally-Controlled Access

This mode facilitates externally controlling all access-timing parameters associated with the DRAMs. Figures 4 and 5 show the timing for read and write cycles.

Output Address Selection

In this mode \overline{CS} has to be low at least 50 nsec before the outputs will be valid. With R/\overline{C} high, the row address latch

contents are transfered to the multiplexed address bus output Q0-Q8. $\overline{\text{RASIN}}$ can go low after the row addresses have been set up on Q0-Q8, and enables one $\overline{\text{RAS}}$ output selected by signals B0, B1 to strobe the Q outputs into the desired bank of memory. After the row-address hold-time of the DRAMs, $\overline{\text{R/C}}$ can go low so that about 40 nsec later, the column address appears on the Q output.



*INDICATES DYNAMIC RAM PARAMETERS

Figure 4. Read Cycle Timing (Mode 4)

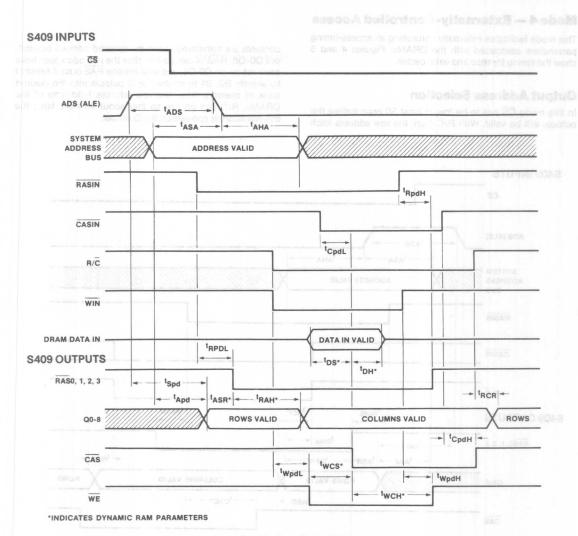


Figure 5. Write Cycle Timing (Mode 4)

Automatic CAS Generation

In a normal memory access cycle $\overline{\text{CAS}}$ can be derived from inputs $\overline{\text{CASIN}}$ or R/C. If $\overline{\text{CASIN}}$ is high, then R/C going low switches the address output drivers from rows to columns. $\overline{\text{CASIN}}$ then going low causes $\overline{\text{CAS}}$ to go low approximately 40 ns later, allowing $\overline{\text{CAS}}$ to occur at a predictable time (see Figure 5). For maximum system speed, $\overline{\text{CASIN}}$ can be kept low, since $\overline{\text{CAS}}$ will automatically occur approximately 60 ns after R/ $\overline{\text{C}}$ goes low (see Figure 4). Most DRAMs have a column address set-up time before $\overline{\text{CAS}}$ (tASC) of 0 ns or -10 ns. In other words, a tASC greater than 0 ns is safe. This

feature reduces timing-skew problems, thereby improving access time of the system.

Fast Memory Access

For faster access time, R/ \overline{C} can go low a time delay (tRPDL + tRAH - tRHA) after \overline{RASIN} goes low, where tRAH is the Row-Address hold-time of the DRAM, and \overline{CASIN} can go low tRCC - tCPOL + tASC (min.) after R/ \overline{C} goes low (see tDiF1, tDiF2 switching characteristics).

Mode 1 — Automatic Forced Refresh Mode 5 — Automatic Access with Hidden Refresh

Mode 1 and Mode 5 are generally used together incorporating the advantages of the "hidden refresh" performed in mode 5 with the possibility to force a refresh by changing to mode 1. An advantage of the Automatic Access over the Externally-Controlled Access is the reduced memory access time, due to the fact that the output control signals are derived internally from one input signal (RASIN).

Hidden and Forced Refresh

Hidden Refresh is a term describing memory refresh performed when the system does not access the portion of memory controlled by the 74S409 ($\overline{CS}=1$). A hidden refresh will occur once per Refresh Clock (RFCK) cycle provided \overline{CS} went high and \overline{RASIN} went low. If no hidden refresh occurred while RFCK was high, the RF I/O (\overline{RFRQ}) goes low immediately after RFCK goes low, indicating to the system when a forced refresh is required. The system must allow a forced refresh to take place while RFCK is low by driving M2 (\overline{RFSH}) low, thereby changing mode of operation to Mode 1.

The Refresh Request on RF I/O (RFRQ) is terminated as soon as RAS goes low, indicating to the system that the foced refresh has been done. The system should then drive M2 (RFSH) high, changing the mode of operation back to Mode 5 (see Figure 6).

Mode 1 - Automatic Forced Refresh

In Mode 1, the R/\(\overline{C}\) (RFCK) pin functions as RFCK (refresh cycle clock) instead of R/\(\overline{C}\), and \(\overline{CAS}\) remains high. If RFCK is kept permanently high then whenever M2 (\overline{RFSH}) goes

low, an externally-controlled refresh will occur and all $\overline{\text{RAS}}$ outputs will follow $\overline{\text{RASIN}}$, strobing the refresh counter contents to the DRAMs. The RF I/O pin will always output high, but can be set low externally through an open-collector driver to reset the refresh counter.

If RFCK is an input clock, one and only one refresh cycle must take place every RFCK cycle. If a hidden refresh does not occur while RFCK is high, in Mode 5, then RF I/O (Refresh Request) goes low immediately after RFCK goes low, indicating to the system that a forced refresh is required. The system must allow a forced refresh to take place while RFCK is low The Refresh Request signal on RF I/O may be connected to a Hold or Bus Request input to the system. The system acknowledges the Hold or Bus Request when ready, and outputs Hold Acknowledge or Bus Request Acknowledge. If this is connected to the M2 (RFSH) pin, a forced-refresh cycle will be initiated by the S409, and RAS will be internally generated on all four RAS outputs, strobing the refresh counter contents on the address ouputs into all the DRAMs. An external RAS Generator Clock (RGCK) is required for this function. It is fed to the CASIN (RGCK) pin, and may be up to 10 MHz. Whenever M2 goes low (inducing a forced refresh), RAS remains high for one to two periods of RGCK, depending on when M2 goes low relative to the highto-low triggering edge of RGCK; RAS then goes low for two periods, performing a refresh on all banks. In order to obtain the minimum delay from M2 going low to RAS going low, M2 should go low tRESBG before the next falling edge of RGCK. The Refresh Request on RF I/O is terminated as RAS begins. so that by the time the system has acknowledged the removal of the request and disabled its Acknowledge, (i.e., M2 goes high), Refresh RAS will have ended, and normal operations can begin again in the Automatic Access mode (Mode 5). If it is desired that Refresh RAS end in less than 2 periods of RGCK from the time RAS went low, then M2 may go high earlier than tFRQH after RF I/O goes high and RAS will go high tRFRH after M2.

mode 5 – Automatic Access with Hidden Refresh

In this mode all address outputs, RAS and CAS are initiated from RASIN making the DRAM access appear similar to static RAM access. The hidden refresh feature enables DRAM refresh accomplished with no time-loss to the system.

Provided the input address is valid as ADS goes low, RASIN can go low any time after ADS. This is because the selected RAS occurs typically 27 ns later, by which time the row address is already valid on the address output of the 74S409. The Address Set-Up time (tASR), is 0 ns on most DRAMs. The 74S409 in this mode (with ADS and RASIN edges simultaneously applied) produces a minimum tASR of 0 ns. This is true provided the input address was valid tASR before ADS went low (see Figure 7).

Next, the row address is disabled t_{RAH} after RAS goes low (30 ns minimum); in most DRAMs, t_{RAH} minimum is less than 30 ns. The column address is then set up and (t_{ASC} later,) CAS occurs. The only other control input required is WIN. When a write cycle is required, WIN must go low at least 30 ns before CAS is output low.

This gives a total typical delay from: input address valid to RASIN (15 ns); to RAS (27 ns); to rows held (50 ns); to columns valid (25 ns); to CAS (23 ns) = 140 ns (that is, 125 ns from RASIN). All of these typical figures are for heavy capacitive loading, of approximately 88 DRAMs.

Refreshing

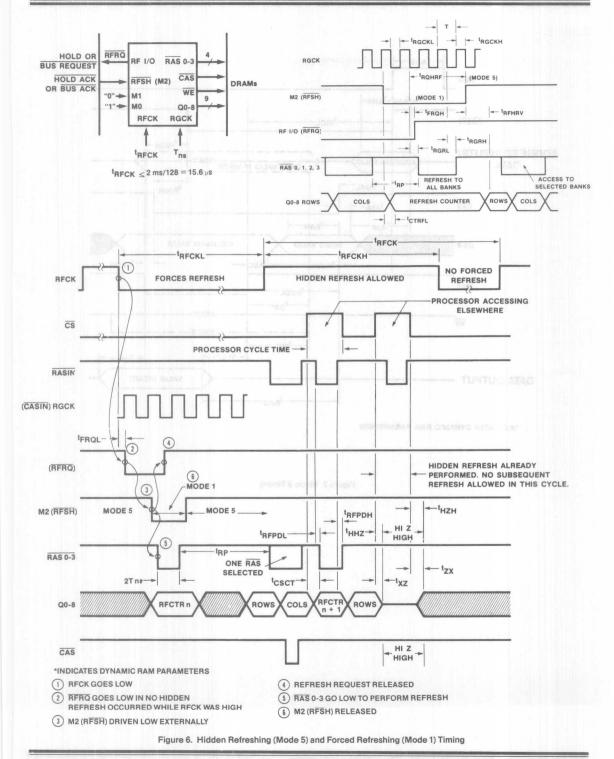
In this mode R/Č (RFCK) functions as Refresh Clock and CASIN (RGCK) functions as RAS Generator Clock.

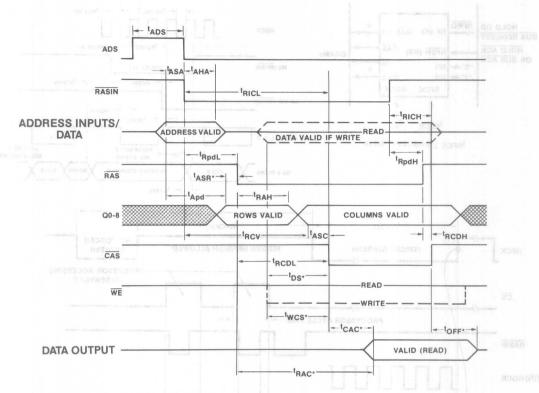
One refresh cycle must occur during each refresh clock period, and then the refresh address must be incremented before the next refresh cycle. As long as 128 rows are refreshed every 2 ms (one row every 16 μ s), all 16K and 64K DRAMs will be correctly refreshed. The cycle time of RFCK must, therefore, be less than 16 μ s. RFCK going high sets an internal refresh-request flipflop. First the 74S409 will attempt to perform a hidden refresh so that the system thruput will not be affected. If, during the time RFCK

is high, \overline{CS} on the 74S409 goes high and \overline{RASIN} occurs, a hidden refresh will occur. In this case, \overline{RASIN} should be considered a common read/write strobe. In other words, if the processor is accessing elsewhere (other than the DRAMs) while RFCK is high, the 74S409 will perform a refresh. The refresh counter is enabled to the address outputs whenever \overline{CS} goes high with RFCK high, and all \overline{RAS} outputs follow \overline{RASIN} . If a hidden refresh is taking place as RFCK goes low, the refresh continues. At the start of the hidden refresh, the refresh-request flipflop is reset so on further refresh can occur until the next RFCK period starts with the positive-going edge of RFCK (see Figure 6). \overline{RASIN} should go low at least 20 ns before RFCK goes low, to ensure occurrence of the hidden refresh.

To determine the probability of a hidden refresh occurring, goes low, (and the internal-request flipflop has not been for $8\mu s$, then the system has 20 chances to not select the 74S409. If during this time a hidden refresh did not occur, then the 74S409 forces a refresh while RFCK is low, but the system chooses when the refresh takes place. After RFCK goes low, (and the internal-request flip-flop has not been reset), RF I/O goes low indicating that a refresh is requested to the system. Only when the system acknowledges this request by setting M2 (RFSH) low does the 74S409 initiate a forced refresh (which is performed automatically). Refer to Mode 1, and Figure 6. The internal refresh request flipflop is then reset.

Figure 6 illustrates the refresh alternatives in Mode 5. If a hidden refresh has occurred and \$\overline{\text{CS}}\$ again goes high before RFCK goes low, the chip is deselected. All the control signals go high-impedance high (logic "1") and the address outputs go three-state until \$\overline{\text{CS}}\$ again goes low. This mode (combined with Mode 1) allows very fast access, and automatic refreshing (possibly not even slowing down the system), with no extra ICs. Careful system design can, and should, provide a higher probability of hidden refresh occurring. The duty cycle of RFCK need not be 50 percent; in fact, the low-time should be designed to be a minimum. This is determined by the worst-case time (required by the system) to respond to the 74S409's forced-refresh request.





*INDICATES DYNAMIC RAM PARAMETERS

Figure 7. Mode 5 Timing

Mode 2 - Automatic Burst Refresh

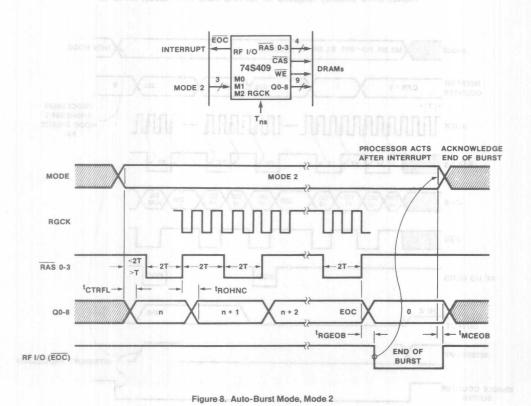
This mode is normally used before and/or after a DMA operation to ensure that all rows remain refreshed, provided the DMA transfer takes less than 2 ms (see Figure 8). When the 74S409 enters this mode, CASIN (RGCK) becomes the RAS Generator Clock (RGCK), and RASIN is disabled. CAS remains high, and RF I/O goes low when the refresh counter has reached the selected End-of-Count and the last RAS has ended. RF I/O then remains low until the Auto-Burst Refresh mode is terminated. RF I/O can therefore be used as an interrupt to indicate the End-of-Burst condition.

The signal on all four \overline{RAS} outputs is just a divide-by-four of RGCK; in other words, if RGCK has a 100 ns period, \overline{RAS} is high and low for 200 ns each cycle. The refresh counter increments at the end of each \overline{RAS} , starting from the count it contained when the mode was entered. If this was zero then for a RGCK with a 100 ns period with End-of Count set to 127, RF I/O will go low after $128 \times 0.4 \mu s$, or $51.2 \mu s$. During this time, the system may be performing operations that do not involve DRAM. If all rows need to be burst refreshed, the refresh counter may be cleared by setting RF I/O low externally before the burst begins.

Burst-mode refreshing is also useful when powering down systems for long periods of time, but with data retention still required while the DRAMs are in standby. To maintain valid refreshing, power can be applied to the 74S409 (set to Mode 2), causing it to perform a complete burst refresh. When end-of-bust occurs (after 26 µs), power can then be removed from the 74S409 for 2 ms, consuming an average power of 1.3% of normal operating power. No control signal glitches occur when switching power to the 74S409.

Mode 3a - All-RAS Automatic Write

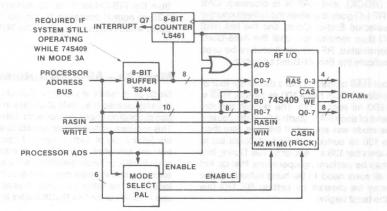
Mode 3a is useful at system initialization, when the memory is being cleared (i.e., with all-zeroes in the data field and the corresponding check bits for error detection and correction). This requires writing the same data to each location of memory (every row of each column of each bank). All \overline{RAS} outputs are activated, as in refresh, and so are \overline{CAS} and \overline{WE} . To write to all four banks simultaneously, every row is strobed in each column, in sequence, until data has been written to all locations. The refresh counter is used to address the rows, and \overline{RAS} is low for two RGCK cycles and high for two cycles.



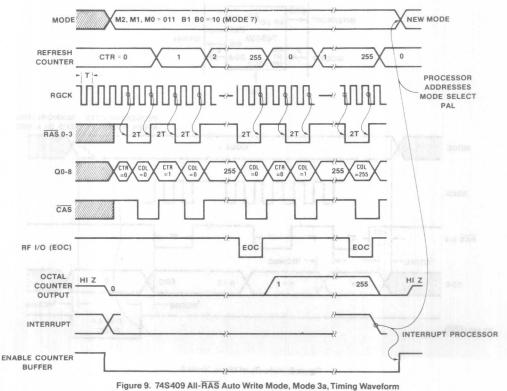
Monolithic III Memories

To select this mode, B1 and B0 must have previously been set to 00, 01, or 10 in Mode 7, depending on the DRAM size. For example, for 16K DRAMs, B1 and B0 are 00. For 64K DRAMs, B1 and B0 are 01.

low, and CASIN (RGCK) becomes RGCK. RF I/O goes low whenever the refresh counter is 127, 255, or 511 (as set by End-of-Count in Mode 7), and the RAS outputs are active.



74S409 Extra Circuitry Required for All-RAS Auto Write Mode, Mode 3a



Mode 3b — Externally-Controlled All-RAS Write

To select this mode, B1 and B0 must first have been set to 11 in Mode 7. This mode is useful at system initialization, but under processor control. The memory address is provided by the processor, which also performs the incrementing. All four RAS outputs follow RASIN (supplied by the processor), strobing the row address into the DRAMs. R/C can now go low, while CASIN may be used to control CAS (as in the Externally-Controlled Access mode), so that CAS strobes the column address contents into the DRAMs. At this time WE should be low causing the data to be written into all four banks of DRAMs. At the end of the write cycle, the input address is incremented and latched by the 74S409 for the next write cycle. This method is slower than Mode 3a, since the processor must perform the incrementing and accessing. Thus the processor is occupied during RAM initialization, and is not free for other initialization operations. However, initialization sequence timing is under system control, which may provide some system advantage.

Mode 4 — Externally-Controlled Access

Mode 4 is described in with mode 0 in section "Mode 0 and Mode 4."

Mode 5 – Automatic Access with Hidden Refresh

See description of mode 0 and mode 5.

Mode 6 - Fast Automatic Access

The Fast Automatic Access mode can only be used with fast DRAMs which have t_{RAH} of 10 nsec-15nsec. The typical RASIN to \overline{CAS} delay is 105nsec. In this mode \overline{CAS} can be extended after \overline{RAS} goes high to extend the data output valid time. This feature is useful in applications with short cycles where \overline{RAS} has to be terminated as soon as possible to meet the precharge (t_{RP}) requirements of the DRAM.

Mode 6 timing is illustrated in Figures 10 and 11. Provided that the input address is valid as ADS goes low, \overline{RASIN} can go low any time after ADS. This is because the selected \overline{RAS} occurs typically 27 ns later, by which time the row address is already valid on the address output of the 74S409. The Address

Set-Up time (t_{ASR}), is 0 ns on most DRAMs. The 74S409 in this mode (with ADS and \overline{RASIN} edges simultaneously applied) produces a minimum t_{ASR} of 0 ns. This is true provided the input address was valid t_{ASA} before ADS went low (see Figure 10).

Next, the row address is disabled t_{RAH} after \overline{RAS} goes low (20 ns minimum); the column address is then set up and t_{ASC} later, \overline{CAS} occurs. The only other control input required is \overline{WIN} . When a write cycle is required, \overline{WIN} must go low at least 30 ns before \overline{CAS} is output low.

This gives a total typical delay from: input address valid to RASIN (15 ns); to RAS (27 ns): to rows valid (50 ns); to columns valid (25 ns); to CAS (23 ns) = 140 ns (that is, 125 ns from RASIN). All of these typical figures are for heavy capacitive loading, of approximately 88 DRAMs.

This mode is therefore extremely fast. The external timing is greatly simplified for the memory system designer: the only system signal required is RASIN.

In this mode, the R/C (RFCK) pin is not used, but CASIN (RGCK) is used as CASIN to allow an extended CAS after RAS has already terminated. Refer to Figure 11.

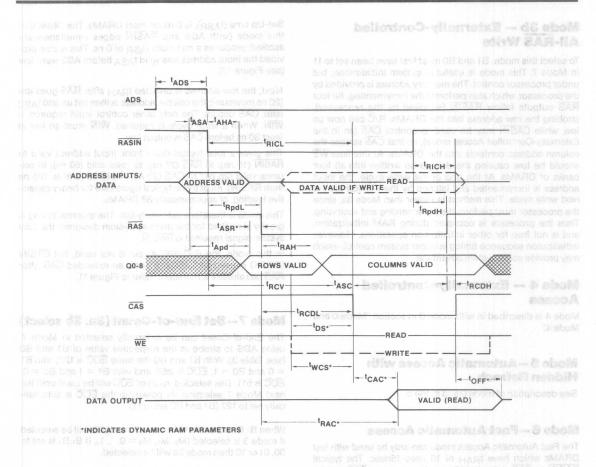
Mode 7 - Set End-of-Count (3a, 3b select)

The End-of-Count can be externally selected in Mode 7, using ADS to strobe in the respective value of B1 and B0 (see Table 3). With B1 and B0 the same $\overline{\text{EOC}}$ is 127; with B1 = 0 and B0 = 1, $\overline{\text{EOC}}$ is 255; and with B1 = 1 and B0 = 0, $\overline{\text{EOC}}$ is 511. This selected value of $\overline{\text{EOC}}$ will be used until the next Mode 7 selection. At power-up the $\overline{\text{EOC}}$ is automatically set to 127 (B1 and B0 set to 11).

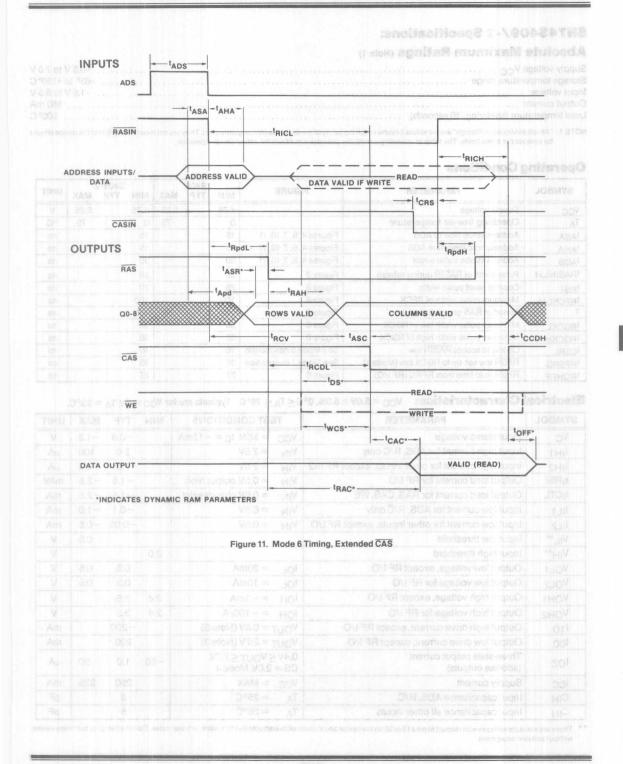
When B_1, B_2 are set to 11 in mode 7, mode 3b will be selected if mode 3 is selected (M_2 , M_1 , $M_0=0$, 1, 1). If B_1, B_2 is set to 00, 01 or 10 then mode 3a will be selected.

	SELECT D BY ADS)	END OF COUNT
B1	В0	SELECTED
0	0	127
0	1	255
1	0	511
1	1	127

Table 3. Mode 7



END OF COUNT	BLECT BY ADS)	Figure 10. Mode	6 Timing (CASIN High) because in the first sector and a first sector with short with short sector with sector with short sector with sector with short sector with
			next the precharge (tpp) requirements of the BRAM.
127			ypically 27 nalator by which time the row address is already



SN74S409/-2 Specifications:

Absolute Maximum Ratings (Note 1)

Supply voltage V _{CC}	-0.5 V to 7.0 V
Storage temperature range	-65° to +150° C
Input voltage	-1.5 V to 5.5 V
Output current	150 mA
Lead temperature (soldering, 10 seconds)	300°C

NOTE 1: "Absolute Maximum Ratings" are the values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of operating conditions provides conditions for actual device operation.

Operating Conditions

SYMBOL	PARAMETER	FIGURE	MIN TYP MAX		MIN	UNIT			
VCC	Supply voltage		4.75		5.25	4.75		5.25	V
TA	Operating free-air temperature		0		75	0	80.5	75	°C
tASA	Address setup time to ADS	Figures 4, 5, 7, 10, 11	15			15			ns
^t AHA	Address hold time from ADS	Figures 4, 5, 7, 10, 11	15			15	OT6	91110	ns
tADS	Address strobe pulse width	Figures 4, 5, 7, 10, 11	30	1	-	30			ns
trasinl,H	Pulse width of RASIN during refresh	Figure 3	50			50			ns
tRST	Counter reset pulse width	Figure 3	70			70			ns
tRFCKL,H	Minimum pulse width of RFCK	Figure 6	100		110000	100			ns
T SS	Period of RAS generator clock	Figure 6	100			100			ns
†RGCKL	Minimum pulse width low of RGCK	Figure 6	35		5.5.0003	35			ns
trgckh tr	Minimum pulse width high of RGCK	Figure 6	35			35			ns
tCSRL	CS low to access RASIN low	See Mode 5 description	n 10			10			ns
treskg	RFSH low set-up to RGCK low (Mode 1)	See Mode 1 description	n 35			35			ns
trohrf.	RFSH hold time from RFRQ (RF I/O)	Figure 6	2T			2T			ns

Electrical Characteristics: $V_{CC} = 5.0V \pm 5.0\%$, $0^{\circ}C \le T_{A} \le 75^{\circ}C$ Typicals are for $V_{CC} = 5V$, $T_{A} = 25^{\circ}C$.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VC	Input clamp voltage	$V_{CC} = MIN, I_C = -12mA$		-0.8	-1.2	V
IH1	Input high current for ADS, R/C only	V _{IN} = 2.5V	VIII	2.0	100	μА
I _I H2	Input high current for other inputs, except RF I/O	V _{IN} = 2.5V		1.0	50	μΑ
I _I RSI	Output load current for RF I/O	V _{IN} = 0.5V, output high		-1.5	-2.5	mAV
IJCTL	Output load current for RAS, CAS, WE	V _{IN} = 0.5V, chip deselct	RADIVE	-1.5	-2.5	mA
IIL1	Input low current for ADS, R/C only	V _{IN} = 0.5V		-0.1	-1.0	mA
I _I L2	Input low current for other inputs, except RF I/O	V _{IN} = 0.5V		-0.05	-0.5	mA
VIL**	Input low threshold	Substill Property			0.8	V
VIH**	Input high threshold		2.0			V
VOL1	Output low voltage, except RF I/O	IOL = 20mA		0.3	0.5	V
VOL2	Output low voltage for RF I/O	IOL = 10mA		0.3	0.5	V
VOH1	Output high voltage, except RF I/O	$I_{OH} = -1mA$	2.4	3.5		V
VOH2	Output high voltage for RF I/O	$IOH = -100\mu A$	2.4	3.5		V
I _{1D}	Output high drive current, except RF I/O	V _{OUT} = 0.8V (Note 3)		-200	No Personal	mA
loD	Output low drive current, except RF I/O	V _{OUT} = 2.7V (Note 3)		200		mA
loz	Three-state output current (address outputs)	0.4V ≤ V _{OUT} ≤ 2.7V, CS = 2.0V, Mode 4	-50	1.0	50	μΑ
Icc	Supply current	V _{CC} = MAX		250	325	mA
CIN	Input capacitance ADS, R/C	T _A = 25°C		8		pF
CIN	Input capacitance all other inputs	T _A = 25°C		5		pF

^{**} These are absolute voltages with respect to pins 13 or 38 on the device and include all overshoots due to system or tester noise. Do not attempt to test these values without suitable equipment.

Switching Characteristics: $V_{CC} = 5.0V \pm 5.0\%$, $0^{\circ}C \le T_{A} \le 75^{\circ}C$ See Figure 12 for test load (switches S1 and S2 are closed unless otherwise specified) typicals are for $V_{CC} = 5V$, $T_{A} = 25^{\circ}C$.

SYMBOL	ACCESS PARAMETER	FIGURE	MIN	'S409 TYP	MAX	MIN	'S409-2	MAX	UNIT
tRHA	Row address held from column select	Figure 4	10	100		10			ns
tRICL	RASIN to CAS output delay (Mode 5)	Figures 7, 10	95	125	160	75	100	130	ns
tRICL	RASIN to CAS output delay (Mode 6)	Figures 7, 10, 11	80	105	140	65	90	115	ns
tRICH	RASIN to CAS output delay (Mode 5)	Figures 7, 10	50	63	80	50	63	80	ns
tRICH	RASIN to CAS output delay (Mode 6)	Figures 7, 10, 11	40	48	60	40	48	60	ns
tRCDL	RAS to CAS output delay (Mode 5)	Figures 7, 10		98	125		75	100	ns
tRCDL	RAS to CAS output delay (Mode 6)	Figures 7, 10, 11	a mort S	78	105	DE N	65	85	ns
tRCDH	RAS to CAS output delay (Mode 5)	Figures 7, 10	THE STATE OF	27	40		27	40	ns
tRCDH	RAS to CAS output delay (Mode 6)	Figures 7, 10		40	65	BHILE	40	65	ns
tCCDH	CASIN to CAS output delay Mode 6)	Figure 11	40	54	70	40	54	70	ns
tRCV	RASIN to column address valid (Mode 5)	Figures 7, 10		90	120	HI (E	80	105	ns
tRCV	RASIN to column address valid (Mode 6)	Figures 7, 10, 11	2840	75	105	nee p	70	90	ns
†RPDL	RASIN to RAS delay	Figures 4, 5, 7, 10, 11	20	27	35	20	27	35	ns
treph treph	RASIN to RAS delay	Figures 4, 5, 7, 10, 11	15	23	32	15	23	32	ns
†APDL	Address input to output low delay	Figures 4, 5, 7, 10, 11		25	40		25	40	ns
t _{APDH}	Address input to output high delay	Figures 4, 5, 7, 10, 11		25	40	- Park	25	40	ns
tSPDL	Address strobe to address output low	Figures 4, 5	of to eat	40	60	e Goral	40	60	ns
tSPDH	Address strobe to address output high	Figures 4, 5	\$40-000 (8)	40	60	District Co.	40	60	ns
tWPDL	WIN to WE output delay	Figure 5	15	25	30	15	25	30	ns
tWPDH	WIN to WE output delay	Figure 5	15	30	60	15	30	60	ns
tCRS	CASIN setup time to RASIN high (Mode 6)	Figure 11	35	el hasso	1876 ±C	35	and the ST	X do as	ns
tCPDL	CASIN to CAS delay (R/C low in Mode 4)	Figure 5	32	41	58	32	41	58	ns
tCPDH	CASIN to CAS delay	Figure 5	25	39	50	25	39	50	ns
tRCC	Column select to column address valid	Figure 4	HMad	40	58	at 100	40	58	ns
tRCR	Row select to row address valid	Figures 4, 5	B RUSING	40	58	Laon.	40	58	ns
tRAH	Row address hold time (Mode 5)	Figures 7, 10	30		10.7	20			ns
tRAH	Row address hold time (Mode 6)	Figures 7, 10, 11	20	0	v8.	12		沙德克	ns
tASC	Column address setup time (Mode 5)	Figures 7, 10	8			3			ns
tASC	Column address setup time (Mode 6)	Figures 7, 10, 11	6	SWE.		3			ns
t _{DiF1}	Maximum (t _{RPDL} - t _{RHA}) (Mode 4)				15			15	ns
tDiF2	Maximum (t _{RCC} - t _{CPDL}) (Mode 4)				15			15	ns

SYMBOL	REFRESH PARAMETER	TEST CONDITIONS	MIN	'S409 TYP	MAX	MIN	'S409-2	MAX	UNIT
tFRQL	RFCK low to forced RFRQ low	C _L = 50 pF, Figure 6		20	30		20	30	ns
tFRQH	RGCK low to force RFRQ high	C _L = 50pF, Figure 6		50	75	100	50	75	ns
tRGRL	RGCK low to RAS low	Figure 6	50	65	95	50	65	95	ns
tRGRH	RGCK low to RAS high	Figure 6	40	60	85	40	60	85	ns
t _{RFRH}	RFSH high to RAS high (encoding forced RFSH)	See Mode 1 description	55	80	110	55	80	110	ns
tCSCT	CS high to RFSH counter valid	Figure 6	1 - 1 3	55	70	A YES	55	70	ns
tCTL	RF I/O low to counter outputs all low	Figure 3	en sett se	nakimi e	100	WO. T	90ET #	100	ns
†RFPDL	RASIN to RAS delay during refresh	Figures 3, 6	35	50	70	35	50	70	ns
tRFPDH	RASIN to RAS delay during refresh	Figures 3, 6	30	40	55	30	40	55	ns
trelct.	RFSH low to counter address valid	CS = X, Figures 3, 6, 8		47	60	-	47	60	ns
tREHRV	RFSH high to row address valid	Figures 3, 6		45	60		45	60	ns
tROHNC	RAS high to new count valid	Figures 3, 8		30	55	E.H	30	55	ns
†RLEOC	RASIN low to end-of-count low	C _L = 50pF, Figure 3			80		11/10/19	80	ns
†RHEOC	RASIN high to end-of-count high	C _L = 50pF, Figure 3			80			80	ns
†RGEOB	RGCK low to end-of-burst low	C _L = 50pF, Figure 8		State of the state of	95			95	ns
†MCEOB	Mode change to end-of-burst high	C _L = 50pF, Figure 8	STEEN I		75			75	ns

Switching Characteristics: (Contd) AT = 000 MOR = 900 Hook And Street Street Sprinker In Contd

OVMBOL	ACCESS DADAMETER	TEST CONDITIONS	'S409			'S409-2			
SYMBOL	ACCESS PARAMETER	TEST CONDITIONS	MIN T	P M	X M	IN TYP	MAX	UNI	
1 4 8 0	THREE-STATE PARAMETER								
tzH osi	CS low to address output high from Hi	Figures 6, 12 R1 = 3.5k, R2 = 1.5k	3 45040	5 6	0 20	35	60	ns	
tHZ	CS high to address output Hi-Z from high	C _L = 15pF, Figures 6,12 R2 = 1k, S1 Open	a shalli) 2	0 4		20	40	ns	
tzL	CS low to address output low from Hi-Z	Figures 6, 12 R1 = 3.5k, R2 = 1.5k	D ebalis) g	5 6) A	35	60	ns	
tLZ	CS high to address output Hi-Z from low	C _L = 15pF, Figures 6,13 R1 = 1k, S2 Open	(8 abol 2	5 5	0	25	50	ns	
tHZH	CS low to control output (WE, CAS, (RASO-3) high from Hi-Z high	Figures 6,12 R2 = 750Ω , S1 open	(8 show)	0 8)	50	80	ns	
tHHZ	CS high to control output (WE, CAS, (RASO-3) Hi-Z high from high	$C_L = 15pF$ $R2 = 750\Omega$, S1 open	d should	0 7	5	40	75	ns	
tHZL	CS low to control output (WE, CAS, (RASO-3) low from Hi-Z high	Figure 12 S1, S2 Open	boM) bits 4	5 7	5 m do	45	75	ns	
tLHZ	CS high to control output (WE, CAS, (RASO-3) Hi-Z high from low	$C_L = 15pF$, Figure 12 R2 = 750 Ω , S1 open	5	0 8	0	50	80	ns	

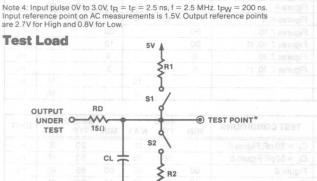
*Internally the device contains a 3K resistor in series with a Schottky Diode to VCC.

Note 1: Output load capacitance is typical for 4 banks of 22 DRAMs or 88 DRAMs including trace capacitance. These values are: Q0-Q8. CL = 500pF; RASO-RAS3, $C_L = 150pF$; CAS $C_L = 600pF$ unless otherwise noted.

Note 2: All typical values are for $T_A = 25$ °C and $V_{CC} = 5.0V$.

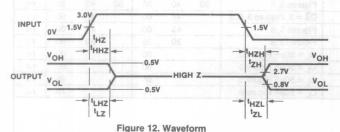
Note 3: This test is provided as a monitor of Driver output source and sink current capability. Caution should be exercised in testing this parameter. In testing these parameters, a 150 resistor should be placed in series with each output under test. One output should be tested at a time and test time should not exceed 1 second.

are 2.7V for High and 0.8V for Low.



R1, R2 = 4.7K EXCEPT AS SPECIFIED.

* The "TEST POINT" is driven by the output under test, and observed by instrumentation.



10 0 0 200 400 600 800 1000 CpF

Figure 13. Change in Propagation Delay vs Loading Capacitance Relative to a 500 pF Load

Applications

The 74S409 Dynamic RAM Controller provides all the address and control signals necessary to access and refresh dynamic RAMs. Since the 74S409 is not compatible with a specific bus or microprocessor, an interface is often necessary between the 74S409 and the system. A general application using PAL to implement the interface and two additional

chips to provide refresh clock and chip select is shown in Figure 14.

The 74S409 operating modes may vary from application to application. For efficient refresh it is recommended to use mode 1 and mode 5 to take advantage of the hidden (transparent) refresh with forced refresh backup.

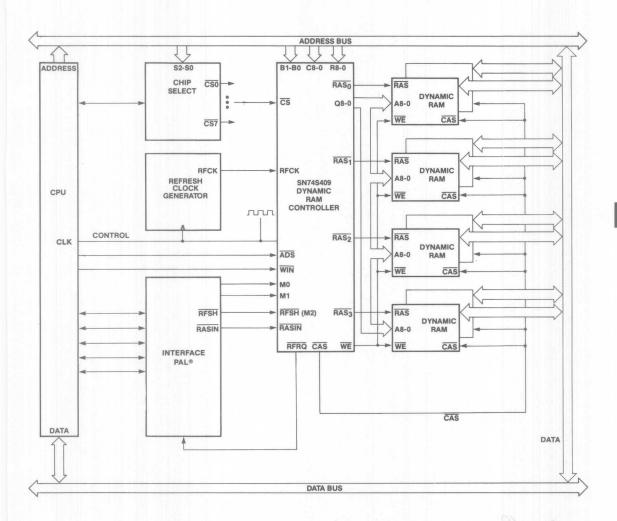
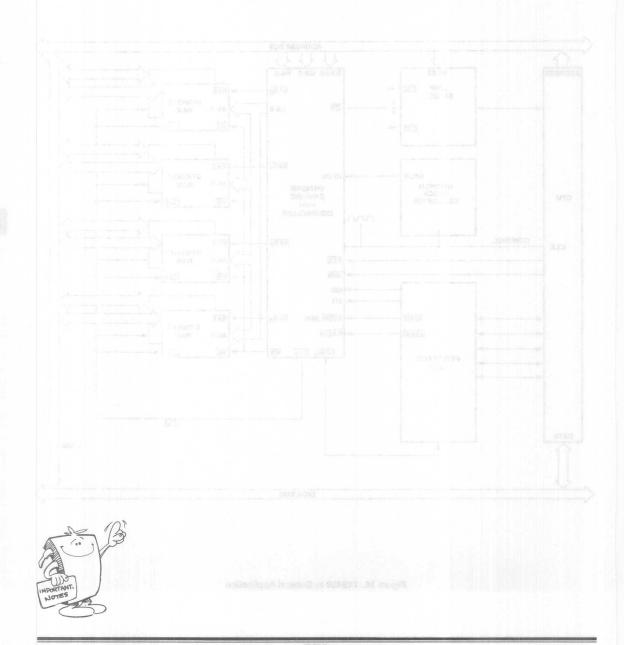


Figure 14. 74S409 in General Application

The 743406 Dynamic RAM Custrollar provides an ties iddness and retresh iddness and control rignals neon sory to edoes and retresh fynamic RAMs. Slings the 7454. As not compatible with a position bus or microprocessory or interruce is often not one other necessary between the 743400 and the system. A general application between the RAJ to implement the restore and two additional time restore and two additional

Higure 14.

The MS409 operating tracks may very frum apply about a application. For efficient retreen it is reportmented by as made 1 and made 5 to take schantage of the human francation) obtast with track retreet the care.



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2-01

ARITHMETIC ELEMENTS AND LOGIC SN74S381 Arithmetic Logic Unit/Function Generator . . . 10-3

Features/Benefits

- · A fully parallel 4-bit ALU
- · Ideally suited for high-speed processors
- · Generate and propagate outputs for full carry lookahead
- Three arithmetic functions
- Three logic functions
- Preset and clear functions

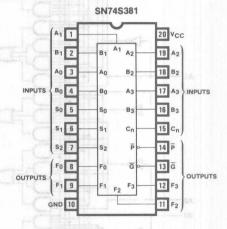
Description

The 'S381 is a Schottky TTL arithmetic logic unit (ALU)/function generator that performs eight binary arithmetic/logic operations on two 4-bit words as shown in the function table. These operations are selected by the three function-select lines (S0, S1, S2). A full lookahead carry circuit is provided for fast, simultaneous carry generation by means of two cascaded outputs (P and G) for the four bits in the package.

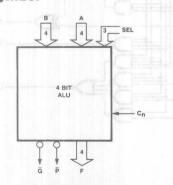
Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
SN74S381	N, J	Commercial

Pin Configuration



Logic Symbol



Function Table

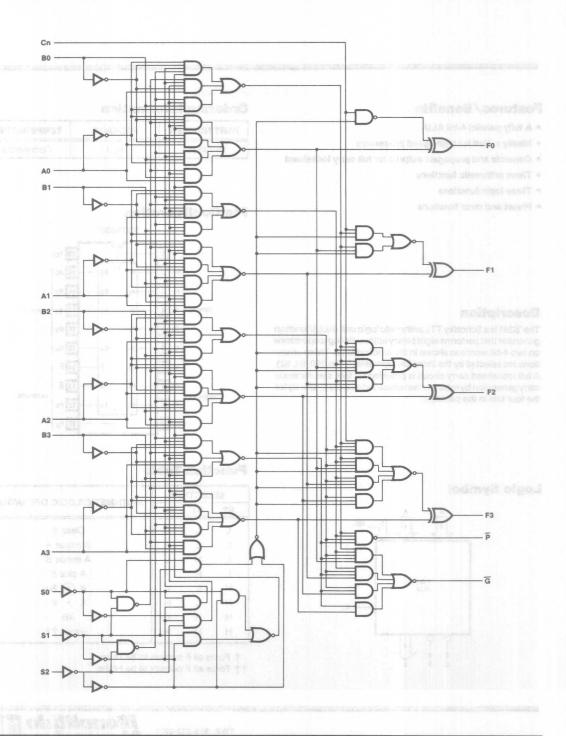
SE	LECTI	ON	ADITUMETICAL COLO ODERATION
S2	S2 S1 S0		ARITHMETIC/LOGIC OPERATION
L	L	L	Clear †
L	L	Н	B minus A
L	Н	L	A minus B
L	Н	Н	A plus B
H	L	L	A (+) B
H	L	Н	A + B
Н	H	L	AB
Н	Н	Н	Preset ††

Force all F outputs to be Lows. †† Force all F outputs to be Highs.

TWX: 910-338-2376



10-3



Function Table

						INP	UTS									OUT	PUTS		
FUNCTION	117	S2	S1	SO	Cn	A3	A2	A1	A0	ВЗ	B2	B1	ВО	F3	F2	F1	F0	G	P
Clear		0	0	0	Х	Х	Х	X	X	X	X	X	Х	0	0	0	0	0	0
					0	0	0	0	0	0	0	0	0	1	1	1	1	1	0
					0	0	0	0	0	1	1	1	1	1 =	mb.	11	0	0	0
B minus A					0	1	1	1	1	0	0	0	0	0	0	0	0	1	- 1
	1/35	0	100		0	1	1	1	1	1	1	1	1	1	1	1	1	1	0
(Inverse Subtraction)		0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0
Subtraction)	-				1	0	0	0	0	1	1	1	1	-1	1	1	- 1	0	0
					1	1	1	1	1	0	0	0	0	0	0	0	10108	1	001
					1	1	1	1	1	1	1	1	1	0	0	0	0	1	0
may not used to an incident	-				0	0	0	0	0	0	0	0	0	1	1	1	1	1	0
					0	0	0	0	0	1	1	1	1	0	0	0	0	1	1
					0	1	1	1	1	0	0	0	0	1	1	.1	0	0	0
A minus B		0			0	1	1	1	1	1	1	1	1	1	1	1	1	1	0
(Subtract)		0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	100				1	0	0	0	0	1	1	1	1	0	0	0	1	1	- 1
	148				1	1	1	1	1	0	0	0	0	1	1	191	1	0	0
					1	1	1	1	1	1	1	1	1	0	0	0	0	1	0
W 1-85					0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
					0	0	0	0	0	1	1	1	1	1	1	1	01100	1	0
					0	1	1	1	1	0	0	0	0	1	1	1	1	1	0
A plus B		0	1	1	0	1	1	1	1	1	1	1	1	1	1	.1	0	0	0
(Add)	-	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	1	1	-1
					1	0	0	0	0	1	1	1	1	0	0	0	0	1	0
					1	1	1	1	1	0	0	0	0	0	0	0	0	1	0
					1	1	1	1	1	1	1	1	1	1	1	1	1	0	0

Function Table

	-				- 11	NPU	TS						(TUC	PUT	S	wonii	
FUNCTION	S2	S1	SO	Cn	A3	A2	A1	A0	В3	B2	B1	ВО	F3	F2	F1	F0		
_				Х	0	0	0	0	0	0	0	0	0	0	0	0	tuqni.	
A+)B	1	0	0	X	0	0	0	0	.1.	1	.1	1	1	.1	1	1		
(OR)	'	U	U	X	1	1	1	1	0	0	0	0	1	1	1	.1	F-940U	
				X	1	1	1	1	1	1	1	1	0	0	0	0	pega io	
A + B (XOR)		1	2	Х	0	0	0	0	0	0	0	0	0	0	0	0	-rigiti	
	1	0	4	X	0	0	0	0	1	1	1	1	1	1	1	1	eghur	
	1	0	1	X	1	1	1	1	0	0	0	0	1	1	1	1	redu Ori	
				X	1	1	1	1	1	1	1	1	1	1	1	10	burio.	
		301		X	0	0	0	0	0	0	0	0	0	0	0	0	rue Lie	
A · B	1	1	0	X	0	0	0	0	1 0	1	1	1	0	0	0	0	n accusal	
(AND)	-		0	X	1	1	1	1	0	0	0	0	0	0	0	0	0.01.37.010.3	
				X	1	1	1	1	1	1	1	1	1	1	1	1	TRUE I	
				Х	0	0	0	0	0	0	0	0	.1	1	1	1		
Preset	1	4	4	X	0	0	0	0	1	1	1	1	1	1	1	1		
Fieset	1	1	- 1	X	1	1	1	1	0	0	0	0	1	1	1	1		
			100	X	1	1	1	1	1	1	1	1	1	1	1	1		

- 1 = HIGH voltage level
- 0 = LOW voltage level
- X = Don't care

Absolute Maximum Ratings

Supply voltage V _{CC}	
Input voltage	
Storage temperature range	65° to +150° C

Operating Conditions

SYMBOL	PARAMETER DO DO	MIN	COMMERCIAL TYP	MAX	UNIT
Vcc	Supply voltage	4.75	5	5.25	V
TA	Operating free-air temperature	0		75	°C

Electrical Characteristics Over Operating Conditions

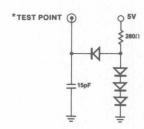
SYMBOL	PARAMETER		TEST CONDITION	IS	MIN	COMMERCIAL TYP	MAX	UNIT	
V _{IL}	Low-level input voltage	0 0 8	0 0 0 0	0 0 0 0			0.8	٧	
VIH	High-level input voltage	1 0	1 1 1 1		2		E sulq (Add)	V	
VIC	Input clamp voltage	V _{CC} = MIN	I _I = -18 mA	0 0 0			-1.2	V	
0			1 1 1	Any S input	7		-2		
IIL	Low-level	V _{CC} = MAX	V _I = 0.5 V	Cn			-8	mA	
	input current			All others					
				Any S input		eld	50		
IH	High-level input current	V _{CC} = MAX	V _I = 2.7 V	Cn		ary a statement of the second	250	μΑ	
	input current			All others	AD 20 00	MOTO DE	200		
Ц	Maximum input current	V _{CC} = MAX	V ₁ = 5.5 V	0 0 X			1	mA	
V _{OL}	Low-Level output voltage	V _{CC} = MIN V _{IL} = 0.8 V	V _{IH} = 2 V I _{OL} = 20 mA	1 1 X 1 1	0, 0 T	(RO)	0.5	V	
V _{OH}	High-level output voltage	V _{CC} = MIN V _{IL} = 0.8 V	V _{IH} = 2 V I _{OH} = -1 mA	0 0 X	2.7	3.4		V	
los	Output short- circuit current*	V _{CC} = MAX	0 0 0 1 7	r I X	-40	(1900)	-100	mA	
Icc	Supply current	V _{CC} = MAX	0 0 0 0	0 0 X	105		160	mA	

^{*} Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

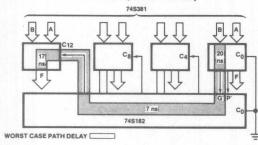
SYMBOL	PARAMETER	TEST CONDITIONS (See Interface Test Load/Waveforms)	FROM (INPUT)	TO (OUTPUT)	748 TYP	381 MAX	UNIT
tp	Propagation delay time		С	Any F	10	17	ns
tp	Propagation delay time		Any A or B	G	12	20	ns
tp	Propagation delay time		Any A or B	P	11	18	ns
^t PLH	Propagation delay, low-to-high	C _L = 15 pF R _L = 280Ω			18	27	ns
^t PHL	Propagation delay, high-to-low		Any A or B	Any F	16	25	ns
tp	Propagation delay time		Any S	Any F, G, P	18	30	ns

Test Load



* The "TEST POINT" is driven by the output under test, and observed by instrumentation.

16-BIT ALU (USING 74S381)



MAXIMUM DELAY OF ADDITION/SUBTRACTION.

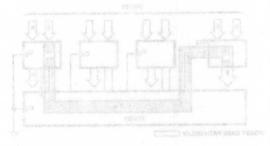
	74S381 + 74S182
1-4 bits	27ns
5-16 bits	44ns
17-64 bits	64ns



KAR		(rustuo)	(contract final final rest (contract)		
				Propagation delay inc	
	12			Propagation dalay time	
			CL = 15 pF PL = 2800		
18					

None LineT

16-BIT ALU (USING 748031)



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Cray Multipliers

DESCRIPTION	PART NUMBER	MAX DELAY	PINS
8x8 Multiplier (latched) 8x8 Multiplier 8x8 Multiplier	SN74S557 SN74S558 SN54S558	60 ns (X _i , Y _i , to S ₁₅) 60 ns 60 ns	40 40 40
16x16 Multiplier	SN74S556	76 ns (X _i , Y _i to S ₁₅₋₀) 90 ns (X _i , Y _i to S ₃₁₋₁₆)	84 84

Five New Ways to Go Forth and Multiply

Chuck Hastings

Our Multiplier Population Explosion

Recently it has seemed as if every time you turned around Monolithic Memories was announcing *another* new multiplier. Want to catch your breath, and find out where each of these fits into the overall scheme of things? Read on.

Actually, there have been five new multipliers in all within the last three years, plus two which had previously been available for several years. In time order of introduction, these are:

Parts No.	Description ^A
57/67558	150-nsec 8x8 Flow-Through Cray Multiplier ^B
57/67558-1	125-nsec 8x8 Flow-Through Cray Multiplier ^B
54/74S508	8-Bit Bus-Oriented Sequential Multiplier/ Divider
54/74S558	60-nsec 8x8 Flow-Through Cray Multiplier
54/74S557	60-nsec 8x8 Flow-Through Cray Multiplier with Transparent Output Latches
54/74S516	16-Bit Bus-Oriented Sequential Multiplier/ Divider
54/74S556	90-nsec 16x16 Flow-Through Cray Multiplier with Transparent Input and Output Latches for full 32-bit output

NOTES: A. Times are worst-case times for commercial-temperature-range parts.

B. Obsolete. 54/74S558 replaces these in both new and existing designs.

You will notice that the above parts fall into two categories: flow-through Cray multipliers, and bus-oriented sequential multiplier/dividers. Although all of these parts get referred to rather casually as "multipliers," there are major differences between the two general types; see Table 1 below.

The Cray Multipliers

The essential idea of a Cray multiplier, as originally put together by Seymour Cray in the late 1950s with discrete logic at Control Data Corporation, is to wire up an array of full adders in the form of a binary-arithmetic-multiplication pencil-and-paper example. That is, everywhere that there is a "1" or a "0" in a longhand binary-multiplication example, the Cray type of multiplication uses a full adder. One may visualize a Cray multiplier functionally as a "diamond," as follows:

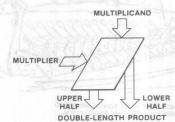


Figure 1. Pencil-and-Paper Analogy to Cray-Multiplier Operation

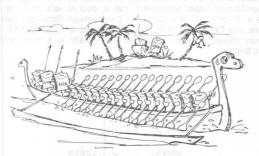
	Flow-Through Cray Multiplier	Bus-Oriented Sequential Multiplier/Divider
Role in System	Building-block role — as many as 34 parts used in one super- minicomputer (NORD-500 from Norsk Data').	Co-processor role — one, or occasionally two, parts used in one microcomputer ² .
Internal Operation	Static arithmetic-logic network; multiplies without being clocked? using eight bits of the multiplier at a time.	State machine; requires clocking to operate; contains edge- triggered registers; sequenced by a state counter; multiplies using two bits of the multiplier at a time ⁴ .
External Control	Controlled by several mode-control input signals.	Controlled by sequences of micro-opcodes which come from a microprocessor, a registered PAL, or some other sequential control device.
Package	40-pin DIP ('S557/8); 84-pin LCC or 88-pin PGA ('S556)	24-pin DIP.
Operations Performed	Can only perform multiplication.	Can perform multiplication, division, and multiplication-with-accumulation.
Storage Capabilities	Either no storage capabilities ('558 types), or optional storage for the double-length product only ('557 type), or full product and input storage ('556 type).	Four full-length registers; capable of storing both input operands and the double-length product.
Second Sources	8x8, Multiple-sourced (AMD, Fairchild, Monolithic Memories).	Sole-sourced; only bipolar dividers on the market.
Where Used	Initial usage has been in high-end minicomputers, array processors, and signal processors.	Initial usage has been in industrial-control microcomputers, digital modems, military avionics, CRT graphic systems, video games, and cartographic analysis systems.
Future Prospects	Potential large market today since these parts are now low-cost and multiple-sourced, and should be used in all new mini-computer designs!	Potential huge world-wide market for enhancement of micro- processor, bit-slice processor, and microcomputer capabilities and for small-scale signal processing!

Table 1. A comparison of the two types of Monolithic Memories Multipliers

Five New Ways to Go Forth and Multiply

Our 57/67558, introduced in the mid-1970s, was the original single-chip Cray multiplier. To achieve what was for that time very high performance for a Schottky-TTL-technology part, the internal design of the 57/67558 also exploited other speed-freak multiplication techniques such as Booth multiplication⁴ and Wallace-Tree addition⁵. All of these techniques achieve increased speed through extensive parallelism, and can be used at the system level as well as within LSI components. Subsequently, process improvements made it possible to offer a faster final-test option, the 57/67550-1, which attained a sales-volume level essentially equal to that of the original part.

About five years ago, AMD paid us the sincere compliment of second-sourcing these parts with the 75-nsec 25S558. Three years ago, we returned the compliment with the 60-nsec 54/74S558. All of these '558 parts, and the 70-nsec 54/74F558 announced by Fairchild, are fully compatible drop-in equivalents except for the variations in logic delay.



"ALL OF THESE TECHNIQUES ACHIEVE INCREASED SPEED THROUGH EXTENSIVE PARELLELISM."

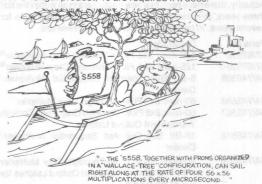
When AMD introduced the 25S558, they introduced along with it the 80-nsec 25S557, a "metal option" of the same basic design with "transparent" output latches to hold the double-length product. "Transparent" means that the latches go away when you don't want them there; a latch-control line like that of the 54/74S373 controls whether these output latches store information, or simply behave as output buffers. Anyway, when we introduced our 54/74S558, we followed it within a few weeks with the 60-nsec 54/74S557, which is a much faster drop-in replacement for AMD's part. And subsequently, Fairchild has announced a 70-nsec 54/74F557.

Because AMD's 'S557 has the output latches implemented in TTL technology after the ECL-to-TTL converters, whereas our 'S557 has them implemented in ECL technology before the conversion, the latches operate much faster in ours. Our 'S557 is typically only about a nanosecond slower than our 'S558, whereas the logic-delay difference between AMD's two parts is considerably greater. Consequently, our margin of superiority over AMD for the 'S557 is even greater than for the 'S558.

More recently, we introduced the 90-nsec 'S556, which is a 16x16 direct size-upgrade of the 'S557/8 architecture, with the addition of input latches. In a "pipelined" mode, an 'S556 can produce a new 32-bit product every 75 nsec.

'S557/8 Cray multipliers come in a 40-pin dual-inline package, either ceramic or plastic. Worst-case power-supply current is 280 mA. The 'S556 comes in your choice of an 84-pin LCC (Leadless Chip Carrier) or an 88-pin PGA (Pin-Grid Array) package. Worst-case power-supply current is 800 mA (900 mA over military temperature range). The data-bus outputs can sink up to 8 mA IOL, for all of these multipliers.

References 5 and 6 discuss technical approaches to using Cray multipliers in high-performance minicomputers. The 'S558, together with PROMs organized in a "Wallace-tree" configuration, can sail right along at the rate of four 56x56 multiplications every microsecond, on the basis of fixed-point arithmetic with no renormalization. (See table 7 on page 16 of reference 5; the multiplication time is 238 nsec for a "division step," which is a fixed-point multiplication, and 319 nsec for a floating-point multiplication where extra time is required for renormalization and correction of the exponent of the product.) 34 'S558s or 'S557s are required to perform this multiplication if the computer system architecture does not call for the computation of the least-significant half of the double-length product; 49 are required if it does.



The "local" architecture of the multiplier section of a digital system can take two rather different forms. A minicomputer which executes an unpredictable mixture of arithmetic and logical instructions one after the other, typically needs to be able to get the complete multiplication over and done with before going on to the next program step—which is probably not another multiplication. An array processor or digital correlator, however, tends to do very regular iterative computations; and the performance of such a system can often be greatly increased by a technique called "pipelining," in which the arithmetic unit consists of stages with registers or latches in between each stage, and partial computational results move from one stage to the next on each clock.

The "flow-through" architecture of the 'S558 works equally well in synchronous or asynchronous pipelined systems, but registers or latches must be provided externally. The 'S557, however, is actually a *superset* of the 'S558, and the added internal-output-latch feature adapts it particularly well to pipelined systems. The 'S556 provides latches at *both* ends.



11

Even a smaller-scale system can make effective use of these parts. To return to the case of 56x56 multiplication, which corresponds to the word-length needed for multiplying mantissas in several popular floating-point-number formats, an iterative clocked scheme using just seven 8x8 multipliers, some adders, and an accumulator register can form the entire 112-bit double-length product in just seven multiply/add cycles. A number of mid-range minicomputers today multiply in this manner. The multipliers are configured as suggested by the following block diagram:

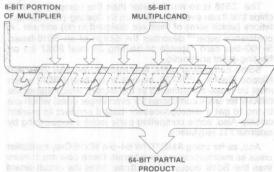


Figure 2. 8x56 Cray Multiplier In Diamond Representation

There is even an occasional 8-bit or 16-bit microprocessorbased system with a need for *very* fast multiplication, where 'S557/8s or 'S556s may get used as microprocessor peripherals^{7,8}. Digital-video systems, in particular electronic games, with "vector graphic" capabilities are one example.

The world of 'S556/7/8 applications has turned out to include all sizes of minicomputers, digital video systems, and signal processors — FFT (Fast Fourier Transform) processors, voice recognition equipment, radar systems, digital correlators and filters, electronic seismographs, brain and body scanners, and so forth. And there are many unexpected off-beat applications, such as real-time data-rescaling circuits in instruments, altogether too numerous to list here. After all, an'S556 can multiply two 16-bit numbers together and output their entire 32-bit product in 90 nsec worst case...less time than it would take a speeding bullet to move the distance equal to the thickness of this piece of paper. How's that for Supermultiplier?

The Multiplier/Dividers

The Monolithic Memories 'S516 and 'S508 are state-of-theart TTL-compatible intelligent peripherals for microprocessors, somewhere between arithmetic sequential circuits and specialized bipolar microprocessors. The 'S516 and 'S508 each can perform any of 28 different multiply and multiply-and-accumulate instructions, plus any of 13 different divide instructions, at bipolar speeds under the control of an internal state counter. (See Figure 2 of the 'S516 data sheet.) The state counter's sequence is in turn guided by 3-bit instruction codes which are external inputs to the 'S516/508. The 'S516 computes with 16-bit binary numbers, and the 'S508 computes with 8-bit binary numbers, as the part numbers none-too-subtly imply.

A 16-bit bi-directional data bus connects the 'S516 with the outside world for bringing in multipliers, multiplicands, dividends, and divisors; and returning products, quotients and remainders. It also has clock (CK) and run/wait (GO) inputs, and an overflow indication (OVR) output.

The 'S508 has all of the above inputs and outputs also, except that it has only an 8-bit bidirectional data bus. Since it comes in the same 24-pin package as the 'S516, it obviously has eight more pins available for other purposes. Four of these are used to bring out the internal-state-counter value; one each is used for a completion (DONE) status output, an output-enable control (OE) input, and a masterreset (MR) control input; and one is not used at all.

A simple, general interfacing scheme can be used to team a 'S516 with any of the currently popular 16-bit microprocessors, or an 'S508 with any 8-bit microprocessor. (See Figure 7 of the 'S516 data sheet.) With a couple extra interface circuits, an 'S516 can also be interfaced to an 8-bit microprocessor. Particularly if the system software is written in a highly-structured language such as PASCAL or FORTH, an 'S516/508 can be retrofitted into an existing system with a large gain in performance and very little impact on either hardware or software — calls to the previous software-implemented one-step-at-a-time multiply and divide subroutines are simply rerouted to substitute a command from the microprocessor to the 'S516/508 to accept an operand and start its operation sequence.

The 'S516 and 'S508 are in fact two different "metal options" of one basic design; the 'S516 has twice as many data bits in each internal register. The 'S516 and 'S508 both have a worst-case clock rate of 6 MHz (commercial) or 5 MHz (military); the typical rate is 8 MHz. The simplest complete twos-complement 16x16 multiplication instruction can be performed in nine clock cycles by an 'S508, since 2-bits-at-a-time Booth multiplication is used; 4 thus, the worst-case time required by the 'S516 to multiply in this mode is 1.5 μ sec for a commercial part, and for an 'S508 it is 833 nsec. On the same basis, 32/16 division can be done in 21 clock cycles, or 3.5 μ sec worst-case, by an 'S516; and 16/8 division can be done in 13 clock cycles, or 2.2 μ sec worst-case, by an 'S508.

An 'S516/508 can perform either positive or negative multiplication or multiply-accumulation, and many of the instructions provide for "chaining" of successive computations to eliminate extra operand transfers on the bus; these features further enhance the computational speed of the 'S516/508 in particular applications. Arithmetic can be either integer or fractional with respect to positioning of the results.

An 'S516 can powerfully enhance the capabilities of any present-day 16-bit or 8-bit microprocessor in a compute-bound application. In fact, it can be used in any digital system where there is a need to multiply and divide on a bus. An 'S508 can likewise enhance the capabilities of any 8-bit microprocessor.



The 'S516 comes in an industry-standard 600-mil 24-pin dual-inline package, modified to include an integral aluminum heatsink which does not add appreciably to the package height. It requires only +5V and ground power connections, and draws a worst-case power-supply current of 450mA (commercial) or 500mA (military). Power consumption is greatest at cold temperatures, and decreases substantially as operating temperature increases. The 16 databus inputs require at most 0.25mA input current; the other inputs require at most 1mA. The 16 databus outputs can sink up to 8mA lou. The 'S508 also fits the above description, except that its worst-case power-supply current is 380mA (commercial) or 400mA (military), and it has only 8 databus inputs and outputs.

In describing applications of these parts, it is difficult to know where to start — they can be used in almost any design where a microprocessor can be used, and you know how many places that is today. So, perhaps a good starting point is to see what uses customers have thought up all by themselves. One customer even used two 'S516s in "pingpong" mode on a single 16-bit bus! So, rather than merely speculating as to what these parts might be good for, here's a list of what Monolithic Memories's customers have already proven they are good for:

- Real-time control of heavy machinery⁹
- · Low-cost, high-performance digital modems
- CRT graphics, including video games
- Military avionics
- Cartographic analysis

As it happens, the above are 'S516 applications, except that digital modem designs have been done with both the 'S516 and the 'S508. Several of the 'S516 designs are already in production. In each of these applications, the microprocessor could have coped all right with the computational complexity, albeit at its own less-than-tremendous speed, but a 'S516 used together with the microprocessor can provide extra muscle for handling formidable problems.



Competition? Well, since there are no second sources for the 'S516, and no competitor at present has a similar fast part capable of performing division as well as multiplication, right now the 'S516 has no *direct* competition. Indirectly, there are some competing parts which perform *only* multiplication, and would have to perform division by Newton-Raphson iteration to be usable for any application where division is required. However, the 'S516 is (as far as we know) by far the lowest-

priced bipolar 16-bit multiplier, and the other microprocessor peripheral chips which can perform division as well as multiplication are relatively-slow MOS devices. In one case, an 8-bit cascadable CMOS part requires a 50% reduction in clock rate to do 16-bit arithmetic. And considerable numerical-analysis and programming sophistication are required to implement Newton-Raphson division with fixed-point operands. (It's easier with floating-point operands.) In contrast, the 'S516/508 can be easily interfaced to almost any microprocessor using one or two PALs,* and can perform either multiplication or division on command?

The 'S516 is so much faster than the competing MOS chips that it can even take them on for *floating-point* computations (which some of them are designed to do) and win. A conference paper¹⁰ describes the design of an 'S516-based S-100-bus card capable of beating an Intel 8087 2:1 on floating-point arithmetic.

Some competing parts, in particular the AMI 2811 and Nippon Electric µPD7720, include an on-board ROM which must be mask-programmed at the factory, which makes life difficult for small companies (or even larger ones) which are trying to get a microprocessor-based product to market quickly. Also, some competing parts require sequencing by external TTL jellybeans.

And, as for using AMD/TRW 64-pin 16x16 Cray multiplier chips as microprocessor peripherals, these cost much more than the 'S516, occupy about three times the circuit-board space, multiply faster, don't divide at all except by Newton-Raphson iteration, and also require one or two "overhead" microprocessor instructions to interface for a given arithmetic operation. From a system viewpoint, when this overhead time is reckoned with, these chips provide little actual gain in multiply performance over the 'S516 at lots of extra cost, and an actual loss in divide performance: the 'S516 is much more cost-effective overall.

"S516s potentially fit into many, many places in commercial, industrial, and military electronics, particularly into small-scale real-time systems. The part is fast enough to enhance the performance of a 16-bit Motorola 68000, Zilog Z8000, or Intel 8086, as well as that of any 8-bit microprocessor. It is also fast enough to considerably improve the multiplication and division performance of 16-bit 2901-based "bit-slice" bipolar microcomputers, which are often used as processors in desktop graphics CRT terminals.

It is worth bringing the 'S516 to the attention of any designer who is developing:

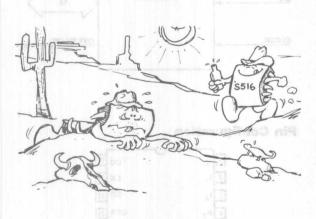
- · A personal computer or small business computer.
- A word processor, or a more grandiose "office automation system"
- A cruise missile, or any other "smart weapon."
- · A digital modem.
- A small-scale speech-processing system. (These are very multiplication-intensive. We have one magazine article on the 'S516 in such an application.¹)
- · A smart instrument, which does data conversion.
- An industrial control system, particularly one which must do many coordinate transformations.
- An all-digital studio-quality high-fidelity system.
- A cost-reduced computerized medical scanning system.
- A multiprocessor system for scientific computations¹²)

If an 'S516/508 is introduced into a system configured around an older microprocessor as a "co-processor" or

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helpmate for the microprocessor, and the application is arithmetic-intensive, the end effect can be a major upgrading of performance at the system level. ²⁷ Consequently, a major reason for designing these parts in is *microprocessor life-cycle enhancement*. In particular, many MOS microprocessors have single-length and double-length add and subtract instructions: but either they have no multiply or divide instructions at all, or else they perform their multiply and divide instructions so slowly as to jeopardize the ability of the entire system to handle its computing load in real time.

So picture, if you will, the entrepreneur or chief engineer of a firm making a successful microprocessor-based widget which has been on the market for a few months, which uses an older 8-bit microprocessor such as a 6800 or 8085 or Z80. Just when his/her sales are really taking off, here comes a new start-up competitor with a similar system, using a Motorola 68000, with added features and faster performance made possible by the 68000's 16-bit word length and multiply/divide capabilities. The 'S516 can, in this instance. serve as a "great equalizer"-it can be retrofitted into the older system as previously described, and provides even higher-speed multiplication and division than the 68000. (Enough so, actually, that there are designers using the 'S516 with the 68000.) Thus, the 'S516 can dramatically extend the life cycle of existing microcomputer systems based on microprocessors which either don't have multiplication and division instructions, or perform these operations relatively slowly.



"... THE 1556 CAN DRAMATICALLY EXTEND THE LIFE CYCLE OF EXISTING MICROCOMPUTER SYSTEMS BASED ON MICROPROCESSORS WHICH EITHER DON'T HAVE MULTIPLICATION AND DIVISION INSTRUCTIONS, OR PERFORM THESE OPERATIONS RELATIVELY SLOWLY..."

'S508s are somewhat easier to control from a logic-design viewpoint than 'S516s, purely because they have more control inputs and outputs. However, the shorter 'S508 word length makes the part naturally fit into smaller-scale systems than those which might use an 'S516. Essentially, the 'S508 is optimized for small-scale systems.

Now that you know what these parts are, can't you think of at least half a dozen prime uses for them right in your own hack yard?

References (all available from Monolithic Memories)

- "Combinatorial Floating Point Processor as an Integral Part of the Computer," Tor Undheim, Electro/80 Professional Program Session Record, Session 14 reprint, paper 14/1.
- "SN54/74S516 Co-Processor Supercharges 68000 arithmetic," Richard Wm. Blasco, Vincent Coli, Chuck Hastings and Suneel Rajpal, Monolithic Memories Application Note AN-114.
- "How to Design Superspeed Cray Multipliers with 558s," Chuck Hastings, included within the SN54/74S557/8 data sheet.
- "Doing Your Own Thing in High-Speed Digital Arithmetic," Chuck Hastings, Monolithic Memories Conference Proceedings reprint CP-102.
- "Big, Fast, and Simple Algorithms, Architecture, and Components for High-End Superminis," Ehud Gordon and Chuck Hastings, Monolithic Memories Application Note AN-111
- 6. "Fast 64x64 Multiplication using 16x16 Flow-Through Multipliers and Wallace Trees," Marvin Fox, Chuck Hastings and Suneel Rajpal, Monolithic Memories Conference Proceedings reprint CP-111.
- "An 8x8 Multiplier and 8-bit μp Perform 16x16 Bit Multiplication," Shai Mor, EDN, November 5, 1979. Monolithic Memories Article Reprint AR-109.
- "Using a 16x16 Cray Multiplier as a 16-Bit Microprocessor Peripheral to Perform 32-Bit Multiplication and Division," Chuck Hastings, Monolithic Memories Conference Proceedings reprint CP-140
- "The Design and Application of a High-Speed Multiply/ Divide Board for the STD Bus," Michael Linse, Gary Oliver, Kirk Bailey, and Michael Alan Baxter, Monolithic Memories Application Note AN-115.
- "Minimum Chip-Count Number Cruncher Uses Bipolar Co-Processor," C. Hastings, E. Gordon, and R. Blasco. Monolithic Memories Conference Proceedings reprint CP-109
- "Medium-speed Multipliers Trim Cost, Shrink Band-width in Speed Transmission," Shlomo Waser and Allen Peterson, Electronic Design, February 1, 1979; pages 58-65. Monolithic Memories Article Reprint AR-107.
- "A Synchronous Multi-Microprocessor System for Implementing Digital Signal Processing Algorithms," T.P. Barnwell, III and C.J.M. Hodges, Southcon/82 Professional Program Session Record, Session 21 reprint, paper 21/4.

Features/Benefits

- Co-processor for enhancing the arithmetic speed of all present 16-bit and 8-bit microprocessors
- Bus-oriented organization
- 24-pin package
- 16/16 or 32/16 division in less than 3.5 μsec
- 16x16 multiplication in less than 1.5 μsec
- 28 different multiplication instructions such as "fractional multiply and accumulate"
- 13 different divide instructions
- Self-contained and microprogrammable

Description

The SN74S516 ('S516) is a bus-organized 16x16 Multiplier/ Divider. The device provides both multiplication and division of 2s-complement 16-bit numbers at high speed. There are 28 different multiply options, including: positive and negative multiply, positive and negative accumulation, multiplication by a constant, and both single-length and double-length addition in conjunction with multiplication. 13 different divide options allow single-length or double-length division, division of a previously-generated result, division by a constant, and continued division of a remainder or quotient.

The 'S516 is a time-sequenced device requiring a single clock. It loads operands from, and presents results to, a bidirectional 16-bit bus. Loading of the operands, reading of the results, and sequential control of the device is performed by a 3-bit instruction field.

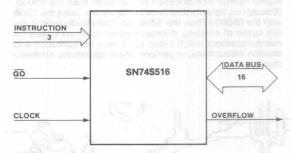
The 'S516 has the additional feature that operands and results can be either integers or fractions; when it deals with fractions, automatic scaling occurs. Results can be rounded if required, and an Overflow output indicates whenever a result is outside the normally-accepted number range.

For a simple multiplication of two operands the device takes nine clock periods — one for initialization, and eight for the actual multiplication. A realistic clock period is 167 ns, which gives a multiplication time of 1333 ns typical for 16x16 multiplication, plus 167 ns additionally for initialization, or 1500 ns in all. More complex multiplications will take additional clock periods for loading the additional operands. A simple division operation requires 16 + 4 = 20 clock periods for a typical time of 3.333 ns (32 bits/16 bits), also plus 167 ns for initialization, or 3500 ns in all.

Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
SN74S516	24T	Commercial

Logic Symbol



Pin Configuration



SKINNYDIP® is a registered trademark of Monolithic Memories.

TWX: 910-338-2376 2175 Mission College Blvd. Santa Clara. CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2374

		CTIC		OPERATION	CLOCK
1			A	RITHMETIC OPERATIONS	-
			0	X1 · Y	9
			1	-X1 · Y	9
			2	$X1 \cdot Y + K_z, K_w$	9
			3	-X1 · Y + K _z , K _w	9
			4	K _z , K _w /X1	21
		5/6	0	X·Y	10
		5/6	1	-X · Y	10
		5/6	2	$X \cdot Y + K_Z, K_W$	10
		5/6	3	$-X \cdot Y + K_z, K_w$	10
		5/6	4	K _w /X	22
		5/6	5	K ₇ /X	22
	5/6	6	0	X·Y+Z	11
	5/6	6	1	-X · Y + Z	11
	5/6	6	2	X · Y + K _z · 2 ⁻¹⁶	11
	5/6	6	3	-X · Y + K _z · 2 ⁻¹⁶	11
	5/6	6	4	Z, W/X	23
	5/6	6	5	Z/X	23
5/6	6	6	0	X·Y+Z, W	12
5/6	6	6	1	-X · Y + Z, W	12
5/6	6	6	2		12
5/6	6	6	3	-X · Y + W _{sign}	8 12
5/6	6	6	4	_	24
5/6	6	6	5	W _{sign} /X	24
5/6	6	6	6	(See Note 9 below.)	7
5/6	6	6	7	Load X, Load Z, Load W, Clear Z	4
	5/6	6	7	Load X. Load Z. Read Z	3
168	neg.	HU Y	pris.	READING OPERATIONS	re one st
5/8/	1 70	1,18	7		市的方
		7	7		
	7	7	7	Read Z, W, Z	3
7	7	7	7	Read Z, W, Z, W	4
		5	7		2
	5	7	7	Round, then Read Z, W	3

NOTES

- X,Y are input multiplier and multiplicand.
- X1 is the previous contents of the first rank of the X register (either the old X or a new X).
- Fractional or integer arithmetic is specified by having the next-to-the-last operand loaded using a 5 or 6 instruction respectively. All rows beginning with "5/6" in effect represent two instructions. 5 does fractional arithmetic and 6 does integer arithmetic.
- Z, W is a double-precision number. Z is the most significant half, Z, W represents addend upon input, and product (or accumulated sum) after multiplication.
- K_Z, K_W represents previous accumulator contents. K_Z is the most-significant half
- Wsign is a single-length signed number, with sign extension.
- 7. Maximum clock cycle = 167 ns for an 6-MHz clock.
- If n instruction codes are shown at the left under "instruction sequences," the number of clock cycles at the right is n+8 for multiplication and n+20 for division.
- The code "5/6 6 6 6" represents an incomplete operation since it leaves the 'S516 in state 1 rather than in state 0, 8, or 10.

Figure 1. 'S516 Instruction Set (Partial List)

S	UMMARY OF SIGNALS/PINS
B ₁₅ -B ₀	Bidirectional data bus inputs/outputs
12-10	Instruction (sequential control) input
CK	Clock pulse input
GO	Chip activation input
OVR	Arithmetic overflow output

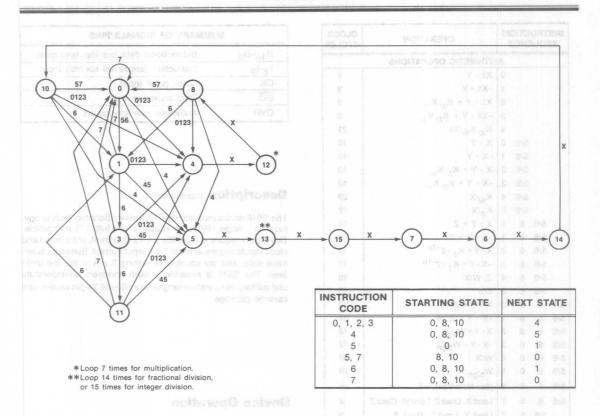
Description (continued)

The 'S516 device uses standard low-power Schottky technology, requires a single +5V power supply, and is fully TTL compatible. Bus inputs require at most 250 μA input current, and control and clock inputs require at most 1 mA input current. Bus outputs are three-state, and are capable of sinking 8 mA at the low logic level. The 'S516 is available in both commercial-temperature and military-temperature ranges, in a 600-mil 24-pin dual-in-line ceramic package.

Device Operation

The 'S516 contains four 16-bit working registers. Y is the multiplier register; X is the multiplicand and divisor register; W is the least-significant half of a double-length accumulator, and holds the least-significant half of the product after a multiplication operation, or the remainder after a division operation; and Z is the most-significant half of this same accumulator. In addition to these registers, there is a high-speed arithmetic unit which performs addition, subtraction, and shifting steps in order to accomplish the various arithmetic operations; a loading sequencer; and a PLA control network.

Operands are loaded into the working registers in time sequence at each clock period, under the control of this sequencer. The chip-activation signal GO must be LOW in order to begin the loading process and continue to the next step in the loading operation. If GO is continually held HIGH, the 'S516 remains in a wait state with its outputs held in their high-impedance states, so that the other devices attached to the bus may drive it. In this condition, the 'S516 does not respond to any codes on its instruction inputs; in effect, it does not "wake up" until GO goes LOW. Also, GO may change only when the clock input CK is HIGH. After all of the operands are loaded, the 'S516 jumps to the multiply routine, or to the divide routine, and performs the required operations as indicated in Figure 1. After 9 clock periods for a simple multiply or 21 clock periods for a simple divide, for example, the result is placed on the bus in time sequence.



KEY: Y instalger publicly 1d-81 ruol another 8162 od?

The numbers inside the circles indicate the *state* of the 'S516 multiplier/divider. These states are represented by a four-bit state counter, where A is the least-significant bit of this state counter and D is the most-significant bit. (These four bits are not available externally on the 'S516.)

The next state of the 'S516 is a function of the present state and the instruction lines. For example if the 'S516 is at state 0 and the instruction is 0, 1, 2, or 3, then the next state is state 4 (multiply instruction); if the instruction is 4, the next state is state 5 (divide instruction); and so forth. The instructions which take the 'S516

from one state to another are indicated by the numbers written next to the state-transition path lines. "0123," for instance, implies that *any* of instructions 0, 1, 2, or 3 will take the 'S516 along the path marked "0123."

"X" next to a path implies that the path will be followed regardless of the value of the instruction inputs at that time. In other words, for the purpose of state transitions, X means "don't care." There are cases, however, where the particular instruction used may affect when the contents of the registers are available on the bus — see Figures 9 and 10 for contrasting examples of how this effect operates.

Figure 2. Transition Diagram for the 'S516 Multiplier/Divider

Three instruction inputs I₂, I₁, I₀, which may change only when the clock input CK is HIGH, select the required function and drive the sequencer from state to state. Thus, the action of the multiplier/divider at any clock period is a function of the machine state and the state of the control inputs. Figure 2 shows the multiply/divide state table, and all possible operations. After a Read or Round operation, the machine is driven back to state 0, and a new sequence of arithmetic operations is assumed. If a chain operation is being performed, such as accumulation of products, state 0 is bypassed, and loading of an operand or jumping to the next arithmetic operation occurs at the end of the

previous arithmetic operation — at state 8 for a multiplication instruction, or at state 10 for a division instruction.

Register X is a dual-rank register, which allows the loading of an operand X during the multiplication or division process. If the machine enters the loading sequence and a new X operand has not been loaded, then the machine proceeds with the previously-loaded X, denoted in this text as "X1." This loading-while-processing capability allows a cycle to be saved during "chained" calculations, and also allows multiplication and division by a constant. (See Figure 13). (continued next page)

Figures 3 and 4 show the codes and durations for the 41 different possible arithmetic operations. These operations can be concatenated in strings to perform complicated 2s-com-

plement arithmetic operations at high-speed. Rounding and reading of results can be performed after any operation. Figure 5 is a block diagram of the 'S516 16x16 Multiplier/Divider.

(continued page after next)

							TIME	-SLO	T a				
OPERATION	20	1	2	3	4	5	6	7	-8	>9	10	311	12
X1 · Y	INS CODE BUS	0 Y	ML	JLTIPI	LY			W	3	8/8 X		DE SIM	
-X1 • Y	INS CODE BUS	1 Y	ML	JLTIPI	LY			3	9	8/6 X			
(1 · Y + K _Z , K _W	INS CODE BUS	2 Y	ML	JLTIPI	LY		4	9 W	0	8/8 X			
-X1 • Y + K _Z , K _W	INS CODE BUS	3 Y	ML	JLTIPI	LY		100	8 V/	9	6/6 X		O SUN	
X · Y	INS CODE BUS	5/6 X	0 Y	ML	ILTIPI	Υ	X adf h	a Ansi	tetit er	is to ein	ieinoo s	upissiq	
-X · Y	INS CODE BUS	5/6 X	1 Y		ILTIPI							esigniles raits reigs	
$x \cdot y + K_Z, K_W$	INS CODE BUS	5/6 X	2 Y	ML	ILTIPI							etni vall Stralleri	
$-X \cdot Y + K_Z, K_W$	INS CODE BUS	5/6 X	3 Y	MU	ILTIPI	Y	n Cod	olakrif	3.46	Figur			
X·Y+Z	INS CODE BUS	5/6 X	6 Z	0 Y	MU	LTIP	PLY						
-X · Y + Z	INS CODE BUS	5/6 X	6 Z	1 Y	MU	LTIP	PLY						
$X \cdot Y + K_Z \cdot 2^{-16}$	INS CODE BUS	5/6 X	6	2 Y	MU	LTIP	LY						
-X · Y + K _Z ·2 ⁻¹⁶	INS CODE BUS	5/6 X	6	3 Y	ми	LTIP	PLY						
X • Y + Z, W	INS CODE BUS	5/6 X	6 Z	6 W	0 Y	М	JLTIP	LY					
-X · Y + Z, W	INS CODE BUS	5/6 X	6 Z	6 W	1 Y	М	JLTIP	LY	Dan y		7	T F ASI	
X⋅Y+W _{sign}	INS CODE BUS	5/6 X	6	6 W	2 Y	М	JLTIP	LY			L	1727/18	Vodell.
-X · Y + W _{sign}	INS CODE BUS	5/6 X	6	6 W	3 Y	М	JLTIP	LY					

NOTES: 1) X1 is the previous contents of the first rank of the X register (either old X or a new X).

3) W_{sign} is a single-length signed number, with sign-extension as needed.

Figure 3. Multiplication Codes and Times for 16x16 Multiplication in the 'S516

²⁾ K_Z·2⁻¹⁶ is a single-length signed number comprising the most-significant half of the previous double-length product and here gets added in at the least-significant end of the new result.

⁴⁾ Fractional or integer arithmetic is specified by having the next-to-the-last operand loaded using a 5 or 6 instruction respectively. All rows beginning with "5/6" in effect represent two instructions. 5 does fractional arithmetic and 6 does integer arithmetic.

THE SLOT OF THE SLOT

OPERATION	ns teds become	10 1 , 9	2	3	4	5	6	7	8	9 1	0 1	1 1	2 13	1	4 1	5 1	6	17	18	19	20	21	22	23	3 24
K _Z , K _W /X ₁	INS CODE BUS	4	ang av	No.		g est			-61	DIV	/IDI	e)eo E	HOME	10	RES		q	D) 8	ggri	na	X 19	1	9(19)	BOR	:30 :
K _W /X	INS CODE BUS	5/6 X	4			١,	,l.				DI	VIDE	Ē				Ti.						1		
IZ /V	INS CODE	5/6	5	0.18	31473						J. U	D.13	""										1	1	
K _Z /X	BUS	X	1-									וטו	/IDE		1200000								1'	18	
7 14/7	INS CODE	5/6	6	4				W	LOTE TO	JUNA		0	DIV	0	3.6	y IF					V.	ix		4	
Z, W/X	BUS	X	Z	W									DIVI	DE	8									'	
7/\	INS CODE	5/6	6	5				U	Idir	JUNI		T	30	0	UDI	41				V	Ţ	X-	1	1	
Z/X	BUS	X	Z	_									ļ .	יוכ	/IDI	=								'	
W/X	INS CODE	5/6	6	6	4	T		30	action.	HARA		2	30	0	DI	// 0				28 4	v.	FX			1
VV/A	BUS	X	_	W	_										יוט	טוע	E								1
W /Y	INS CODE	5/6	6	6	5			160	JOIT	33,366		0	30	00	3 8	D	///				1.	LX-			1
W _{sign} /X	BUS	X	0	W	_			- 51			_1	Y		81	JB.	וט	VIL	E	В.				1	L	1

NOTES: 1) X1 is the previous contents of the first rank of the X register (either old X or a new X).

- 2) Fractional division divides a 32-bit 2s-complement number in 1 clock period less than integer division.
- 3) $W_{\mbox{sign}}$ is a single-length signed number, with sign-extension as needed.
- 4) Division operation W_{sign}/X requires that the Z register be initialized with all-zero contents at the time Z is loaded.
- 5) Fractional or integer arithmetic is specified by having the next-to-the-last operand loaded using a 5 or 6 instruction respectively. All rows beginning with "5/6" in effect represent two instructions, one of which does fractional arithmetic and one of which does integer arithmetic.

Figure 4. Division Codes and Times for 32/16 Division in 'S516

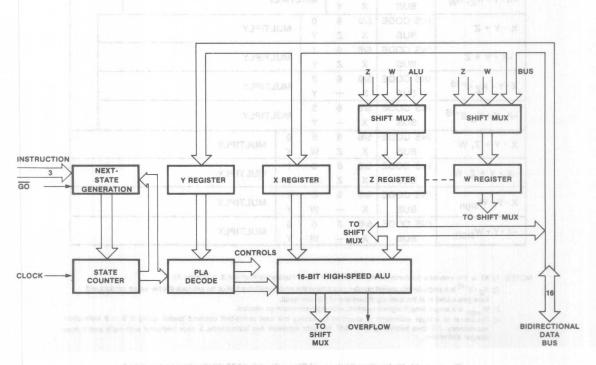


Figure 5. Internal Architecture of the 'S516

11

Initialization

The 'S516 has no direct master reset input. However, initialization of the 'S516 can easily be performed by continually presenting instruction code 7, which after a maximum of 21 clock periods forces the machine back to state 0.

Multiplication

The 'S516 provides 2s-complement 16-bit multiplication, and can also accumulate previously-generated double-length products. No time penalty is incurred for accumulation, since the machine accumulates while the multiplication operation is proceeding. In addition to accumulation, the device can add into a product either a single-length or a double-length number. It can also use a previously-loaded operand as a constant, so that constant multiplication and accumulation is possible.

One key feature is the ability to perform both positive multiplications and negative multiplications, again without any speed penalty. This feature allows complex-arithmetic multiplications to be programmed with very little overhead. Another important feature is the ability to work with either fractions or integers.

Division

The 'S516 also provides a range of division operations. A double-length number in Z,W is divided by X; the result Q is stored in Z, and the remainder R in W. Again all numbers are in the 2s-complement number representation, with the most significant bit of an operand (whether single-length or double-length) having a negative weight. In order to facilitate repeated division, with the multiple-length quotient always keeping the same sign, the remainder is always the same sign as the dividend. Fractional or integer operation is possible, and division and multiplication operations can be concatenated. For example, the operations (AxB)/C,(A+B)/C can easily be performed. The dividend can be any previously-generated result — product, quotient, or remainder; or it may be a double-length or single-length signed operand.

Reading Results

The result of an arithmetic operation, or of a string of operations, can be read onto the 16-bit bus if the machine is at the end of an operation or at the start of a new sequence. The read operation requires that the $\overline{\text{GO}}$ signal be held LOW so that the information is read out onto the bidirectional bus, when code 7 is specified. (See Figure 6.) Since there is a double-length accumulator Z,W, reading can take two cycles. First, register Z is read. After another clock has been received, if code 7 is still present, the least-significant half of the product from the W register is placed on the bus, or likewise the remainder if a division operation had been performed.

If the 'S516 is instructed to perform a read operation during the loading sequence, then the sequence is broken and the machine is forced back to state 0 ready to start the sequence again. Control read operations at state 0 just swap the contents of register Z and W.

Integer and Fractional Arithmetic

The 'S516 can work with either fractional or integer number representations. When working with integers, all numbers are scaled from the least-significant end, and the least-significant bit

is assumed to have a weight of 2^0 . For integer multiplication, accumulation, and division, all numbers are scaled from this least-significant weight, and results are correct if interpreted in this manner. The double-length register Z,W can therefore hold numbers in the range -2^{31} to $+2^{31}$ –1; the operands X and Y, and single-length results, are in the range -2^{15} to $+2^{15}$ –1.

When working with fractions, the machine automatically performs scaling so that input operands and results have a consistent format. All numbers in the fractional representation are scaled from the most significant end, which has a weight of -2^0 (negative). The binary point is one place to the right of this most-significant bit, so that the next bit has a weight of 2^{-1} . The double-length register Z,W therefore holds numbers in the range -1 to $+1-2^{-3}1$ and the operands X and Y and single-length results are in the range -1 to $+1-2^{15}$. Since automatic scaling occurs, the product of two numbers always has the least-significant bit as a 0, unless an accumulation is performed with the least-significant bit being a 1.

During a chain operation with the partial results not being read onto the bus, the '\$516 will stay in either the fractional or integer mode. At the start of a sequence of operations, fractional or integer operation is designated by loading operands using instruction code 5 or instruction code 6 respectively.

Mixed fractional and integer arithmetic is also possible, by redefining the weight of the least-significant or most-significant bits. However, care must be exercised, due to the automatic scaling feature, when fractional arithmetic is programmed.

Rounding

Rounding can be performed on the result of a multiplication or division. Generally rounding would only be called out during fractional operation, but nothing in the 'S516 precludes forming a rounded result during integer arithmetic.

Rounding for multiplication provides the best single-length most-significant half of the product. Rounding occurs at the end of a multiplication, and is performed instead of a Load or Read operation when a code 5 is specified, instead of a code 7, to get from state 8 or state 10 back to state 0. (See Figure 2; also, note that this mode of operation precludes "stealing" a cycle according to the method illustrated in Figure 9.) The 'S516 looks at the most-significant bit of the least-significant half of the product W₁₅, and adds 1 to the most-significant half of the product at the least-significant end if W₁₅ is a 1. After the operation, the 'S516 is in state 0, so that the rounded product can be read, and the W register is cleared.

Rounding for division is performed by forcing the least-significant bit of the quotient in Z to a 1 unless the division is exact (remainder is zero). This method of rounding causes a slightly higher variance in the result than having an additional iterative division operation, but is considerably easier to perform. Again, after rounding the 'S516 goes to state 0, so that a read operation can be performed, and the W register is cleared.

Overflow

The 'S516 has an overflow output OVR which is cleared prior to each operation, and is set during an operation if the product or quotient goes outside the normally-accepted range.

For multiplication, overflow can only occur if the most negative number in the operand range is used: (-1)x(-1)=+1, which cannot be held in the 'S516's internal registers. Overflow can more easily occur during either positive or negative accumulation of products. For fractional arithmetic, if the product or accumulation goes outside the range of -1 to +1-2⁻³¹, then the overflow flipflop will be set.

The overflow flip-flop is enabled in state 8 for the multiply operation or in state 10 for a divide operation. It only gets reset when a transition to state 0 from states 0, 3, 8, 10 and 11, when instruction 7 is being presented to the 'S516.

Overflow may also occur during division if the quotient goes outside the generally-accepted number range of –1 to +1–2⁻¹⁵ during fractional operation. This would occur if the divisor is less than the dividend, or equal to the dividend if a positive quotient is being generated. For integer arithmetic the numbers must be scaled by 2^{15} .

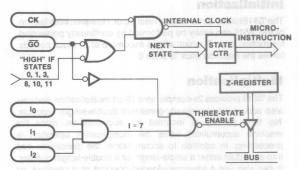


Figure 6. 'S516 Internal Circuitry of "GO" Line and Three-State-Enable

During the states 0, 1, 3, 8, 10 and 11 if the "GO" line (\overline{GO}) is held at logic HIGH then the machine will be in a wait state until \overline{GO} goes to logic LOW.

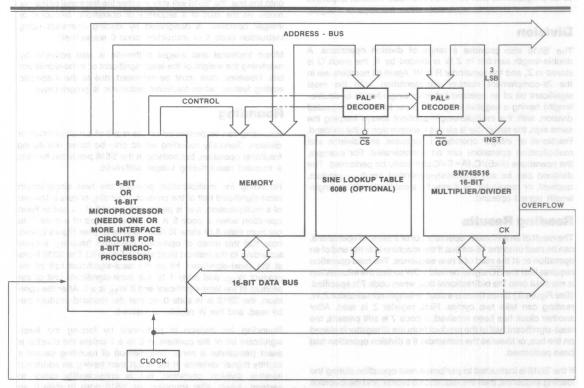


Figure 7. Interfacing the 'S516 to a Microprocessor

Figure 7 shows the block diagram of a microprocessor system with its arithmetic capabilities enhanced by the use of a 'S516 16x16 multiplier/divider. The relatively small number of instruction lines (only 3) of the 'S516 provides a unique way to control the multiplier/divider. As may be seen from Figure 7, these three instruction lines are assigned to the three least-significant bits (LSBs) of the address bus, while the remaining

address bits are decoded by a Programmable Array Logic (PAL®) circuit to determine when the multiplier/divider is selected. For example, suppose the 'S516 is assigned address 100; then any address in the range of 100-107 will enable the 'S516 (i.e., the \overline{GO} line is LOW). Thus, if the address is 100 the 'S516 instruction is 0; if the address is 106 the 'S516 instruction is 6; and so forth.

Data Formats

2-8

2-8

2-24

2-10

2-10

2-9

2-11

2-12

2-27 2-28 2-29 2-30 "0"

91

0

0

0

2-13

2-11 2-12 2-13 2-14

2

2-14

* The least significant bit of W_i is always a binary 0 due to normalization. Note that -1 x -1 yields an overflow in fractional multiply.

2-23

2-5

2-5

2-21

11

2-6

2-6

Integer Multiply

Fractional Multiply
Xi, Y1 - Input, Multiplicand, Multipler

Zi - MS Half Output Product

Wi - LS Half Output Product*

2-2

2-3

Sign

15

Sign

X_i, Y₁ - Input, Multiplicand, Multiplier

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Sign	214	213	212	211	210	29	28	27	26	25	24	23	22	21	20

Zi - MS Half Output Product

15	14	13	12	11	10	9	8	7	6	5	4	3	2	g-1	0
Sign															

Wi - LS Half Output Product**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
215	214	213	212	211	210	29	28	27	26	25	24	23	22	21	20

^{**} The least significant bit of W_i is a valid data bit. Note that 2⁻¹⁵ x 2⁻¹⁵ yields +2³⁰ which can be represented in the output bits without overflowing.

Fractional Divide

Zi - Input Dividend

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Sign	2-1	2-2	2-3	2-4	2-5	2-6	2-7	2-8	2-9	2-10	2-11	2-12	2-13	2-14	2-15

11

													79		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Sign	2-1	2-2	2-3	2-4	2-5	2-6	2-7	2-8	2-9	2-10	2-11	2-12	2-13	2-14	2-15

Zi - Output Quotient

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Sign	2-1	2-2	2-3	2-4	2-5	2-6	2-7	2-8	2-9	2-10	2-11	2-12	2-13	2-14	2-15

W - Output Partial Remainder †

15	14	13	12	11	10	9	8	7	6	5	4	3	2	\$1	0
Sign	2-1	2-2	2-3	2-4	2-5	2-6	2-7	2-8	2-9	2-10	2-11	2-12	2-13	2-14	2-15

† Note that the partial remainder R = 2^{-15} (W)

Integer Divide Example (Z, W)/X

Zi - MSB Input Dividend

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Sign	230	229	228	227	226	225	224	223	222	221	220	219	218	217	216

Wi - LSB Input Dividend

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
215	214	213	212	211	210	29	28	27	26	25	24	23	22	21	20

X - Input Divisor

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Sign	214	213	212	211	210	29	28	27	26	25	24	23	22	21	20

Zi - Output Quotient

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Sign	214	213	212	211	210	29	28	27	26	25	24	23	22	21	20

Wi - Output Partial Remainde

[-
15	14	13	12	11	10	9	8	- /-	6	5	4	3	2	1	0
Sign	214	213	212	211	210	29	28	27	26	25	24	23	22	21	20

Absolute Maximum Ratings

Supply voltage VCC	7.0 V
Input voltage	7.0 V
Off-state output voltage	
Storage temperature -65° to +1	50°C

Operating Conditions

SYMBOL	PARAMETERS	FIGURE	MIN	OMMERCIAL TYP	MAX	UNIT
Vcc	Supply voltage	lov viat	4.75	5	5.25	V
TA	Operating free-air temperature		0 389		45**	°C
fMAX	Clock frequency	8	6			MHz
tCWP	Positive clock pulse width	8	70			ns
tCWN	Negative clock pulse width	8	50			ns
t _{BS}	Bus setup time for inputting data*	8 101	50			ns
t _{BH}	Bus hold time for inputting data*	8	35			ns
tINSS	Instruction, GO setup time	8	10			ns
tINSH	Instruction, GO hold time	8	30			ns

^{*} During operations when the bus is being used to input data.

** This device has a limited operating temperature range.

Electrical Characteristics Over Operating Conditions and V 20 to allogo and all allog a very beneated a great and

SYMBOL	PARAMETER	TEST CONDI	TIONS	MIN TYP	MAX	UNIT
VIL	Low-level input voltage	TU-OS TREF - ME *	tent eith seith is month ei	Autorita over se	0.8	V
VIH	High-level input voltage	a vá benestia trie	Figures 9 timeron 13.	2 worls are	sēlomā	
V _{IC}	Input clamp voltage	V _{CC} = MIN I _I = -18mA			-1.5	V
INCOMENTA GARAGE	Low level input surrent	V - MAY V - 05V	B ₁₅ -B ₀		-250	μΑ
IL	Low-level input current	$V_{CC} = MAX V_{I} = 0.5V$	All other inputs	1	man Silver	mA
I _{IH}	High-level input current	V _{CC} = MAX V _I = 2.4V	transmission and	Total State	250	μΑ
4	Maximum input current	V _{CC} = MAX V _I = 5.5V	and the second second second second second	A STATE OF THE PARTY OF THE PAR	1	mA
VOL	Low-level output voltage	V _{CC} = MIN I _{OL} = 8mA	CO DESCRIPTION OF THE PROPERTY OF	0.3	0.5	V
VOH	High-level output voltage	V _{CC} = MIN I _{OH} = -2mA	and the second second	2.4		V
los	Output short-circuit current*	V _{CC} = MAX V _O = 0V		-10	-90	mA
Icc	Supply current	V _{CC} = MAX		370	450†	mA

^{*} Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

Switching Characterictics Over Operating Conditions

SYMBOL	PARAM	IETER	FIGURE	COMMERCIAL MIN TYP	MAX	UNIT
t _{BO}	Bus output delay from CK C _L = 30 pF	for outputting data;*	8	70	95	ns
YAVAYA	OLIMA SI	FROM I ₂ -I ₀ to bus		30	65	NO SA C
^t PXZ	Output disable delay	From GO to bus		20	40	ns
	Output enable delay;	FROM I ₂ -I ₀ to bus		55	80	
^t PZX	C _L = 30 pF	From GO to bus		25	45	ns
tovr	Overflow output delay from	n CK; C _L = 30 pF	8	odn chang 00 nly wown CK is broth	95	ns

^{*} During operations when the bus is being used to output data.

[†] At cold temperatures see the "I_{CC} vs Temperature" curves on the next page for more complete information. The typical values shown here are at 5.0 V.

Test Waveforms

TEST	V	x*	OUTPUT WAVEFORM -	- MEAS. LEVEL
A II 4		014	Vон —	1.5V
All tpD		0V	V _{OL} —	OF STEMA
tpxz	tpHZ	tpLZ	VOH 0.5V	2.8V
PAZ	0.0V	5.0V	VOL 0.5V	0.0V
	tpZH	tpzL	2.8V	V _{OH}
tPZX	0.0V	5.0V	0.0V	VOL

^{*}At diode; see "Test Circuit" figure below.

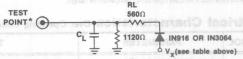
AC Test Conditions

Inputs 0 V_{LOW}, 3 V_{HIGH}. Rise and fall time 1-3 ns from 1 V to 2 V. Measurements are made from 1.5 V_{IN} to 1.5 V_{OUT}, except that t_{PXZ} is measured by a delta in the outputs of 0.5 V from V_{OL} or V_{OH} respectively.

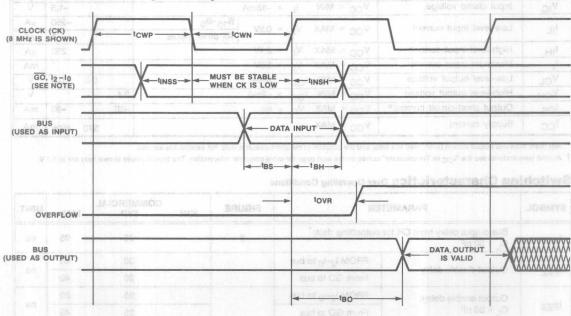
Timing

Timing waveforms are shown in Figure 8. Specific instruction-timing examples are shown in Figures 9 through 13.

Test Load

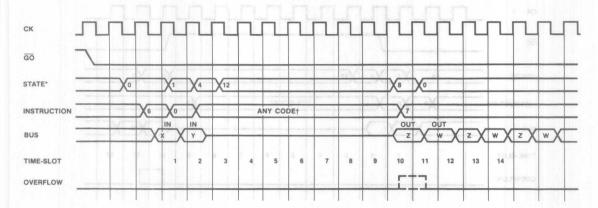


* The "TEST POINT" is driven by the output under test, and observed by instrumentation.



NOTE: GO and I2-I0 can change only when CK is high.

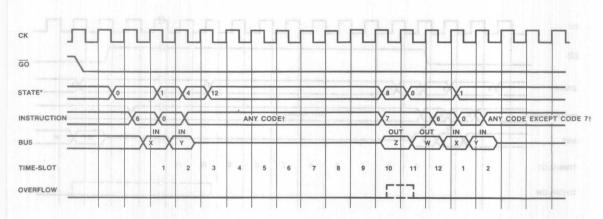
Figure 8. Timing Diagram of the 'S516



NOTES: Register Z is read at the same time that the overflow signal (if present) is set. If the instruction remains at code 7 after time-slot 11, the contents of registers Z and W are swapped each cycle.

†"Any code" means any of code 0 through code 7. However, code 6 will load a new value of X, and code 7 will cause the 'S516 to attempt to drive the data bus. "Not available externally on the 'S516.

Figure 9. Instruction Timing Example No. 1: Load X, Load Y, Multiply, Read Z, Read W. By Presenting Code 7 on the Instruction Lines During the Last Multiply Cycle (State 8), the Results May Be Read During Time-Slots 10 and 11



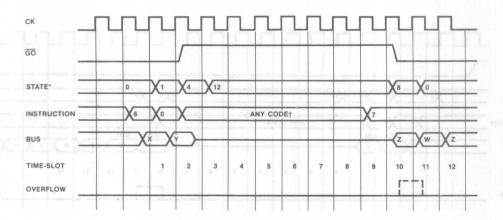
NOTES: The instruction lines may be changed only when CK is high.

†"Any code" means any of code 0 through code 7. Code 6 may be used here since a new X explicitly gets loaded for the next multiply operation. However, code 7 will cause the 'S516 to attempt to drive the data bus.

*Not available externally on the 'S516.

Figure 10. Instruction Timing Example No. 2: Repeat: "Load X, Load Y, Multiply, Read Z, Read W"

11

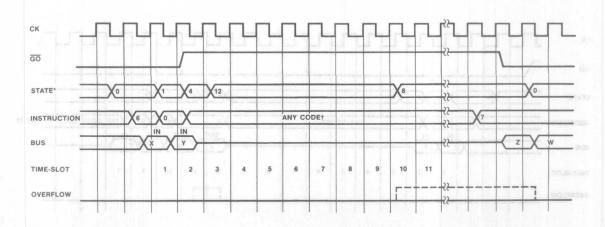


NOTES: Code 7 is given in time-slot 9, but has no effect until time-slot 10 since GO is HIGH. After GO goes LOW in time-slot 10, Z may be read.

†"Any code" means any of code 0 through code 7.

*Not available externally on the 'S516.

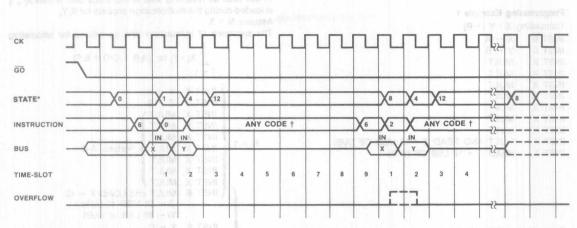
Figure 11. Instruction Timing Example No. 3: Load X, Load Y, Multiply, Read Z, Read W. This Timing Diagram
Corresponds to Table 1. Only After Eight Clock Pulses of the Operation Cycle, the Result Is Read — Z
During Time-Slot 10 and W During Time-Slot 11



NOTES: †"Any code" means any of code 0 through code 7. Code 6 or code 7 may be used here; since GO is HIGH, no new X can be loaded, and the 'S516 cannot attempt to drive the data bus.

*Not available externally on the 'S516.

Figure 12. Instruction Timing Example No. 4: Load X, Load Y, Multiply, Wait, Read Z, Read W



NOTES: This sequence of operations is suitable for use when reading is to be done only at the very end of the operation sequence. The new X value is loaded during the time that the previous multiplication is being performed. See Programming Example #3 for N

$$X = M$$
 Yellowand eaw if an $\sum_{i,j=1}^{N} x_i \cdot Y_i$ fillum surviving as if $X_i \cdot Y_j$ with the property of both solutions of $X_i \cdot Y_j$ and $X_i \cdot Y_j$ with the solution $X_i \cdot Y_j$ and $X_i \cdot Y_j$ and

†"Any code" means any of code 0 through code 7. However, code 7 will cause the 'S516 to attempt to drive the data bus.

*Not available externally on the 'S516.

††Code 6 allows loading of a new X in State 12 and it takes the 'S516 State Counter to State 8. In State 8, Y is loaded via instruction 2 and the next multiply-accumulate cycle is initiated.

Figure 13. Instruction Timing Example No. 5: Sum of Products

11

Programming Examples

In the following examples assume that each line with a separate instruction corresponds to one clock pulse. Instruction codes are 0, 1, 2, 3, 4, 5, 6, 7 and x according to the usage explained in the key to Figure 2.

Programming Example 1

Calculating X · Y (A·B)

INST 6	X - A	
INST 0	Y - B	
INST X	MULT	
INST 7	MULT AND READ Z = 16 MSB OF (A

INST 7 READ W = 16 LSB OF (A·B)

Programming Example 2

Calculating X1 · Y (A·C)

INST 0

INST 7

X1 is a previous multiplier value. It was previously loaded (in example 1) with A.

Y ← C

```
INST X
         MULT
INST X
        MULT
INST 7
         MULT and READ Z = 16 MSB OF (A·C)
```

READ W = 16 LSB OF (A·C)

Programming Example 3

Calculating
$$\sum_{i=1}^{N} X_i \cdot Y_i \quad (A \cdot B + C \cdot D + E \cdot F + \dots)$$

In this case we read only after N multiplications. A new X_{j+1} is loaded during the multiplication process for $X_{j}Y_{j}$. Assume N = 3.

The sequence of instructions and operations for calculating

Programming Example 4

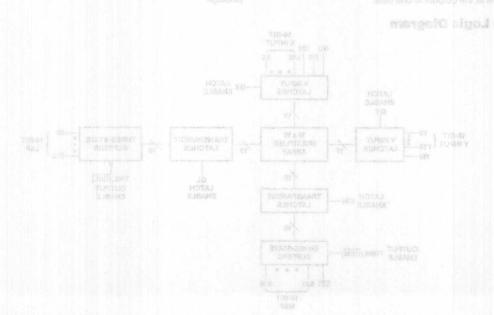
Multiplication plus a constant (A·B + Constant) Assume that the constant is a 32-bit 2s-complement number.

```
INST 6
          X \leftarrow A
INST 6
          Z - C LOAD 16 MSB of constant
          W - D LOAD 16 LSB of constant
INST 6
INST 0
          Y - B
INST X
          MULT
INST X
          MULT
INST X
          MULT
INST X
          MULT
                  Perform A·B + (Z, W)
INST X
          MULT
INST X
          MULT
INST X
          MULT
INST 7
          MULT and READ Z = 16 MSB of (A·B + (C, D))
INST 7
          READ W = 16 LSB of (A·B + (C, D))
```

Programming Example 5

Dividing a 32-bit number by a 16-bit number ((B, C)/A)

```
INST 6
          X \leftarrow A
INST 6
          Z -B
          W-C
INST 4
INST X
INST X
INST X
INST X
INST X
INST X
                    · High-spend 16x15 omaltel maltiplier
INST X
                  · Latched or Longo rent inputs/outputs
INST X
INST X
          Perform Division (Z, W)
INST X
INST X
                   (antiq eloftXm siv) y qqua V 2+ algni3 e
INST X
INST X
INST X
INST X
INST X
                                      Description
INST X
INST X
INST X
          DIVIDE and READ the quotient Z = \frac{(B, C)}{A}
INST 7
                                   (B, C)
          READ the remainder W of
```



16x16 Flow-Thru™ Multiplier Slice 74S556

Features/Benefits

- . Twos-complement, unsigned, or mixed operands
- Full 32-bit product immediately available on each cycle
- High-speed 16x16 parallel multiplier
- · Latched or transparent inputs/outputs
- Three-state output controls, independent for each half of the product
- Single +5 V supply (via multiple pins)
- Available in 84-terminal Leadless-Chip Carrier and 88-Pin-Grid-Array packages

Description

The 'S556 is a high-speed 16x16 combinatorial multiplier which can multiply two 16-bit unsigned or signed twos-complement numbers on every cycle. Each operand X and Y has an associated mode-control line, XM and YM respectively. When a mode-control line is at a LOW logic level, the operand is treated as an unsigned 16-bit number; when the mode-control line is at a HIGH logic level, the operand is treated as a 16-bit signed twos-complement number. Additional inputs RS and RU allow the addition of a bit into the multiplier array at the appropriate bit positions for rounding. The entire 32-bit double-length product is available at the outputs at one time.

Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE	
74S556	P88, L84*	Commercial	

P88 is an 88-Pin-Grid-Array Package.

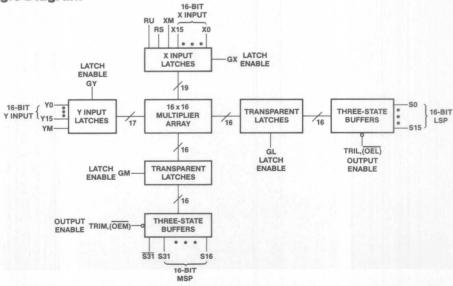
L84 is an 84-terminal Leadless-Chip Carrier Package.

* The 84-terminal leadless chip carrier, L84, and its socket, L84-2, are in development; contact the factory for further details.

The most-significant product bit, S31, is available in both true and complemented form to simplify longer-wordlength multiplications. The product outputs are three-state, controlled by assertive-low enables. The MSP outputs are controlled by the TRIM $(\overline{\text{OEM}})$ control input, while the LSP outputs are controlled by the TRIL $(\overline{\text{OEL}})$ control input. This allows one or more multipliers to be connected to a parallel bus or to be used in a pipelined system.

All inputs and outputs have transparent latches. The latches become transparent when the input to the corresponding gate control line GX, GY, GM, GL is HIGH. If latches are not required, these control inputs may be tied HIGH, leaving the multiplier fully transparent for combinatorial cascading. The device uses a single +5 V power supply, and is available both in an 84-terminal leadless chip carrier (LCC) package and in an 88-pin-grid-array package.

'S556 Logic Diagram



Flow-Thru™ is a trademark of Monolithic Memories

TWX: 910-338-2376

Monolithic MMI

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	SUMMARY OF SIGNALS/PINS
X ₁₅₋₀	Multiplicand 16-bit data inputs
Y ₁₅₋₀	Multiplier 16-bit data inputs
XM, YM	Mode-control inputs for each data word; LOW for unsigned data and HIGH for twos- complement data
S ₃₁₋₀	Product 32-bit output
S ₃₁	Inverted MS product bit (for expansion)
RS, RU	Rounding inputs for signed and unsigned data, respectively
GX	Gate control for X _i , RS, RU
GY	Gate control for Yi
GL	Gate control for least-significant half of product
GM	Gate control for most-significant half of product
TRIL OEL	Three-state control for least-significant half of product
TRIM OEM	Three-state control for most-significant half of products

Rounding Inputs

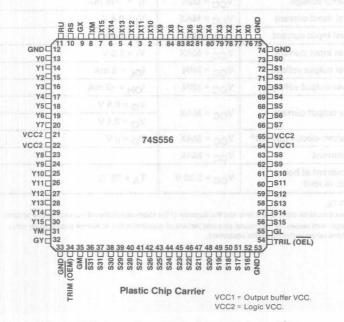
INP	UTS	ADDS		USUALLY L	ISED WITH
RU	RS	215	214	XM	YM.
L	L	NO	NO	X	X
L	Н	NO	YES	H [†]	H [†]
Н	L	YES	NO	L	L
Н	Н	YES	YES	X an * queel	*esi

[†] In mixed mode, one of these could be low but not both.

Mode-Control Inputs

OPERATING MODE	INPUT	CONTRO		
	X ₁₅₋₀	Y ₁₅₋₀	XM	YM
Unsigned	Unsigned	Unsigned	L	L
Minad	Unsigned	Twos-Comp.	L	Н
Mixed	Twos-Comp.	Unsigned	Н	L
Signed	Twos-Comp.	Twos-Comp.	Н	Н

84-Terminal Leadless Chip Carrier Pinout



All V $_{\rm CC}$ and GND pins must be connected to the respective V $_{\rm CC}$ and GND connections on the board and should not be used for daisychaining through the IC.

^{*} Usually a nonsense operation.

Operating Conditions

SYMBOL	PARAMETER	Strom	FIGURE	MIN	COMMERCIAL TYP	MAX	UNIT
Vcc	Supply voltage	SE LIN]		4.75	5	5.25	V
TAX	Operating free-air temperature		WORD)	0	contraction and services	75	°C
t _{S1}	Setup time (X _i , R _i)/Y _i to GX/GY	H J	2a, 2b	10	stati inemak	mee	ns
	Caturations V. V. D. to CM. CI	t _{S2L}	3a, 3b	60	uet 32-bit outpur	Boa A	ns
t _{S2}	Setup time X _i , Y _i , R _i to GM, GL	t _{S2M}		Inversed MS product but (for e 47 laid			115
	Octor time OV OV to OL OM	t _{S3L}	4a, 4b, 4c,	60	ding inputs for sig	Hour	ns
ts3	Setup time GX, GY to GL, GM	t _{S3M}	4d, 4e, 4f	75	respectively		115
t _{H1}	Hold time (X _i , R _i)/Y _i to GX/GY	AND	2a, 2b	8	ic 1 oX to londeds	etelu	ns
t _{H2}	Hold time X _i , Y _i , R _i to GM, GL	t _{H2L} , t _{H2M}	3a, 3b	3	Y vol tostnos	Gata	ns
^t H3	Hold time GX, GY to GM, GL	t _{H3L} , t _{H3M}	4a, 4b, 4c, 4d, 4e, 4f	0		rig to	ns
t _w	Latch enable pulse width		6	12	e-luoni sal lannas solika	sistp	ns

^{*} Indicates case temperature.

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		PARAMETER TEST CONDITIONS		MIN T	TYP† MAX		UNIT	
VIL	Low-level input voltage**						0.8	V		
VIH	High-level input voltage**	. 9	Carrier Pines	gidC sau	2	len	lem	V		
VIC	Input clamp voltage	V _{CC} = MIN	I _I = -18 mA				-1.5	V		
IIL	Low-level input current	V _{CC} = MAX	V _I = 0.4 V				-0.4	mA		
IH	High-level input current	V _{CC} = MAX	V _I = 2.4 V				75	μΑ		
I _I	Maximum input current	V _{CC} = MAX	V _I = 5.5 V	01-01-01-02 01-01-02-03			1	mA		
VOL	Low-level output voltage	V _{CC} = MIN	I _{OL} = 8 mA	ar Dry			0.5	V		
Vон	High-level output voltage	V _{CC} = MIN	I _{OH} = -2 mA	er Dry	2.4			V		
lozL	Off state output oursel	V - MAY	V _O = 0.5 V	81 (36-			-100	μΑ		
lozh	Off-state output current	V _{CC} = MAX	V _O = 2.4 V	95 211			100	μΑ		
los	Output short-circuit current*	V _{CC} = MAX	V _O = 0 V	K D LOSV	-20		-90	mA		
Icc	Supply current	V _{CC} = MAX		astiny		600	800	mA		
Icc	Supply current at hot temperature limit	V _{CC} = 5.25 V	T _A = 75°C	as Igny es grey			700	mA		

^{*} Not more than one output should be shorted at a time and the duration of the short-circuit should not exceed one second.

^{**} These are absolute voltages with respect to the ground pins and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

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Switching Characteristics Over Operating Conditions

SYMBOL	PAR	AMETER	TEST		74S556 COMMERCIAL		UNIT
			CONDITIONS	MIN	TYP	MAX	
^t DTL	Transparent	X _i ,Y _i ,R _i to S ₁₅₋₀ Figs. 1, 2c, 3b, 4c, 4f			və xə 50	76	ns
^t DTM	Multiply GX, GY, GM, GL = H	X _i ,Y _i ,R _i to S ₃₁ ,S ₃₁₋₁₆ Figs. 1, 2c, 3b, 4c, 4f			60	90	ns
^t D1L	Transparent	GX, GY to S ₁₅₋₀ Figs. 2a, 2b, 4d, 4e	CL = 30 pF	NO REST CRAW	* 1	80	ns
^t D1M	Output Multiply GM, GL = H	GX,GY, to S ₃₁ ,S ₃₁₋₁₆ Figs. 2a, 2b, 4d, 4e	RL = 560Ω See figure 7			92	ns
t _{D2}	Transparent Input Multiply GX, GY = H	GM, GL to S _i Figs. 3a, 4a, 4b		X	1-10-10-10-1	35	ns
t _{PXZ}	Three-State Disable Timing	TRIL (OEL), TRIM (OEM) to S _i Fig. 5				30	ns
t _{PZX}	Three-State Enable Timing	TRIL (OEL), TRIM (OEM) to S _i Fig. 5			ral ural	30	ns

Transparent Multiply — Flowthrough Operation

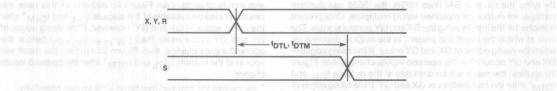
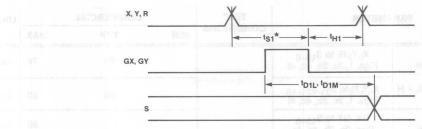


Figure 1

The transparent multiply is a flowthrough operation of the 'S556. Both the input and output latches are made transparent by keeping GX, GY, GM, and GL at a HIGH level. The operands are

the outputs (D.1) and tO.LM, after the observe abute quance

presented to the X, Y, and R inputs; the results are available t_{DTL} and t_{DTM} later, for the least and most significant halves of the product respectively.



* With this particular timing, set-up time t_{S1} will automatically be met.

Figure 2a.

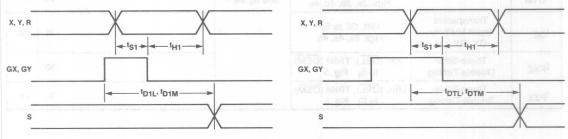


Figure 2b

Figure 2c

By tying the GL and GM lines HIGH, the 'S556 can perform transparent output (or pipelined input) multiplies. Data present is latched at the inputs using the GX and GY control signals. The time at which the result S is present at the outputs depends on when the rising edges of GX and GY occur. If the rising edges of GX and GY occur after the operand inputs change, then Figure 2a applies; the result will be available at the outputs t_{D1L} and t_{D1M}^* after the rising edges of GX and GY. If the rising edges of GX and GY occur less than $(t_{Wmin} - t_{S1min})$ before the operand

and inputs change, then Figure 2b applies; in this case the result will also be available at the outputs $t_{\rm D1L}$ and $t_{\rm D1M}^*$ after the rising edges of GX and GY. However, if the rising edges of GX and GY occur more than $(t_{W\ min}$ -' $t_{\rm S1}\ min)$ before the operand inputs change, then Figure 2c applies; the result will appear at the outputs $t_{\rm DTL}$ and $t_{\rm DTM}^*$ after the operand inputs change.

Transparent Input Multiply — Pipelined Output

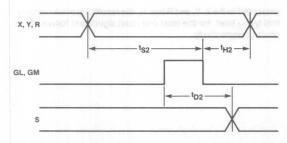


Figure 3a

Figure 3b

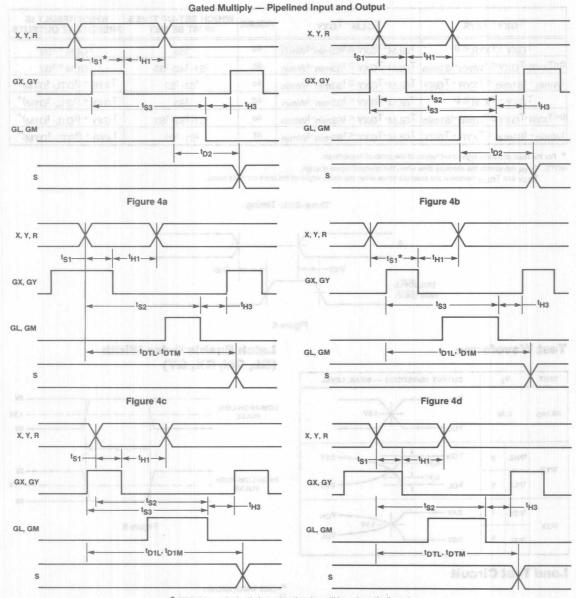
By tying the GX and GY lines HIGH, the 'S556 can perform transparent input (or pipelined output) multiplies. Data is presented at the inputs, and t_{S2} after X, Y and R change, the results can be latched. The time at which the result S is present at the outputs depends upon when the rising edges of GL and GM occur. If they occur at or after $(t_{S2\,min}-t_{Wmin})$ from the inputs

changing, then Figure 3a applies; the result appears at the outputs t_{D2} after the rising edges of GL and GM. If the rising edges of GL and GM occur before ($t_{S2\ min}$ - $t_{W\ min}$) from the inputs changing, then Figure 3b applies; the result appears at the outputs t_{DTL} and t_{DTM}^* after the operand inputs change.

* For the least and most significant halves of the product, respectively.

^{*} For the least and most significant halves of the product, respectively.





* With this particular timing setup time t_{S1} will be automatically met.

Figure 4e

The gated multiply represents the pipelined input and output operation. The latch enable lines GX, GY, GL, GM are used to store incoming operands and outgoing results. The particular set-up times that must be met and the time the result takes to reach the outputs depends on two timing relationships. The first is when the rising edges of GX and GY occur with respect to the operand inputs changing, and the second is when the rising edges of GL and GM occur with respect to the rising edges of GX and GY. On the above timing diagrams, denote the absolute time

Figure 4f

that the operand inputs change as T_{XYR} , the absolute time that the rising edges of GX and GY occur as T_{GXY} , and the absolute time that the rising edges of GL and GM occur as T_{GLM} . Thus, the two delays of concern can be explicitly stated as $(T_{GXY} - T_{XYR})$ and $(T_{GLM} - T_{GXY})$. Notice that either of these quantities can be positive or negative depending on which event occurs first. Timing for gated multiplies can then be summarized in the following table:

T _{GXY} - T _{XYR}	T _{GLM} - T _{GXY}	FIGURE	WHICH SET-UP TIMES MUST BE MET	WHEN RESULT IS PRESENT AT OUTPUT	
T _{GXY} - T _{XYR} ≥ 0	T _{GLM} -T _{GXY} ≥ t _{S3min} -t _{Wmin}	4a	t _{S3}	T _{GLM} + t _{D2}	
0 <t<sub>XYR-T_{GXY} ≤ t_{Wmin}-t_{S1min}</t<sub>	T _{GLM} -T _{GXY} ≥ t _{S3min} -t _{Wmin}	4b	t _{S1} , t _{S2} , t _{S3}	T _{GLM} + t _{D2}	
t _{Wmin} - t _{S1min} < T _{XYR} - T _{GXY}	T _{GLM} -T _{GXY} ≥ t _{S3min} -t _{Wmin}	4c	t _{S1} , t _{S2}	TXYR + (tDTL, tDTM)*	
T _{GXY} - T _{XYR} ≥ 0	TGLM-TGXY < tS3min-tWmin	4d	t _{S3}	T _{GXY} + (t _{D1L} , t _{D1M})*	
0 <t<sub>XYR-T_{GXY} ≤ t_{Wmin}-t_{S1min}</t<sub>	T _{GLM} -T _{GXY} < t _{S3min} -t _{Wmin}	4e	ts1, ts2, ts3	T _{GXY} + (t _{D1L} , t _{D1M})*	
twmin - tS1min < TXYR - TGXY	TGLM-TGXY < tS3min-tWmin	4f	t _{S1} , t _{S2}	TXYR + (tDTL, tDTM)*	

^{*} For the least and most significant halves of the product respectively.

NOTE: TXYR represents the absolute time when the operand inputs change.

TGXY and TGLM represent the absolute times when the rising edges of the latch controls occur.

Three-State Timing

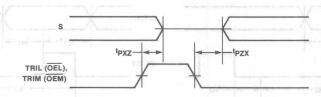
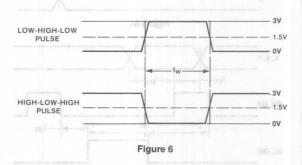


Figure 5

Test Waveforms

TEST	V	X	OUTPUT WAVEFORM — MEAS. LEVEL
All tpD	5.0	ov	VOH 1.5V
tpxz	tpHZ	. 0	VOH 0.5V + 2.8V
TAZ	tpLZ	5	V _{OL} 0.5V + 0.0V
tpzx	^t PZH	0	2.8V V _{OH}
PZX	tpZL	5	0.0V VOL

Latch Enable Pulse Width (GL, GM, GX, GY)



Load Test Circuit

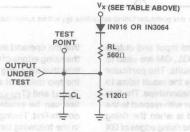


Figure 7

Recommended Bypass Capacitors

The switching currents when the outputs change can be fairly high, and bypass capacitors are recommended to adequately decouple the VCC and GND connections.

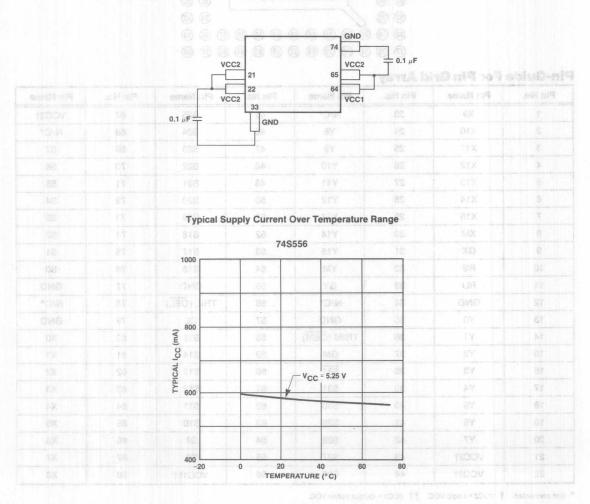
For example, on the 84-terminal LCC package, pins 21 and 22 are VCC2 supplies and should be decoupled with pin 33, a GND input, using a 0.1 μ f monolithic ceramic disk capacitor. The

capacitor must have good high-frequency characteristics. Also pins 64 and 65, VCC1 and VCC2, should be decoupled with pin 74, a GND input, with a similar capacitor arrangement.

For the 88-pin-grid-array package pins 21 and 22 are VCC2 supplies and should be decoupled with pin 35, the GND pin. Pins 66 and 67, VCC1 and VCC2, should be decoupled with pin 77, the GND pin.

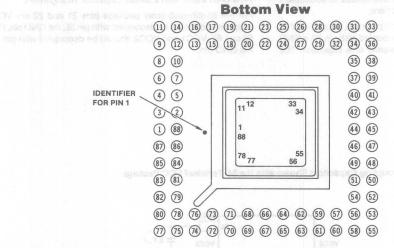


Decoupling Capacitors Shown with the 84-Terminal LCC Package



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88 Pin-Grid-Array Pin Locations



Pin-Guide For Pin Grid Array

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Nam
1	Х9	23	N/C*	45	S25	67	VCC2†
2	X10	24	Y8	46	S24	68	N/C*
3	X11	25	Y9	47	S23	69	S7
4	X12	26	Y10	48	S22	70	S6
5	X13	27	Y11	49	S21	71	S5
6	X14	28	Y12	50	S20	72	S4
7	X15	29	Y13	51	S19	73	S3
8	XM	30	Y14	52	S18	74	S2
9	GX	31	Y15	53	S17	75	S1
10	RS	32	YM	54	S16	76	S0
11	RU	33	GY	55	GND	77	GND
12	GND	34	N/C*	56	TRIL (OEL)	78	N/C*
13	Y0	35	GND	57	GL	79	GND
14	Y1	36	TRIM (OEM)	58	S15	80	X0
15	Y2	37	GM	59	S14	81	X1
16	Y3	38	S31	60	S13	82	X2
17	Y4	39	S31	61	S12	83	Х3
18	Y5	40	S30	62	S11	84	X4
19	Y6	41	S29	63	S10	85	X5
20	Y7	42	S28	64	S9	86	X6
21	VCC2†	43	S27	65	S8	87	X7
22	VCC2†	44	S26	66	VCC1††	88	X8

^{*} Not connected. † VCC2 = Logic VCC. †† VCC1 = Output buffer VCC.

Rounding of being a state were bus a funcion

Multiplication of two n-bit operands results in a 2n-bit product†. Therefore, in a pure n-bit system it is necessary to convert the double-length product into a single-length product. This can be accomplished by truncating or rounding. The following examples illustrate the difference between the two conversion techniques in decimal arithmetic:

Obviously, rounding maintains more precision than truncating, but it may take one more step to implement. The additional step involves adding one-half of the weight of the single-length LSB to the MSB of the discarded part; e.g., in decimal arithmetic rounding 39.28 to one decimal point is accomplished by adding

0.05 to the number and truncating the LSB:

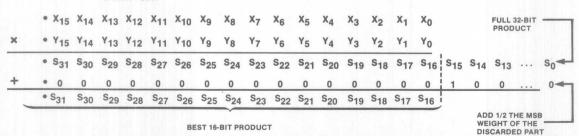
The situation in binary arithmetic is quite similar, but two cases need to be considered; signed and unsigned data representation. In signed multiplication, the two MSBs of the result are identical, except when both operands are –1; therefore, the best single-length product is shifted one position to the right with respect to the unsigned multiplications. Figure 8 illustrates these two cases for the 16x16 multiplier. In the signed case, adding one-half of the $\rm S_{15}$ weight is accomplished by adding 1 in bit position 14, and in the unsigned case by adding 1 in bit position 15. Therefore, the 'S556 multiplier has two rounding inputs. RS and RU. Thus, to get a rounded single-length result, the appropriate R input is tied to $\rm V_{CC}$ (logic High) and the other R input is grounded. If a double-length result is desired, both R inputs are grounded.

†In general multiplication of an M-bit operand by an N-bit operand results in an (M + N)-bit product.

BEST 16-BIT PRODUCT

(b) UNSIGNED MULTIPLY

BINARY POINT



NOTES:

- (a) In signed (twos-complement) notation, the MSB of each operand is the sign bit, and the binary point is to the right of the MSB. The resulting product has a redundant sign bit and the binary point is to the right of the second MSB of the product. The best 16-bit product is from S₃₀ through S₁₅, and rounding is performed by adding "1" to bit position S₁₄.
- (b) In unsigned notation the best 16-bit product is the most significant half of the product and is corrected by adding "1" to bit position S₁₅.

Figure 8. Rounding the Result of Binary Fractional Multiplication

on



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Using the 'S556 in a Pipelined Positive-Edge Triggered Clock System

The 'S556 has internal latches which can be used affectively in systems where things happen on positive-going clock edges. This application is an extension of the gated multiply mode shown in Figure 1, in which a 32-bit product can be latched every ts3 nsec in the 'S556.

If the signals GX, GY, GM and GL can be derived from the system clock then the latches can almost have the same effect as having a register. The basic philosophy behind the recommended timing is that the input latches are closed when the output latches are open; the outputs are then closed (and have

latched results) and new data is presented to the input latches, which are opened. This is shown by the relation between GX, GY and GL, GM in Figure 9. The set-up time t_{S3} is shown as one value but strictly speaking, it is split as t_{S3L} and t_{S3M} for the least significant and most significant half of the product respectively. The value of t_{S3L} is less than t_{S3M} , for applications requiring the least significant bits of the result as fast as possible.

One note of caution is that a design must always meet the set-up and hold times for X_i , R_i with respect to GX and for Y_i with respect to GY.

The result S_i is available t_{D2} after the rising edge of GM and GL.

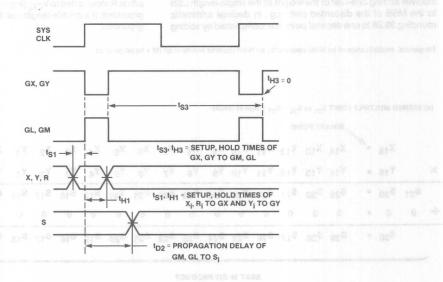


Figure 9

Totally Parallel 32x32 Multiplier

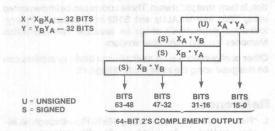
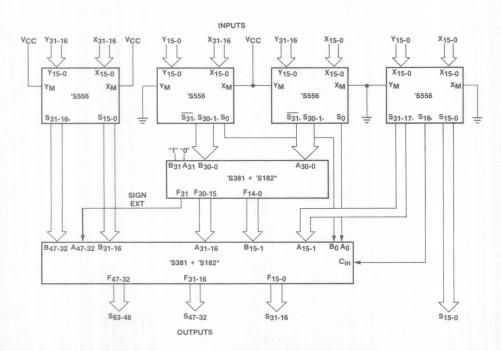


Figure 10. Partial Products for a 32x32 Multiplication

A twos-complement 32x32 multiplication can be performed within 220 nsec using 4 'S556s, 20 'S381s, and 7 'S182s. This 32x32 multiply operation involves adding up four partial products as shown in Figure 10. These four partial products are generated in four multipliers; the outputs are XA*YA, XA*YB, XB*YA, XB*YB, where X31-16 = XB, X15-0 = XA, Y31-16 = YB, Y15-0 = YA.

The implementation of this twos-complement 32x32 multiplier is shown in Figure 11. The outputs of the 16x16 multipliers are connected to two levels of adders to give a 64-bit product. The first level of adders is needed to add the two central partial products of Figure 10, XA*YB and XB*YA. Notice the technique which is used to generate the "sign extension", or the most-significant sum bit of the first level of adders. The 'S556 provides, as a direct output, the complement of the most-significant product bit; having this signal immediately speeds up the sign-extension computation, and reduces the external parts count.



* THESE ARE ADDER BLOCKS USING THE 'S381, A 4-BIT ALU FUNCTION GENERATOR, TO PERFORM A HIGH SPEED ADD OPERATION. THE 'S182 IS A LOOK-AHEAD CARRY GENERATOR WHICH REDUCES THE PROPAGATION DELAY. ALL THE ABOVE PARTS ARE AVAILABLE FROM MONOLITHIC MEMORIES INCORPORATED.

TOTAL MULTIPLY TIME = MULTIPLIER DELAY + ADDER LEVEL 1 DELAY + ADDER LEVEL 2 DELAY = 90 + 65 + 65 = 220 nsec

Figure 11. Implementation of the 32x32 Multiplier

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For example, the inputs to the adder in the most significant position are the $\overline{S31}$ outputs from the two central multipliers. The sign extension of the addition of XA*YB and XB*YA is defined as

SIGN EXT = $\overline{A}.\overline{B}. + \overline{A}.C. + \overline{B}.C.$, where

A is the most-significant bit of the term XA*YB;

B is the most-significant bit of the term XB*YA; and

C is the carry-in to the most-significant bits of XA*YB and XB*YA, in the adder.

The sign extension can be computed as the negation of the carry-out term of three terms, \overline{A} , \overline{B} , and C. This term corresponds to the negative of the carry-out of the bit position just one place to the right of the most-significant bit position of the first level of adders. The negative of the carry-out can be generated by presenting a carry-out and a binary "one" to the most significant bit of the adder. The generated sum bit then corresponds to the negation of the carry-out of the previous stage, which is the sign

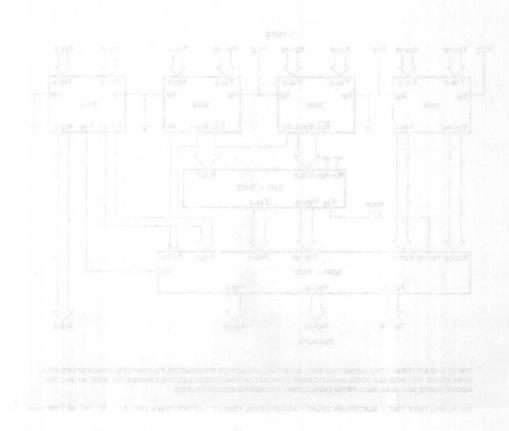
extension required to be added to the 16 most-significant bits of the XB*YB partial product term.

The second level of adders, which performs a 48-bit add function, is fairly straightforward. These adders can be implemented using 'S381 four-bit ALUs and 'S182 carry-bypasses ("carry-lookahead generators") which are available from Monolithic Memories Inc. and from other vendors.

Other configurations such as 48x48 and 64x64 multipliers can be designed using the same methodology, r1.

References

 "Fast 64x64 Multiplication using 16x16 Flow-through Multiplier and Wallace Trees," Marvin Fox, Chuck Hastings and Suneel Rajpal, Monolithic Memories System Design Handbook, pages 8-53 to 8-61.



8x8 High Speed Schottky Multipliers

SN74S557 SN54/74S558

Features/Benefits

- Industry-standard 8x8 multiplier
- Multiplies two 8-bit numbers; gives 16-bit result
- Cascadable; 56x56 fully-parallel multiplication uses only 34 multipliers for the most-significant half of the product
- Full 8x8 multiply in 60ns worst case
- · Three-state outputs for bus operation
- Transparent 16-bit latch in 'S557
- Plug-in compatible with original Monolithic Memories' 67558

Description

The 'S557/'S558 is a high-speed 8x8 combinatorial multiplier which can multiply two eight-bit unsigned or signed twoscomplement numbers and generate the sixteen-bit unsigned or signed product. Each input operand X and Y has an associated Mode control line, X_M and Y_M respectively. When a Mode control line is at a Low logic level, the operand is treated as an unsigned eight-bit number; whereas, if the Mode control is at a High logic level, the operand is treated as an eight-bit signed twos-complement number. Additional inputs, R_S and R_U, (R, in the 'S557) allow the addition of a bit into the multiplier array at the appropriate bit positions for rounding signed or unsigned fractional numbers.

The 'S557 internally develops proper rounding for either signed or unsigned numbers by combining the rounding input R with X_M , Y_M , $\overline{X_M}$, and $\overline{Y_M}$ as follows:

 $R_{11} = \overline{X_M} \cdot \overline{Y_M} \cdot R = Unsigned rounding input to 2⁷ adder.$

 $R_S = (X_M + Y_M) R = Signed rounding input to 2⁶ adder.$

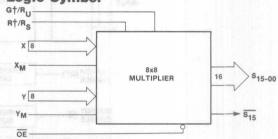
Since the 'S558 has no latches, it does not require the use of pin 11 for the latch enable input G, so R_S and R_U are brought out separately.

The most-significant product bit is available in both true and complemented form to assist in expansion to larger signed multipliers. The product outputs are three-state, controlled by an assertive-low Output Enable which allows several multipliers to be connected to a parallel bus or be used in a pipelined system. The device uses a single +5V power supply and is packaged in a standard 40-pin DIP.

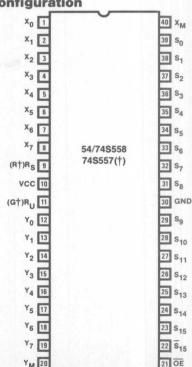
Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
54S558	J, (44), (L)	Military
74S557, 74S558	N,J,	Commercial

Logic Symbol

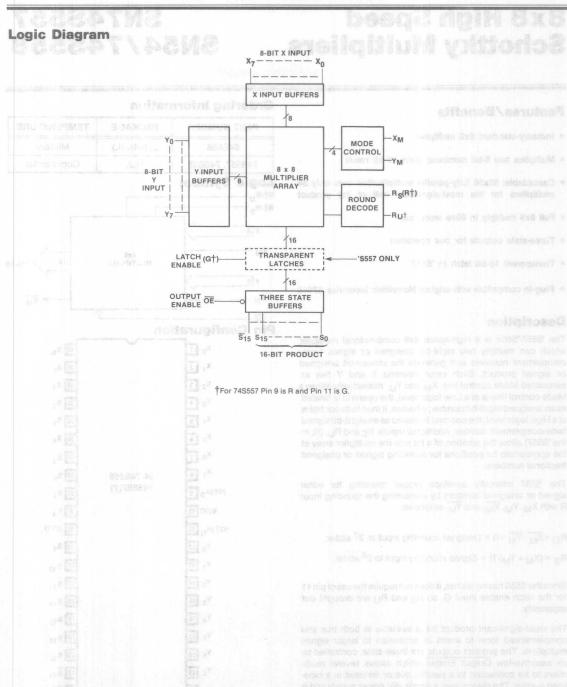


Pin Configuration



†For 74S557 Pin 9 is R and Pin 11 is G.

Monolithic MMI Memories



11

Absolute Maximum Ratings

Supply voltage V _{CC}	7.0 V
Input voltage Off-state output voltage	5.5 V
Storage temperature65° to +1	150° C

Operating Conditions

SYMBOL	PARAMETER	DEVICE	MILITARY			COMMERCIAL			UNITS
STMBUL	PARAMETER	DEVICE	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Vcc	Supply voltage	all	4.5	5	5.5	4.75	5	5.25	٧
TA	Operating free-air temperature	all	-55		125*	0		75	°C
t _{su}	X _i , Y _i to G set	'S557			- 611d	40		3.10	ns
th	X _i , Y _i to G hold time	'S557	VAIT	YYATA	TO THE	0	1178		ns
t _w	Latch enable pulse width	'S557	ANN	MAAV	MANA	15	4/44	MANA	ns

^{*} Case temperature

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS	MIN TYPT MAX	UNIT
V _{IL}	Low-level input voltage			0.8	V
VIH	High-level input voltage	Long Expatt		2	V
VIC	Input clamp voltage	V _{CC} = MIN	I _I = -18mA	-1.5	V
IIL	Low-level input current	V _{CC} = MAX	V ₁ = 0.5V	-1	mA
ΊΗ	High-level input current	V _{CC} = MAX	V ₁ = 2.4V	100	μΑ
I _I	Maximum input current	V _{CC} = MAX	V _I = 5.5V	1	mA
VOL	Low-level output voltage	VCC = MIN	I _{OL} = 8mA	0.5	V
Vон	High-level output voltage	V _{CC} = MIN	I _{OH} = -2mA	2.4	V
OZL	1001 \$ 100=	V MAY	V _O = 0.5V	-100	μΑ
lozh	Off-state output current	V _{CC} = MAX	V _O = 2.4V	100	μΑ
los	Output short-circuit current*	V _{CC} = MAX	V _O = 0V	-20 -90	mA
Icc	Supply current	V _{CC} = MAX		200 280	mA

^{*} Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

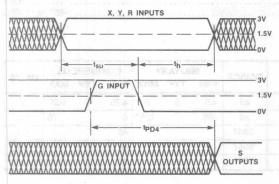
Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	DEVICE	TEST	MILIT.		COMMERC MIN TYP†	MAX	UNIT
^t PD1	X _i , Y _i to S ₇₋₀	All	VE	40	60	40	50	ns
t _{PD2}	X _i , Y _i to S ₁₅₋₈	All	V6.7	45	70	45	60	ns
t _{PD3}	X _i , Y _i to \overline{S}_{15}	All	C _L = 30pF	50	75	50	65	ns
t _{PD4}	G to Si	'S557	$R_L = 560\Omega$. 20	40	20	35	ns
t _{PXZ}	ŌE to S _i	All	see test figures	20	40	20	30	ns
t _{PZX}	OE to Si	All		15	40	15	30	ns

 $[\]dagger$ Typicals at 5.0V V_{CC} and 25°C T_A.

Timing Waveforms

Setup and Hold Times ('S557)

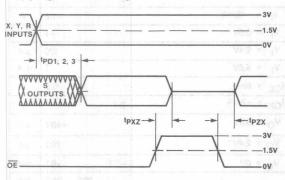


NOTE: If the rising edge of G occurs before (${}^{t}SU_{MIN}^{-t}V_{MIN}$) from the inputs changing, then the applicable propagation delays are ${}^{t}PD_{D}$, ${}^{t}PD_{D}$ and ${}^{t}PD_{D}$, (and not ${}^{t}PD_{D}$). In this case the time at which the results arrive at the outputs depends on when the inputs change instead of when the rising edge of G occurs.

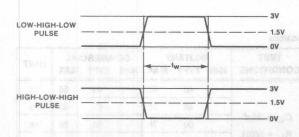
Test Waveforms

TEST	VX		OUTPUT WAVEFORM — MEAS. LEVE	L
All tpD	5.	ov	VOH 1.5V	
tpxz	for tPHZ	for t _{PLZ}		BV
	0.0V	5.0V	V _{OL} 0.5V + 0.	ov
tpzx	for t _{PZH}	for t _{PZL}	2.8V 1.5V	ЭН
ıbZX	0.0V	5.0V	/ _	DL

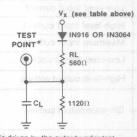
Propagation Delay



Latch-Enable Pulse Width ('S557)

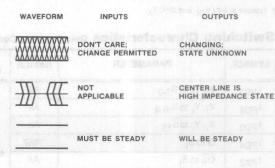


Test Load



* The "TEST POINT" is driven by the output under test, and observed by instrumentation.

Definition of Timing Diagram



SUMMARY OF SIGNALS/PINS						
X7-X0	Multiplicand 8-bit data inputs					
Y ₇ -Y ₀	Multiplier 8-bit data inputs					
X _M , Y _M	Mode control inputs for each data word; LOW for unsigned data and HIGH for twos-complement data					
S ₁₅ -S ₀	Product 16-bit output					
S ₁₅	Inverted MSB for expansion and ambnuon site					
R _S , R _U	Rounding inputs for signed and unsigned data respectively ('S558 only)					
G	Transparent latch enable ('S557 only)					
ŌĒ	Three-state enable for S_{15} - S_0 and $\overline{S_{15}}$ outputs					
R	Rounding input for signed or unsigned data; combined internally with X _M , Y _M ('S557 only)					

senumetet doldw ROUNDING INPUTS bettedoese ast Villibengianu to bengia as 190 \$557

	INPUTS	AD	DS	
ΧM	Y _M	R	27	26
L	L	Н	YES	NO
L bar	e escella Haird and	Har I	NO	YES
gist Hin be	erim to benja	ensiH no	NO NO	YES
ni Hadir	ii eldali H rs si tio	DOM:	NO	YES
X	X	Mene-Entr	NO	NO

som beteroneg ena erudni \$558 ent 1722 ent 11 stallollum

INPUTS		ADDS		USUALLY USED WITH		
RU	RS	27	26	XM	YM	
L	Kay Division	NO	NO	X	X	
oks 1	alieH _{16.2}	NO	YES	si Ht apr	gh-†Hoedar	
H	da igra .	YES	NO	rat of said	Time Farms	
Н	H	YES	YES	*	*	

†In mixed mode, one of these could be Low but not both.
*Usually a nonsense operation. See applications section of data sheet.

74S557 FUNCTION TABLE

INPUTS		PRODUCT RESULT FROM ARRAY	LATCH CONTENTS (INTERNAL TO PART)	OUTPUTS	FUNCTION BE AS AS
ŌĒ	G	Ti	Qi	si	0 0
L	L	X	L H	L H	Latched
L	Н	L H	(L)* (H)*	L H	Transparent
TT	L M 30	X X	(L) (H)	Z Z	Hi-Z; Latched Data not Changed
Н	Н	X	(X)*	Z	Hi-Z

^{*} Identical with product result passing through latch.

MODE CONTROL INPUTS

OPERATING	INPUT	MODE CONTROL INPUTS		
MODE	X7-X0	Y7-Y0	XM	YM
Unsigned	Unsigned	Unsigned	L	L
Mixed	Unsigned	Twos-Comp.	L	Н
Mixed	Twos-Comp.	Unsigned	Н	L
Signed	Twos-Comp.	Twos-Comp.	Н	Н

Functional Description

The 'S557 and 'S558 multipliers are 8x8 full-adder Cray arrays capable of multiplying numbers in unsigned, signed, twoscomplement, or mixed notation. Each 8-bit input operand X and Y has associated with it a mode control which determines whether the array treats this number as signed or unsigned. If the mode control is at High logic level, then the operand is treated as a twos-complement number with the most-significant bit having a negative weight; whereas, if the mode control is at a Low logic level, then the operand is treated as an unsigned number.

The multiplier provides all 16 product bits generated by the multiplication. For expansion during signed or mixed multiplication the most-significant product bit is available in both true and complemented form. This allows an adder to be used as a subtractor in many applications and eliminates the need for certain SSI circuits.

Two additional inputs to the array, R_S and R_U, allow the addition of a bit at the appropriate bit position so as to provide rounding to the best signed or unsigned fractional eight-bit result. These inputs can also be used for rounding in larger multipliers. In the 'S557, these two inputs are generated internally from the mode controls and a single R input.

The product outputs of the multiplier are controlled by an assertive-low Output Enable control. When this control is at a Low logic level the multiplier outputs are active, while if the control is at a High logic level then the outputs are placed in a high-impedance state. This three-state capability allows several multipliers to drive a common bus, and also allows pipelining of multiplication for higher-speed systems.

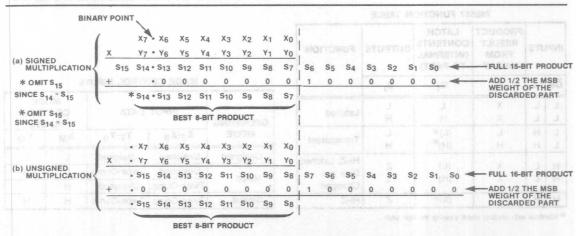
Rounding

Multiplication of two n-bit operands results in a 2n-bit product†. Therefore, in an n-bit system it is necessary to convert the double-length product into a single-length product. This can be accomplished by truncating or rounding. The following examples illustrate the difference between the two conversion techniques in decimal arithmetic:

Obviously, rounding maintains more precision than truncating, but it may take one more step to implement. The additional step involves adding one-half of the weight of the single-length LSB to the MSB of the discarded part; e.g., in decimal arithmetic rounding 39.28 to one decimal point is accomplished by adding 0.05 to the number and truncating the LSB:

The situation in binary arithmetic is quite similar, but two cases need to be considered: signed and unsigned data representation. In signed multiplication, the two MSBs of the result are identical, except when both operands are –1; therefore, the best single-length product is shifted one position to the right with respect to the unsigned multiplications. Figure 1 illustrates these two cases for the 8x8 multiplier. In the signed case, adding one-half of the $\rm S_7$ weight is accomplished by adding 1 in bit position 6, and in the unsigned case 1 is added to bit position 7. Therefore, the 'S558 multiplier has two rounding inputs, $\rm R_S$ and $\rm R_U$. Thus, to get a rounded single-length result, the appropriate R input is tied to $\rm V_{CC}$ (logic High) and the other R input is grounded for the 'S558, and the single R input is grounded for the 'S557.

†In general: multiplication of an M-bit operand by an N-bit operand results in an (M + N)-bit product.



NOTES

- (a) In signed (twos-complement) notation, the MSB of each operand is the sign bit, and the binary point is to the right of the MSB. The resulting product has a redundant sign bit and the binary point is to the right of the second MSB of the product. The best eight-bit product is from S₁₄ through S₇, and rounding is performed by adding "1" to bit position S₆.
- (b) In unsigned notation the best 8-bit product is the most significant half of the product and is corrected by adding "1" to bit position S₇.

Figure 1. Rounding the Result of Binary Fractional Multiplication

Signed Expansion

The most-significant product bit has both true and complement outputs available. When building larger signed multipliers, the partial products (except at the lower stages) are signed numbers. These unsigned and signed partial products must be added together to give the correct signed product. Having both the true and complemented form of the mostsignificant product bit available assists in this addition. For example, say that two signed partial products must be added and MSI adders are used; we then have the situation of adding together the carry from the previous adder stage plus the addition of the two negative most-significant partial-product bits. The result of adding these variables must be a positive sum and a negative carry (borrow). The equations for this are:

where C is the carry-in and A and B are the sign bits of the two partial products.

Now an adder produces the equations:

Examining these equations, it can be seen that, if the inversions of A and B are used, then the most significant sum bit of the adder is the sign extension bit.

Sign ext = AB +
$$\overline{BC}$$
 + \overline{CA} = \overline{AB} + \overline{BC} + \overline{CA} ,

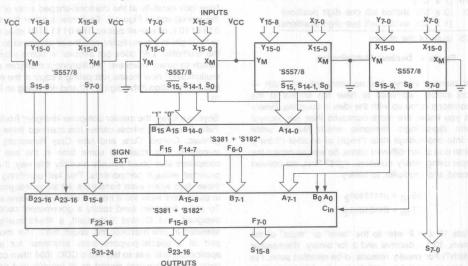
and the sum remains the same.

16x16 Twos-Complement Multiplication

The 16-bit X operand is broken into two 8-bit operands (X7-X0 and X₁₅-X₈), as is the Y operand. Since the situation is that of a cross-product, four partial products are generated as follows:

where the subscript L stands for bits 7-0, ("low or least-significant half), and the subscript H stands for bits 15-8.

Expanded twos-complement multiplication requires a sign extension of the B and C partial products. Thus, B₁₅ and C₁₅ need to be extended eight positions to the left (to align with D₁₅). In this approach two more adders are required. But the complement of the MSB (S₁₅) on the 'S557/8 can be used to save these two adders. Figure 2 shows the implementation of 16x16 signed twos-complement multiplication in this manner.



THESE ARE ADDER BLOCKS USING THE 'S381, A 4-BIT ALU FUNCTION GENERATOR, TO PERFORM A HIGH-SPEED ADD OPERATION. THE 'S182 IS A LOOKAHEAD CARRY GENERATOR AND REDUCES THE PROPAGATION DELAY. ALL OF THE ABOVE PARTS ARE AVAILABLE FROM MONOLITHIC MEMORIES INCORPORATED.

TOTAL MULTIPLY TIME = MULTIPLIER DELAY + ADDER LEVEL 1 DELAY + ADDER LEVEL 2 DELAY = 60 +44+64 = 168 nsec

Figure 2. 16x16 Twos-Complement Signed Multiplication

																	X15	X14	X13	X12	X11	X10	X9	X8	X7	X6	X5	X4	Х3	X2	X1	X ₀
																	Y ₁₅	Y14	Y13	Y12	Y11	Y10	Y9	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Yo
									B ₁₅	B ₁₄	B ₁₃	B ₁₂	B ₁₁	B ₁₀	B9	В8	В7	В6	B5	В4	В3	В2	B ₁	B ₀								
D ₁₅	C	14	D13	D ₁₂	D ₁	1 D10	D9	D8	D ₇	D ₆	D ₅	D4	D ₃	D ₂	D ₁	D ₀	A15	A14	A13	A12	A11	A10	A9	Ag	A7	A6	A ₅	A ₄	Аз	A ₂	A1	A ₀
									C ₁₅	C14	C ₁₃	C ₁₂	C ₁₁	C ₁₀	C9	C ₈	C ₇	C ₆	C ₅	C4	Сз	C ₂	C ₁	Co								
521	9	20 1	200	San	50	7 500	Sar	Saa	San	500	501	San	840	840	S47	840	Ser	See	640	640	644	San	60	60	6-	90	C.	94	Sa	Sa	S1	So

Figure 3. Unsigned Expansions of the 8x8 Multiplier to 16x16 Multiplication

Applications: How to Design Superspeed Cray Multipliers with '558s by Chuck Hastings

Multiplication, as most of us think of it, is performed by repeated addition and shifting. When we multiply using pencil and paper, according to the familiar elementary-school method, we first write down the multiplicand, and then write down the multiplier immediately under it and underline the multiplier. Then we take the least-significant digit of the multiplier, multiply that digit by the entire multiplicand, and record the answer in the top row of our workspace, underneath the line. Then we repeat, using now the second-least-significant multiplier digit, and record that answer below the first one, pushed one digit position (that is, "shifted") to the left. This process continues until we run out of multiplier digits (or out of patience), at which point we add up the constants of the whole diamond-shaped workspace and record at the bottom an answer which consists of either m + n - 1 digits or m + n digits, where there are m digits in the multiplier and n digits in the multiplicand. An example, voila':

```
125 (multiplicand)
x107 (multiplier)

875 (7 x 125)
000 (0 x 125, shifted left one digit position)
125 (1 x 125, shifted left two digit positions)
13375 (sum of the above)
```

Figure 4. Decimal Multiplication

The decimal number system has no monopoly on truth—our ancestors simply happened to have ten fingers at the time when someone came up with the idea of counting. Binary numbers, as you know, are more copacetic than are decimal numbers with digital-logic elements, which like to settle comfortably into one voltage state ("High) or another ("Low"), rather than into one of ten different states. So we can repeat the above example using binary numbers, right? First, we convert our multiplicand and multiplier to binary:

$$125_{10} = 01111101_2$$

 $107_{10} = 01101011_2$

The subscripts 10 and 2 refer to the "base" or "radix" of the number system, 10 for decimal and 2 for binary. (Remember your New Math?) For sneaky reasons to be revealed soon, I've used 8-bit binary numbers, which is one bit more than necessary for my example, and added a leading zero. So, we multiply:

Figure 5. Binary Multiplication

I've left off the remarks this time, but they're just like the remarks in the decimal example, at least in principle. Just in case you doubt this answer, I'll convert it back:

164 0	their re to	
0	0	neal ext. (22 64) stebbs (2M b
		university and (m 128) neo and norther
		(256)
0	d laumore	deliev tee (1 512) be to threat e
01121	1024	
0	0	(2048)
1	4096	
d 1si	8192	
0	0	(16384) aroutong talt
0	0	(32768)
	13375	

Figure 6. Binary-to-Decimal Conversion

Now look carefully at the diamond-shaped array of numbers in the workspace in Figure 5. Each row is either the multiplicand 01111101, or else all zeroes. The 01111101 rows correspond to "1" digits in the multiplier, and the all-zero rows to "0" digits in the multiplier. Life does get simpler in some ways when we switch to binary numbers: "multiplying a multiplier digit by the multiplicand" now means just gating a copy of the multiplicand into that position if the digit is "1," and not doing so if the digit is "0."

Seymour Cray, the master computer designer from Chippewa Falls, Wisconsin, whose career has spanned three companies (Univac, Control Data, and now Cray Research) and many inventions, first observed some time in the late 1950s that computers also could actually multiply this way, if one merely provided enough components. This last qualifying remark; in those days when even transistors, let alone integrated circuits. in computers were still a novelty was by no means a trivial one! To prove his point (and satisfy a government contract), Cray designed, and Control Data built, a 48x48 multiplier which operated in one microsecond, about 1960. This multiplier was part of a special-purpose array processor for a classified application, and was so big that a CDC 1604 (then considered a large-scale processor) served as its input/output controller. In principle, such a multiplier at that time would have had to consist of 48 48-bit full adders or "mills." each of which received one input 48-bit number from the outputs of the mill immediately above it in the array, and the other 48-bit number from a gate which either allowed the multiplicand to pass through, or else supplied an all-zero 48-bit number. Actually, these mills have to be somewhat longer than 48 bits. Anyway, that is at least 2304 full adders, and in 1960 a full-adder circuit normally occupied one small plug-in circuit card.

A later version of this multiplier, in the CDC 7600 super-computer, could produce one 48x48 product out every 275 nanoseconds on a pipelined basis. The pipelining was asynchronous, and the entire humungous array of adders and gating logic could have up to three different products rippling down it at a given instant!

Back to the 1980s. Monolithic Memories has for several years produced an 8x8 Cray multiplier, the 67588, as a single 600-mil 40-pin DIP. After we invented this part, AMD second-sourced it. and by now it has become an industry standard. We now also have faster pin-compatible parts, the 54/74S558 and 74S557. Like other West Coast companies 2,000 miles from Wisconsin and Minnesota where Seymour Cray does his inventing, Monolithic Memories previously used the term "combinatorial multiplier" instead of "Cray multiplier" for this type of part. However, "combinatorial multiplier" has nine extra letters and five extra syllables, and also inadvertently implies that the technique involves combinatorial logic rather than arithmetic circuits. Some West Coast designs, including our 67588, use a modified internal array with only half as many full-adder circuits and slightly different interconnections, based on the two-bit "Boothmultiplication" algorithm (see reference 1), plus the two-bit "Wallace-tree" or "carry-save adder" technique (see references 2 and 3). Conceptually, however, the entire chip or system continues to operate as a Cray multiplier.

The '558, in particular can be thought of as a static logic network which fits exactly the binary multiplication example of Figure 5. (See now why I insisted on using 8-bit binary numbers?) There are no flipflops or latches whatever in the '558 — it is a "flow-through" device. Its 40 pins are used up as follows:

Use of Pins	Input, Output, or Voltage	Number of Pins
Multiplier	THE RESERVE THE PROPERTY OF TH	8
A A. JAindin and	A TULA "ALLA"	0
	iuonio ea Olyci-yms	
Complement of Most-	0	and market have
Significant Bit of Double-		
2 Ctata Outrant Frankla	s and a po the mili	- 4
Number-Interpretation-	t works. For now to 380s and 1180s.	s to stu ² ituo
Rounding Control for Product		
Power and Ground	V	2
		40

Table 1. Use of Pins in the '558

The two number-interpretation-mode control pins, one for the multiplier and one for the multiplicand, allow the format for each of these two 8-bit input numbers to be chosen independently, as follows:

Control Input	Interpretation of 8-bit Input Number
L	8-bit unsigned
bas Hutseilana emeta	7-bit plus a sign bit

Table 2. Mode Control Input Encoding

The two rounding control pins allow either integer (right-justified) or fractional (left-justified) interpretation of the 14-bits-plus-sign double-length product of two 7-bits-plus-sign numbers for internal rounding of the double-length result to the most accurate 8-bit number. The control encoding is:

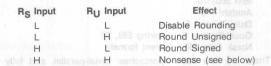


Table 3. Rounding Control Input Encoding

Rounding is normally disabled if the entire 16-bit double-length product output is to be used. If only an 8-bit subset of this product is to be used, this subset can be either bits 15-8 for unsigned rounding as shown in Figure 7, or bits 14-7 for signed rounding as shown in Figure 8. In either case, a "1" is forced into the '558's internal adder network at the bit position indicated by the arrow; adding a "1" into the bit position below the least-significant bit of the final answer has the effect of rounding, as you can see after a little thought. Obviously, forcing a "1" into both of these adder positions at the same time is a nonsense operation for most applications — it adds a "3" into the middle of the double-length result.

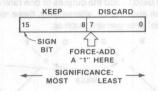


Figure 7. Unsigned Rounding

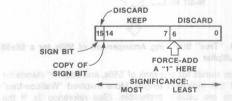


Figure 8. Signed Rounding

By now you probably have a fairly good idea of what a '558 is, and would like a few hints as to how to use it, right? First of all, there is an occasional application in things like video games for very fast multiplication, either 8x8 or 16x16, controlled by an 8-bit microprocessor, where there would be one '558 per system (see reference 4). More typically, however, the '558 is a building block, and several of them are used within one system; in fact, maybe more than several — "many." In the usual Silicon-Valley jargon, we can cascade a number of '558 (8x8) Cray-multiplier chips to create larger Cray multipliers at the systems level.

For the sake of concreteness, I'll discuss the case of 56x56 multipliers, which are appropriate in floating-point units which deal with "IBM-long-format" numbers which have a 56-bit mantissa. Any computer which emulates, or uses the same floating-point format as, any of the following computers can use such a multiplier:

Data General Eclipse Gould/System Engineering SEL 32 Norsk Data 500 (different format)

There are two basic approaches: serial-parallel, and fully parallel. The serial-parallel approach uses seven '558s, and requires seven full multiply-and-add cycles. On the first cycle, the least-significant eight bits of the multiplier are multiplied by the entire multiplicand, and this partial product is saved. On the second cycle, the next-least significant eight bits of the multiplier are multiplied by the multiplicand, and that product (shifted eight bit positions to the left) is added into the first partial product to form the new partial product. And so forth, for five more cycles. It's almost like our decimal-multiplication example of Figure 1, except that instead of base-10 decimal digits we now have base-256 superdigits.

The fully-parallel approach totally applies Cray's usual design philosophy (sometimes characterized as "big, fast, and simple") at the systems level. It uses 49 '558s, in seven ranks; the 'i'th rank performs an operation corresponding to that done during the i'th cycle in the serial-parallel implementation. In principle, a complete mill is used to add the outputs of one rank of '558s to those of the rank above it. Or, alternatively, these mills can be laid out in a "tree" arrangement, such as:

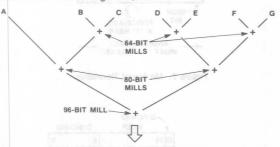


Figure 9. "Tree" Summing Arrangement of Mills for a 56x56 Cray Multiplier

Each letter stands for one rank of '558s, and each "+" stands for a mill of the indicated length. More involved "Wallace-tree" techniques are usually preferable. (See reference 3). If the least-significant half of the double-length product is *never* needed, only 34 'S558s are required. There is one subtlety which needs to be mentioned. If, conceptually, a '558 looks like a diamond —

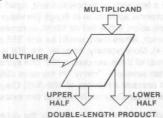


Figure 10. A Single '558 in "Diamond" Notation

then, the 8x56 multiplier for the serial-parallel configuration (which is also one rank of the fully-parallel configuration, which has seven such ranks) looks like this:

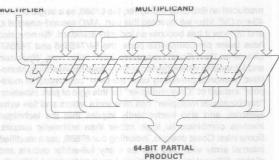


Figure 11. 8x56 Cray Multiplier in "Diamond" Notation

As you may discover after a moment's thought, each slanted double line in Figure 8 calls for addition of the outputs of two '558s — the eight most significant bits of one, and the eight least-significant bits of the next one to the left. There must also be an extra adder (or at least a "half adder") to propagate the carries from this addition all the way over to the left end of the result. The upshot is that an extra 56-bit mill is needed, in addition to the '558s. The eight least-significant bits of the least-significant '558 do not have to go through this mill, since they do not get added to anything else.

One final note: building up a large Cray-multiplier configuration out of '558s requires a *lot* of full adders, or else a lot of something else equivalent to them. Monolithic Memories also makes 74S381 (a 4-bit "ALU" or "Arithmetic Logic Unit") and the 74S182 (a carry-bypass circuit which works well with the '381); and two faster ALUs, the 54/74F381 and the 54/74F382 are in design. These ALUs and bypasses are excellent building blocks from which to assemble the mills used for summation within a rank of '558s, and also the mills used for tree-summation of the outputs of all ranks. For how to put together one of these mills using '381s, '382s, and '182s, see reference 1. For how to use PROMs as Wallace trees, see reference 3.

Now you can go ahead, design your Cray multiplier out of '558s, and start multiplying full-length numbers together in a fraction of a microsecond. Sound like fun?

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- "Doing Your Own Thing in High-Speed Digital Arithmetic," Chuck Hastings, Monolithic Memories Conference Proceedings Reprint CP-102
- "Real-Time Processing Gains Ground with Fast Digital Multiplier," Shlomo Waser and Allen Peterson, *Electronics*, September 29, 1977.
- "Big, Fast and Simple Algorithms, Architecture, and Components for High-End Superminis," Ehud "Udi" Gordon and Chuck Hastings, 1982 Southcon Professional Program, Orlando, Florida, March 23-25, 1982, paper no. 21/3.
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NOTE: All of these references are available as application notes from Monolithic Memories Inc.

1	Introduction	
2	Military Products Division	
3	PROM	
4	PLE™ Devices	
5	PAL® Devices	
6	HAL®/ZHAL™ Devices	
7	System Building Blocks/HMSI™	
8	FIFO	
9	Memory Support	
10	Arithmetic Elements and Logic	
11	Multipliers	
12	8-Bit Interface	
13	Double-Density PLUS™ Interface	
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16	General Information	
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	Schmitt Trigger Input	12-22	314743333	Inverting, 32 mA Output	10 / 54
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	Schmitt Trigger Input	12-22	314743330	Inverting, 32 mA Output	10 54
SN54/74LS245	8-Bit Buffer Transceiver		SN54/74S919.9	8-Bit Diagnostic Register	
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8-Bit Interface Selection Guide

8-Bit Interface

MILITARY PART NUMBER	FUNCTION	POWER	POLARITY	FEATURE
SN54LS240	Buffer	LS	Invert	SARCET
SN54LS241	Buffer	LS	Noninvert	this of Contents Section
SN54LS244	Buffer	LS	Noninvert	Bit Interface Selection S
SN54S240	Buffer	at S	Invert	454L9240 - 6-61t But
SN54S241	Buffer	S	Noninvert	URL 98-8 NASELIAU La vigua NASELIAU
SN54S244	Buffer	ang S	Noninvert	ISAS240 - 8 BITFI
SN54LS245	Buffer Transceiver	LS	Noninvert	4545241 J-BEED
SN54LS273	Register	LS	Noninvert	Master Reset
SN54LS373	Latch	LS	Noninvert	TOTO C. AND TATOLER
SN54S373	Latch	\$3-9 S	Noninvert	miki2 — Sahiri
SN54LS374	Register	LS	Noninvert	un hara - Taga Januari mateka
SN54S374	Register	S	Noninvert	15474LED+1 3-BR BU

12

Pick the Right 8-Bit – or 16-Bit – Interface Part for the Job

Chuck Hastings and Bernard Brafman

Introduction

A few years ago, 20-pin 8-bit buffers, registers, latches, and transceivers came into existence as a rather haphazard upwards evolution from the MSI devices available in the mid-1970s. As time went on, usage of these parts increased until they became one of the fundamental computer-system building-block "primitives"—the "glue" which holds the entire system together. System designers demanded, and semiconductor manufacturers provided, many refinements such as inverting outputs to reduce parts count in assertive-low-bus systems, high-drive outputs to rescue designs with overloaded buses, Schmitt-trigger inputs to likewise rescue designs troubled with severe bus noise, high-voltage outputs specifically suited for driving MOS inputs, seriesresistor outputs for driving highly-capacitive loads such as dynamic-MOS address buses, and so forth.

Today the demands are to reduce component costs and system board area. Reducing parts count achieves both of these objectives at one stroke. With the development of the 300-mil 24-pin SKINNYDIP™ package, it is now possible to effectively incorporate the equivalent of two 20-pin 8-bit interface parts into one 24-pin "16-bit interface" part. The approach is to look for common configurations of pairs of 8-bit parts, and implement the pair as a single chip. Common configurations include back-to-back "registered (or latched) transceivers," with the same options already available in the 20-pin 8-bit parts read back registers or latches, and pipelined registers or latches.

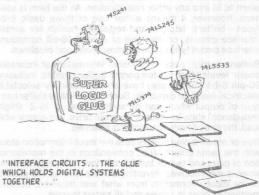
Interface Basics

Where Do Interface Circuits Fit In?

Interface circuits appear as unglamorous bread-and-butter commodity items, as compared to many of the other more complex integrated circuits of today: their sales volume is very high, their average selling price is comparatively low, and essentially interchangeable parts are offered by several suppliers. They have the humble role of being the "glue" which holds digital systems together; they are means rather than ends in themselves.

When preliminary system block diagrams turn into detailed schematics, the blocks turn into complex circuits—microprocessors, multipliers/dividers, automatic dynamics—MOSRAM refresh controllers, high-speed FIFOs, programmable-logic circuits, arithmetic-logic units, and so forth. But then, however, the lines between those blocks turn into interface circuits, which must be there in the final design but never explicitly get noticed during the conceptual-design stage!

The term "interface" is actually a bit of a misnomer, since it implies that these parts always occur at a boundary between two somewhat different types of logic. That may have been true once, and it is still true that many of the circuits commonly called "interface" have inputs and/or outputs which are different electrically from those of, say, triple three-input NAND gates produced using the identical solid-state-circuit technologies. But a general working definition of "interface circuits" also has to cover some other parts which get used



in similar system roles, but have normal inputs and normal totem-pole or three-state outputs. One such definition, current today at Monolithic Memories, is

"... ultra-high performance integrated circuits which do not lend themselves to higher levels of integration, due either to their parallel data structure or to the electrical properties of their inputs and/or outputs."

Interface circuits get used wherever data must be held, transmitted on demand, power-amplified, level-shifted, read from a noisy bus, inverted, or otherwise operated upon in some simple electrical way. If more complex transformations of the data are called for, of a predominantly mathematical rather than electrical nature, the designer will typically try to perform the required operations with readymade LSI or MSI circuits. Even here, of course, interface circuits often have the inconspicuous but crucial role of performing format conversion so that several LSI circuits can communicate with each other. Still, they are viewed as "overhead," which system designers try to minimize and semiconductor producers often rank well below their top level of corporate priorities.

But interface circuits are here to stay, at least for several more years. And the realization is growing among both users and producers of semiconductors that, since interface parts are not about to vanish soon, they need to be treated as something more than afterthoughts to the design process. Users who select interface circuits shrewdly are achieving real gains in system performance and reliability, and significant reductions in system size, weight, and power consumption. Producers who do a conscientious and professional job of developing and marketing these humble parts are finding increased demand for their wares, even during recessions.

Two major trends currently evident in the world of interface circuits are:

- The emergence of an orderly, matrix-like approach to interface products, so that taken all together they form an array rather than simply a splendid jumble of assorted types.
- A strong emphasis on increasing the number of data bits which can be handled or accommodated by a single interfacecircuit package.

This paper will discuss each of these trends in some detail, and will then go on to present some realistic interface applications based on several actual designs.

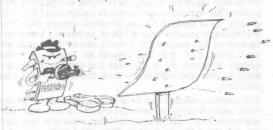
What Kinds of Interface Circuits Are There?

Commonly, the label "interface circuit" is applied to any of a diverse collection of miscellaneous devices which don't seem to fit into any other classification. As the term is used here, however, it means either one of three basic 8-bit types—buffers, latches, and registers—which are simple interface circuits, or else one of several 16-bit compound interface circuit types such as transceivers and pipelines.

Buffers merely "pass" or transmit information at increased power levels. Most contemporary buffer circuits, including 20-pin 8-bit buffers, also have an electronically-selectable electrical-isolation capability. Such a *three-state* buffer has a type of output which can be switched into a "hi-Z" (high-impedance) state in which it does not drive, nor appreciably load, the circuit node to which it is attached.

True or noninverting buffers pass the input information along with the same polarity (i.e., conventions in the representation of ones and zeroes by high and low voltages) that it had when it was received. Inverting buffers reverse the polarity of the input information from what was received, complementing all ones to zeroes and all zeroes to ones.

Most buffers feature standard PNP inputs. However, the 'S/LS340/341/344/310 buffers feature Schmitt-trigger inputs, with a guaranteed 300/400-millivolt deadband (typically twice that) centered about the switching threshold voltage. (This notation is shorthand for "54/74S340, 54/74S341, 54/74S344, 54/74S310, 54/74LS340, 54/74LS341, 54/74LS344 and 54/74LS310," and will be used frequently hereafter.) These Schmitt-trigger buffers won't respond to input noise pulses which would make buffers with normal inputs start to switch, as long as the noise pulses do not completely cross the deadband; thus noise immunity is improved.



"... THE 'LS340/341/344/310 BUFFERS FEATURE SCHMITT-TRIGGER INPUTS, WITH A GUARANTEED... DEADBAND..."

Latches and registers have the same basic capability as buffers, but also have the additional capability that they retain stored information as long as power is supplied to them. Each of these circuit types requires an additional control signal in order to perform its system function.

More specifically, *latches* use an *enable* signal. When this signal is on, they store information, and their outputs do not change even if the information presented to their inputs changes. When their enable signal is off, latches act just like buffers. Turning on the enable signal in effect "freezes" in place whatever information was passing through the latch, so that the latch stores it.

Registers use a clock signal instead of an enable signal. When the clock signal goes through a transition from off to on, this "rising edge" causes the information present at the

inputs to be stored in the register, and then to remain present at the register outputs until another rising edge occurs. When the clock is in a steady-state condition (a "level"), either on or off, or even when the clock goes through a transition from on to off (a "falling edge"), the outputs of the register do not change. Thus, unlike latches, registers lack a mode in which they act exactly like buffers and pass information directly from their inputs to their outputs. This lack is a consequence of the control signal being "edge-sensitive" rather than "level-sensitive"

Transceivers are bidirectional interface circuits capable of interconnecting two buses so that information can pass in either direction. Most of the transceiver parts in production today are buffer transceivers-they are like two crosscoupled buffer circuits within a single 20-pin package. A 16-bit buffer transceiver has eight A-bus data pins and eight B-bus data pins. Either the A-to-B buffers may be enabled. or the B-to-A buffers, or neither; if both sets of buffers were to be enabled, obviously there would be a race condition on each of the data lines, and so the control structure of some buffer transceivers specifically disallows that mode of operation. (Some other types do allow it.) Buffers which are not enabled are, of course, in the hi-Z state. Thus each buffer transceiver interface circuit consists of eight logical elements, and each of these logical elements consists of two simple-buffer elements cross-coupled back-to-back so that the input line for one is the output line for the other and conversely.

Latch transceivers and register transceivers are now positioned to become major factors in the marketplace; several semiconductor houses now offer such devices. In particular, Monolithic Memories now supplies several different families of these devices in the 24-pin 300-mil SKINNYDIP® package; some of these families are also supplied by Texas Instruments. A variety of speeds and architectures are available; see section 12 of this Databook for details.

Pipelines are unidirectional interface circuits having more than one full-width internal latch/register or stage, but typically having just one set of parallel data inputs and one set of parallel data outputs. Two-stage latch pipelines, and both two-stage and four-stage register pipelines, are available. The four-stage devices can store twice as much information per package, but the two-stage devices can be reconfigured more flexibly and have a greater degree of separate control for each stage.

Understanding and Using Interface

How Designers Choose Interface Circuits

In the real world, a digital-logic designer doesn't set out deliberately to use some particular interface circuit whose properties he has carefully learned, in the same way that he might for instance set out to use a bit-slice registered ALU or a multiplier/divider. Rather, as we have said, it is much more likely that it all starts with some innocent-looking little line between two blocks on his preliminary system block diagram which, it turns out, can't really be just a simple little line after all.

Maybe the data which travels on that little line goes away at the source unless the little line is actually also capable of seizing it at the proper time and remembering it. Or maybe the end of the little line is an assertive-low system bus, with enough loads hanging off it to call for almost 30 milliamps of drive capability in whatever contemplates driving the bus, which doesn't quite jibe with the 2-milliamp drive capabilities and assertive-high outputs of the MOS LSI device from which the data is coming.

At this point the designer needs an interface circuit, and—wittingly or unwittingly—he must go through a several-stage decision process to determine what interface circuit he needs to actually implement that little line, before his block diagram can turn into a system. He must also fervently hope that, by the time he gets to the final twig on his decision tree, the interface part he needs will turn out to actually exist. Figure 1 is an example.

A top-down design approach, as illustrated in Figure 1, isn't always wise with integrated circuits, simply because the chances are fairly good that the desperately needed circuit actually won't exist¹. And there was a time, not all that long ago, when only a quasi-random subset of all of the obviously possible variations of the basic interface parts had reached full production status, so that they could be bought and plugged in. The hapless designer just had to memorize what that subset was, and do his design bottom-up from there.

Today, chaos is giving way to order, and enough of the possible interface parts which a designer might want do by now exist (or will exist shortly) that the kind of top-down thought process portrayed in Figure 1 really will work out all right when designing with interface. For instance, the line of interface parts now in production at Monolithic Memories is sufficiently orderly to be organizable into the matrix of the Interface Selection Guide on page 11-3 of this databook. Although this Guide is still somewhat irregular, it is at least recognizable as first-cousin to a logic-design Karnaugh map, and you can actually get your hands on any of the interface parts in the matrix.

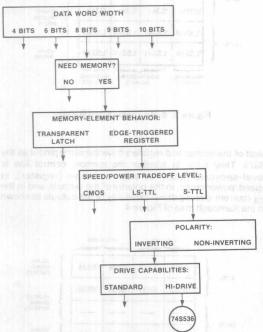


Figure 1. Interface-Circuit-Selection Decision Tree

The dimensions of variation for interface parts in any such Karnaugh map are, of course, two-valued "Boolean" variables. It is realistic from both logical and historical viewpoints to consider that all of the interface parts of the Inter-

face Selection Guide have been derived from a very few basic types, by implementing those combinations which make sense of several two-valued properties of interface parts. These are:

- Commercial versus military temperature-range operation.
- High-speed Schottky (S-TTL) or low-power Schottky (LS-TTL) speed/power range.
- Noninverting or inverting outputs.
- No memory capabilities in the logical elements, so that they operate as buffers; or memory capabilities therein, further subdivided according to whether the logical elements operate as latches or registers.
- Compound 16-bit interface circuits or simple 8-bit interface circuits.
- Hi-drive or standard levels of current-sinking capability (I_{OI}) at the outputs.
- Schmitt-trigger or standard inputs.
- For non-three-state parts, master-reset or clock-enable control inputs.
- Series-resistor or standard outputs.

Obviously, not all imaginable combinations of the above properties actually exist as parts, or would even be useful if they did; and semiconductor houses cannot afford for long to offer 2ⁿ interface-circuit part types for rapidly increasing n. Moreover, certain of the properties which in the past have had just two possible major choices (e.g., S-TTL and LS-TTL) today have more than two; for instance, Section 12 of this Databook includes some CMOS parts.

Nevertheless, by now the matrix approach has been fullyenough implemented to offer a very helpful perspective to the working designer.

Part numbers today allow some of the properties of interface circuits to be directly inferred, at least if the part number follows the conventions of the industry-standard "54/74" numbering series. 54/74 part numbers have a well-defined format VVE4TxxxP, with the following interpretation:

- VV a prefix which varies somewhat from vendor to vendor.
- E4 a temperature-range environmental specification.

 "54" implies the military temperature range (−55°C to +125°C), and "74" the commercial temperature range (0°C to +70°C for several vendors, and 0°C to +75°C for Monolithic Memories). In any case, interface circuits must run properly over a very wide temperature range.
- T a solid-state-circuit technology. Upwards of a dozen of these have been promoted, with widely varying success, during the last decade. The earliest one, plain old gold-doped TTL, omitted using any special letter in part numbers. Today, the two dominant technologies are "S" (high-speed Schottky) and "LS" (Low-power Schottky). Others becoming quite important include "F" (for "FAST," a lower-power form of high-speed Schottky); "ALS" (advanced low-power Schottky); and "SC," "HCT" and "ACT" (isoplanar CMOS processed to be fully TTL-voltage-level compatible).
- xxx a two-digit, three-digit, and today sometimes even four-digit number which uniquely specifies the pinout of the part and its "functional behavior" (see the explanation which follows), independent of speed/ power range.

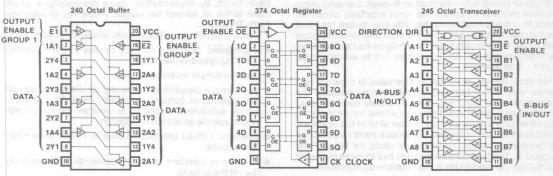
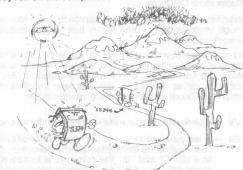


Figure 2. Pinouts for the Three Basic 20-Pin Interface Parts

 P — a package type: plastic, cerdip, flatpack, leadless chip carrier, sidebrazed ceramic, small-outline surface-mount, or whatever.

The functional behavior of a circuit can be defined somewhat circularly as "what a designer needs to know about the circuit in order to construct designs which operate properly using parts from any supplier interchangeably." This definition is akin to one classic definition of computer architecture as "...the structure of the computer a programmer needs to know in order to be able to write any program that will correctly run on the computer." P2



...INTERFACE CIRCUITS MUST
RUN PROPERLY OVER A VERY WIDE TEMPERATURE RANGE ..."

Two parts produced using different solid-state-circuit technologies may exhibit essentially the same functional behavior. If that is the case, and if either part will also satisfy system timing constraints (which is an issue quite separate from that of "functional behavior") and input/output voltage compatibility constraints, the designer does not need to care what kind of internal gates are used within the part—Schottky TTL, ECL, CMOS, NMOS, or water wheels. On the other hand, two parts produced using the same technology may have subtle, or even drastic, differences in their functional behavior; for example, one may have inverting outputs, or hi-drive outputs, or Schmitt-trigger inputs whereas the other does not.

The Matrix of Interface Part Types

The interface parts of the Interface Selection Guide mostly have one of just three different pinouts, shown in Figure 2, in their usual 20-pin plastic or cerdip SKINNYDIP form.

All of the buffers have the same pinout as the 'S240. They differ in speed/power range, in the polarity of the outputs, in the noise-rejection capabilities of the inputs (Schmittrigger or standard), and in enable structure (complementary or assertive-low) as shown in Figure 3, which really is unequivocally a Karnaugh map.

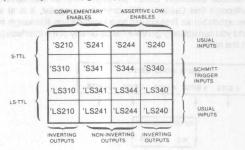


Figure 3. 8-Bit Three-State Buffers

Most of the latches and registers have the same pinout as the 'S374. They differ in whether the memory control line is level-sensitive (latch) or edge-sensitive (register), in speed/power range, in the polarity of the outputs, and in the l_{OL} (current-sinking drive) capability of the outputs as shown in the Karnaugh map of Figure 4.

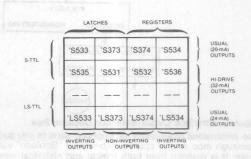
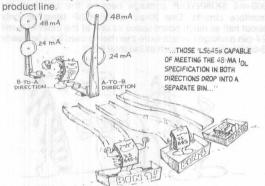


Figure 4. 8-Bit Three-State Latches and Registers

The three transceivers of the Interface Selection Guide are more specifically *buffer transceivers*—compound 16-bit interface circuits like two 8-bit buffer circuits cross-coupled "back-to-back" within a single device. They differ in input-current and output-leakage-current specifications, which here are indistinguishable for test purposes since every data pin is both an input and an output; the 'LS245 specification is tighter. (The 'LS245-1 is also specified as faster, but that is *not* a difference in "functional behavior.") There is also a difference in I_{OL} capability; the 'LS645-1 is specified as higher. Actually, all three devices undergo identical fabrication, and are separated only at final testing; for instance, those 'LS645s capable of meeting the 48-mA I_{OL} specification in both directions drop into a separate bin.

Upcoming developments in interface parts will tend in many cases to follow the matrix approach, at least partially. Even where the new parts do not fit perfectly into the matrix of existing parts, some attention is likely to be paid to issues of balance and symmetry over the entire interface-circuit



In some cases, new interface parts directly "fill in the holes" in the matrix. For instance, some recent additions to Monolithic Memories' line of interface parts are:

Function	Speed/ Power	Polarity	Feature	Part Number
Register	S	Noninv.	Master Reset	SN54/74S273
Register	ed a S	Noninv.	Clock Enable	SN54/74S377 SN54/74S383
Buffer	atik Susta Lance Mo Lance	Noninv.	Series Output Resistor	SN54/74S734*
Buffer	S	Noninv.	Series Output Resistor	SN54/74S731
Buffer	S	Inv.	Series Output Resistor	SN54/74S730
Buffer	S ant else de ant aleme	Inv.	Series Output Resistor	SN54/74S700

NOTES: @—The 'S383' differs from the 'S377 only in having open-collector outputs rather than totempole outputs.

*-The 'S734 is a direct replacement for AMD's Am2966.

Am2966.

#—The 'S730 is a direct replacement for AMD's Am2965.

Table 1. Recent Additions to the Monolithic Memories Interface-Part-Type Matrix



"...THE 'S273 AND 'S377, LIKE THEIR LS-TTL COUNTER-PARTS, ARE DESIGNED WITH STANDARD TTL 'TOTEM-POLE' OUTPUTS..."

The 'S273 and 'S377 bring to higher-performance TTL systems the same functional behavior which has long been available for medium-performance TTL systems, with the popular 'LS273 and 'LS377 parts. The 'S273 and 'S377, like their LS-TTL counterparts, are designed with standard TTL "totem-pole" outputs. Somehow, in the somewhat more chaotic early days of 8-bit interface, the need for high-speed Schottky versions of these parts got overlooked by most interface producers.

Since the 'S273 and 'S377 are totem-pole-output parts, the control pin which gets used on the 'S374 (whose pinout they otherwise follow) for "Output Enable" for the three-state outputs is available for something else. The 'S273 uses it as a "Master Reset" (MR) input, capable of forcing all of the eight D-type flipflops on the chip into the off (low) state simultaneously, regardless of their previous state — or of the state of the clock line and/or the data-input lines. The 'S377, on the other hand, uses that same pin as a "Clock Enable" (CK EN) input, which in effect either allows the clock signal to reach the eight D-type flipflops on the chip, or else cuts it off from reaching the flipflops so that they are not clocked and just sit there holding whatever information they contained previously. The 'S383 is a slight modification of the 'S377 to provide open-collector rather than totem-pole outputs.

The major applications for these parts are in situations where 'S374s would be difficult to control appropriately. Because of the 'S273's MR input, its forte is control applicationsinstruction registers, microinstruction registers, timingpulse registers, and sequential circuits in general, and sometimes as eight individual separate D-type control flipflops in one package. In all of these applications, there has to be a way to force the system into some proper initial state, so that it "starts off on the right foot" and does not get into some unplanned-for, untestable, unpredictable machinepsycho condition on power-up. The 'S377, on the other hand, because of its CK EN input, is the optimum choice for the highest-performance TTL pipeline paths for data, instructions, microinstructions, and address parameters in "overlapped-architecture" machines such as array processors and high-performance minicomputers. Its opencollector counterpart, the 'S383, can be used to drive opencollector buses or to provide wired-OR or wired-AND logic functions

The 'S700, 'S730, 'S731, and 'S734 feature a new type of output stage incorporating a series resistor, designed to efficiently drive highly-capacitative loads such as arrays of dynamic-MOSRAM inputs. Rise and fall times are more

symmetric than with 'S240-type buffers, and the latter need an *external* series limiting resistor for their own protection when driving highly capacitative loads.

Consequently, although 'S240-type buffers may exhibit greater speed when tested under light loading conditions, 'S730-type buffers are likely to perform better under realistic system conditions when driving large distributed capacitative loads is a major factor in the application.

Of these four new buffers, two—the 'S730 and 'S734—are second-source versions of the Am2965 and Am2966 respectively, originally introduced by AMD. The other two—the 'S700 and 'S731—are complementary-enable versions of the 'S730 and 'S734 respectively, just as the 'S210 and 'S241 are complementary-enable versions of the 'S240 and 'S244 respectively. Complementary-enable buffers excel in driving buses with two multiplexed sources for the information, such as instruction addresses and data addresses in a bit-slice bipolar microcomputer system.

The four 'S730-type parts may be grouped with Monolithic Memories' line of conventional and Schmitt-trigger-input buffers in a 2x2 matrix chart or Karnaugh map, with the dimensions of this map chosen to be the polarity of the second-buffer-group enable input E2 (here across the top) and the polarity of the data-buffer logical elements themselves (here down the side), thus:

	ne tote a pole-out	Polarit	y of E2*
	of not federal	E ₂	E ₂
Polarity	Inverting	'LS340 'S240 'S340 'S730	'LS210 'LS310 'S210 'S310 'S700
of Data Buffers	Noninverting	'LS244 'LS344 'S244 'S344	'LS241 'LS341 'S241 'S341 'S731

^{*} Since $\overline{E_1}$ is assertive-low for all of these parts, the parts with an assertive-low $\overline{E_2}$ are "assertive-low-enable" parts, whereas the parts with an assertive-high E_2 are "complementary-enable" parts.

Table 2. 8-Bit Buffers Grouped by Polarity and Enable Structure

By this time, many presently-unused SN54/74xxx part numbers have already been reserved for other potential new parts, even though not all of these parts are yet in production. Nevertheless, it was at least possible to part-number these four series-output-resistor buffers in such a way that the relationship among the four types remains the same as for 'S240-type buffers. To state this another way, one can add 490 to the last three digits of the usual buffer part number to get the part number for the corresponding series-output-resistor part, e.g., 'S241 + 490 = 'S731, etc.

Directions In The Evolution of InterfaceParts

More Bits per Package

Historically, the first interface parts were 16-pin TTL devices offered during the early 1970s, usually with four or six "logi-

cal elements" per package. One "logical element" handles one data bit; in simple interface parts, a logical element may be a buffer, a latch, or a register (with "register" here implying an edge-triggered flipflop).

As the digital-electronics industry shifted from MSI to LSI integrated circuits, and from the quaint and irregular old-time computer word lengths to word lengths which are multiples of eight bits (most often 8, 16, or 32), 8-bit interface devices became the only way to go for simple electrical data transformations—chip counts got intolerably high with 4-bit devices, and 6-bit devices were awkward misfits in most of the newer designs! And, to have eight input data lines, eight output data lines, power and ground, and two control signals, an integrated-circuit package has to have 20 pins.

To conserve board space, the width of this 20-pin package was chosen to be 300 mils (.300") like that of the overwhelming majority of the then-existing bipolar MSI and SSI devices. Hence, during the 1970s, the present 20-pin 300-mil SKINNYDIP package became the standard for interface circuits. One 20-pin SKINNYDIP takes up only about half as much board space as one of the older 600-mil 24-pin packages, which were then being used for a few early 8-bit interface parts such as the Intel 8212.



"... ONE 20-PIN SKINNYDIP" TAKES UP ONLY ABOUT HALF AS MUCH BOARD SPACE AS ONE OF THE OLDER 600-MIL 24-PIN PACKAGES..."

24-pin interface parts were obviously the next major development to come. In the early 1980s, mechanical packaging problems which previously had inhibited the introduction of a 24-pin 300-mil SKINNYDIP were solved, and this package is now also in widespread use for PROMs, PAL programmable-logic circuits, and so forth. So what might one do with four additional pins in an interface part?

One answer is to spend all four of them for additional *control* signals in order to achieve more flexible parts, such as the Monolithic Memories SN54/74LS380 "multifunction" 8-bit register. (See page 6-16 of this databook.) This part is actually implemented with "hard-array logic" technology, and has an internal structure like one form of PAL.

Another answer is to spend all four of them for additional data signals, equally for inputs and outputs. The result is 10-bit interface parts with functionality similar to that of existing 20-pin 8-bit parts.

A middle-of-the-road answer is to divide them equally between control signals and data signals. This approach leads to 9-bit interface parts with improved functionality.

16-bit "double-density" interface-circuits — dual 8-bit circuits in a single 24-pin SKINNYDIP — are a more far-reaching answer than the preceding ones. These circuits use the four extra pins to provide separate control inputs for both 8-bit internal groups, and also to provide improved functionality. The number of data pins is held at 16 by multiplexing the use of two 8-bit groups of input and/or output pins.

The motivation for 16-bit interface parts is, first of all, to cut component counts by replacing two parts with one in as many situations as possible, in order to save board space and assembly costs. Particularly in high-performance computers and array processors, the packaging itself is expensive when it must be designed to provide a proper signal-transmission environment for ultra-fast logic. An almost-50% cut in the board area required for the interface parts—here, as always, the "glue" which holds the whole system together—may result in major indirect savings.

But there are other incentives besides sheer cost reduction which favor cramming as much logic as possible into a given board area. There usually is only one board size in a chassis (or even in a system), and any logic subsystem which cannot fit onto one such board immediately incurs a speed penalty attributable to board-to-board communications—extra buffers for noise-free signal transmission, extra signal-path length on each board over to the edge where the connectors are, more extra length in the backplane wiring, and lots of additional inductance and capacitance permeating all of the above.

So, saving board area is very likely to improve *both* system cost *and* system performance, by increasing the probability that a given logic subsystem will fit onto just one board.

Interface-part internal element density has for many years been increasing at a rate which is, to say the least, unspectacular. Going from four to six to eight to sixteen logical elements in an interface-circuit package doesn't seem like a whole lot, compared for instance to going from 1K to 4K to 16K to 64K to 256K bits in a single dynamic-MOSRAM package in roughly the same number of years.

But, consider what a true LSI interface circuit would have to look like—one with the same magnitude of "equivalent gate count" being bandied about for today's microprocessors, dynamic MOSRAMs, and so forth. First of all, it would need to have several hundred data inputs and several hundred data outputs, so that the most immediately-plausible mechanical design for a package would resemble a sea urchin! And, if it were implemented using any present-day TTL technology, the part would dissipate enough watts to need cooling fins like a Porsche cylinder head!

And so it has turned out that progress over time in increasing the logical-element density for interface parts has been more or less linear, while progress in increasing the level of integration for microprocessors and dynamic MOSRAMs has been more or less exponential. It is no accident that a basic phrase of the definition for "interface circuits" quoted earlier in this paper is "... which do not lend themslves to higher levels of integration ..." If these same density trends continue, digital electronic systems of the future may actually have a higher proportion of packages allocated to interface circuits than is typical today, which if it happens is likely to surprise quite a few people.

Structure of 16-Bit Interface Circuits

Common configurations of two 8-bit interface parts used together furnish a natural starting point for the definition of useful 16-bit interface parts. When the same configuration tends to occur over and over again, it is natural to "draw a boundary around it and put it all on one chip," unless of course the resulting compound chip turns out to need too many pins.

Figure 5 illustrates three such two-part configurations which are observably very common, and intuitively very plausible:

- "Back-to-back" or "cross-coupled." (Figure 5A).
- "Nose-to-tail" or "pipelined." (Figure 5B.)
- "Side-by-side" or "parallel." (Figure 5C.)

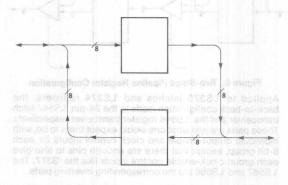


Figure 5A. Back-to-Back Configuration

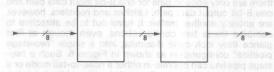


Figure 5B. Nose-to-Tail Configuration

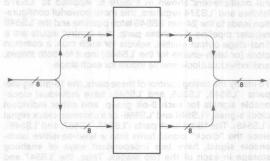


Figure 5C. Side-by-Side Configuration

Figure 5. Common Configurations of Two 8-Bit Interface

The back-to-back configuration, when applied to simple 8-bit buffers, leads to buffer transceivers such as the 'LS245. The 'LS245 is, of course, still a 20-pin part; the choice was made to change its enable structure from that which would be strictly implied by placing two 'LS244s back-to-back, in order to hold the package size to 20 pins and to disallow having both directions simultaneously enabled. These same statements continue to hold for the 'LS645 and 'LS645-1. The 'LS640 and 'LS640-1 are inverting buffer transceivers, and the 'LS643 and 'LS643-1 incorporate an 8-bit inverting buffer back-to-back with an 8-bit noninverting buffer; there are also open-collector equivalents to these parts and the 'LS645 and 'LS645-1. The entire series features the same

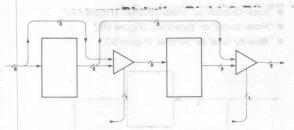


Figure 6. Two-Stage Pipeline Register Configuration

Applied to LS373 latches and 'LS374 registers, the back-to-back configuration leads to the 24-pin 'LS547 latch transceiver and the 'LS546 register transceiver respectively. These parts are just what one would expect them to be, with individual output-enable and clock control inputs for each 8-bit group, except that there are enough pins to also give each group clock-enable control inputs like the 'S377. The 'LS567 and 'LS566 are the corresponding inverting parts.

The nose-to-tail and side-by-side configurations do not lead to anything very interesting with buffers, at least as long as there are only enough pins for one 8-bit input data path and one 8-bit output data path. Latches and registers, however, are entirely another matter. It turns out to be attractive to combine these two configurations, even though at first glance they look quite dissimilar, into a single "two-stage pipeline" configuration as shown in Figure 6. Such a twostage pipeline can operate in either a nose-to-tail mode or a side-by-side mode, according to the setting of the two internal multiplexers shown in Figure 6. Applied to 'LS373 latches and 'LS374 registers, this more powerful configuration leads to the 24-pin 'LS549 latch pipeline and the 'LS548 register pipeline. For these parts, the control inputs are a final-stage output enable, selects for each mux, a common clock (or latch-enable for the 'LS549) input for both stages, and individual clock-enable inputs for each stage.

To clarify the timing control of these parts, the 16-bit register parts ('LS546, 'LS566, and 'LS548) have individual clockenable signals for each 8-bit group, and either individual clock signals ('LS546 and 'LS566) or a common clock signal ('LS548). The 16-bit latch parts ('LS547, 'LS567, and 'LS549), since the "clock" signal turns into a level-sensitive latchenable signal, have two independent ways of enabling storage in each of the two stages. Thus, the 'LS547 and 'LS567 parts feature two separate and equivalent latch-enable control inputs for each 8-bit group, either one of which can cause the group to "latch up" and store information. The 'LS549 part has the same operating mode, except that each 8-bit group has one separate latch-enable control input and there is one more latch-enable input common to both groups. Read-back latches and registers ('LS793 and 'LS794) also have a back-to-back structure; but their "return" element is a buffer (resembling, say, a '244), rather than another latch or register.

As with other TTL 8-bit latches and registers, the part-numbering scheme for all of the parts just mentioned assigns odd numbers to latches and even numbers to registers.

Front-loading latches are one other type of 16-bit interface part. The 'LS646 (noninverting) is to a first approximation an 'LS645 superimposed upon an 'LS546. (The numbering scheme wasn't planned to be that cute—it just happened.) The 'LS648 is a similar inverting part. To clarify what is

mpnops, with a parallelled buffer and flipflop pointing in the A-to-B direction and a similar buffer-flipflop pair pointing in the B-to-A direction. The 'LS646 and 'LS648 are three-state parts: the 'LS647 and 'LS649 are respectively the equivalent open-collector parts. The 'LS651 (inverting) and the 'LS652 (noninverting) are equivalent to the 'LS648 and 'LS646 respectively, but have a different control structure which allows independent enabling of either direction; the 'LS653 and 'LS654 are versions of the 'LS651 and 'LS652 respectively in which the A-direction output buffers are open-collector, and the B-direction buffers are still three-state.

32-bit interface parts are also visible on the horizon. Two four-stage pipelines, the Am29520 and Am29521, are offered by AMD as members of a series of signal-processing parts, and Monolithic Memories is introducing them also as the 'S720 and 'S721. As compared to the 'LS548 and 'LS549, they offer twice as many stored bits per square inch of board, but considerably less flexibility in accessing and controlling register contents.

The matrix approach to classifying various interface parts can be extended to encompass transceivers and pipelines, as is done in Table 3. The correspondence between the various 8-bit simple-interface parts and the 16-bit compound interface parts which are in a sense derived from them, is summarized in Table 4.

Configu- ration	Buffers	Latches		Front- Loading Latches
Simple	210 '310 '240 '340 '241 '341 '244 '344	'373 '531 '533 '535	'374 '532 '534 '536	But, cons look like- count" be
Back-to- Back	'245 '640 '640-1 '643 '643-1 '645 '645-1	'547 '567	'546 '566	'646 '647 '648 '649 '651 '652 '653 '654
Two-Stage Pipeline	dissipata enor	'549	'548	TTu-tach

Table 3. Matrix Classification Scheme for 8-Bit and 16-Bit Interface Parts

Simple Interface Type	Compound Interface Type	Number Of Pins	Buffer	Latch	Regis- ter
at noviemen	Transceivers:	rickling			
'244	'245 '645 '645-1	20			
'240	'640 '640-1	20	X		
'240/'244	'643 '643-1	20	X		
'373	'547	24		X	
'374	'546	24			X
'533	'567	24		X	
'534	'566	24			X
	Pipelines:				
'373	'549	24		X	
'374	'548	24			X

Table 4. Equivalences Between Simple and Compound Interface Types

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Various Applications of Interface Parts

Some Logic-Design Examples

Several illustrative designs using various interface parts may suggest some design insights and some creative ways to use interface. The designs presented have generally been excerpted from actual digital systems.

Reading a switch setting to establish an externally-defined system parameter, such as a device address, is a mundane but essential task in many microprocessor-based systems. Figure 7 illustrates how a group of eight switches may conveniently be read using a byte-wide buffer such as the 'LS244. Since the switches must be electrically isolated from the bus, the 'LS244's three-state outputs are disabled by control signals originated by the microprocessor until the time comes to read in the switch settings. Because the 'LS244 can supply up to 24 milliamps of I_{OL} to drive the bus, this simple scheme can be utilized even on heavily-loaded system data buses.

If still more drive capability is needed, an 'S244 in the same configuration can sink up to 64 milliamps. And, if the system is to be operated in an industrial environment and the switch signals entering the buffer inputs are subject to severe noise, the Schmitt-trigger 'LS344 type of buffer can also be substituted for the 'LS224 with no other change to the circuit.

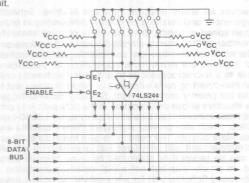


Figure 7. Switch-Setting Readin Circuit

Interfacing two separate buses is a very standard application for transceivers. Figure 8 shows an 'LS245, which has a control structure such that one control signal selects the direction of data transfer and the other one independently allows data transfer to be enabled or disabled. Thus, the two buses can be operated totally isolated from each other, or else either one may be made to follow the other. Depending on the drive-capability and polarity requirements of the application, any of the other buffer transceivers might be used here instead. Or, if memory as well as cross-coupling is required, a latch transceiver or register transceiver might also be used in a similar manner.

Driving a dynamic-MOSRAM address bus with a multiplexed row/column address can conveniently be done with an 'S700 as shown in Figure 9. This part is an inverting complementary-enable buffer with a series-resistor output structure, which is an ideal combination of characteristics here.

First of all, a TTL inverting buffer normally has one less transistor — and hence one less delay — in its internal data path than does an equivalent noninverting buffer, and hence is faster. And dynamic MOSRAMs really don't care if their addresses come in "true" or "complemented" form as long as that form never changes.

Second, a complementary-enable buffer can easily multiplex two different address sources to the same set of outputs without introducing extra switching delay, or allowing a momentary "bus fight" condition, if the same control signal (here $\overline{\text{CAS}}$ or "Column Address Strobe") is tied directly to both $\overline{\text{E}}_1$ and $\overline{\text{E}}_2$ and the two 4-bit groups of outputs are tied together.

Finally, because of the internal series resistor in the S700's output structure, this part (like the S730/1/4) can drive highly capacitative loads, of say up to 70 dynamic-MOSRAM inputs, without the need for external limiting resistors to control undershoot, resulting in a net system speed gain since signal rising and falling transition times remain symmetric. Otherwise, the effective logic delay of the buffer (which is simply the

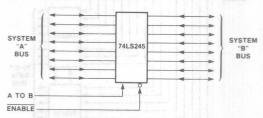


Figure 8. Interfacing Two Separate Buses

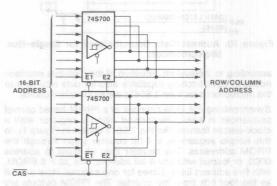


Figure 9. Multiplexed Row/Column Address Drivers

worse of the two transition times) would get degraded, since the use of an external series resistor would have greatly lengthened the low-to-high transition time.

Demultiplexing and holding address and data words for single-bus microprocessors is an application which takes advantage of the strong points of the 'S531 as shown in Figure 10. Since the 'S531 is a "transparent latch" and can operate as a buffer when necessary, the memory system designer can take advantage of the full time slots when the address and data signals are present on the microprocessor outputs. Because the address and data signals are then present for a longer period of time at the 'S531 outputs, it may be possible to use slower (and therefore less expensive!) memory devices than if edge-triggered registers had been used here instead. The three-state outputs of the 'S531 allow the designer to implement bidirectional data buses and DMA address schemes. Variations on this approach can use 'S373s if less drive capability is needed, or LS373s if less speed is needed as well; or 'S535s, 'S533s, or 'LS533s under the same respective circumstances if the address and data buses to be driven are assertive-low

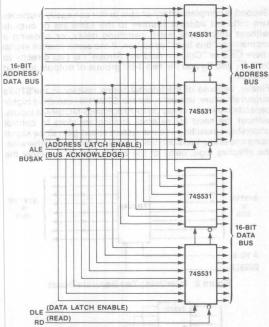


Figure 10. Address/Data Demultiplexer for Single-Bus Microprocessors

according to the system definition. If the data-bus interface needs to have latching capability also for data returning to the microprocessor, then 'LS547s are an excellent choice.

Synchronizing the state changes of a PROM-based control sequencer is easily performed using a register with a clock-enable feature, like the 'LS377 shown in Figure 11. In this simple sequencer, a 4-bit counter steps through the PROM addresses. The counter may be reset to address 0000, or loaded with any 4-bit address. The 32 × 8 PROM, with five address lines, allows for one external input as well as the four bits from the counter. The PROM outputs are pipelined using the 'LS377, which eliminates PROM output glitches, synchronizes the state changes of the sequencer with the system clock, and speeds up the effective cycle time. The availability of enable control inputs on both the counter and the 'LS377 allows forcing "wait" states, where both the counter and the register hold their current state for extended periods of time. If a higher-speed implementation of this design is needed, a 74S161 or 93S16 counter can replace the 74LS161, one of Monolithic Memories' new 63S081A ultra-speed 32x8 PROMs (15 nsec worst-case and 9 nsec typical for tAA, instead of 50 and 37 nsec respectively) can replace the 6331-1, and an 'S377 can replace the 'LS377.

Saving Designs at the Last Minute, or Planning Ahead

Designs hanging out over the edge of unworkability can sometimes be salvaged without any redesign effort, by replacing standard interface parts with hi-drive, Schmitt-trigger-input, or even just inverting pin-compatible parts. Hi-drive parts such as the 'S532 or 'LS645-1 get dropped into 'S374 or 'LS645 sockets respectively late in the design cycle, when the designer suddenly discovers that he has hung several too many inputs on his main system bus. Schmitt-trigger-input parts such as the 'LS341 likewise get

dropped into 'LS241 sockets shortly after the designer has recovered from his first observation of his actual bus waveforms on a good laboratory oscilloscope—it's that or back to the old drawing board. And, when he suddenly remembers after laying out a tightly packed board that "Oh, xxxx, that particular bus is assertive-low," it's nice to be able to simply substitute an 'S534 for an 'S374 in a few places rather than having to find room for several inverter packages. So a designer who has learned to think of interface parts in terms of the matrix approach will now and then find a particularly quick route to saving his skin.

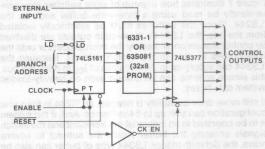


Figure 11. Synchronous PROM-Based Control Sequencer

However, an astute designer may use hi-drive, Schmitttrigger-input, and inverting parts quite deliberately in order to gain speed, economy, drive capability, or noise immunity. A number of the industry-standard buses in the microcomputer world are assertive-low; and inverting buffers, latches. and registers are much more appropriate for connecting these to a microprocessor, or to a bit-slice arithmetic unit. than non-inverting parts with extra inverters in series just to make the polarity come out right. Similarly, Schmitt-trigger hex inverters whose only function in the data path is to provide noise immunity can be eliminated by using 'LS340-type buffers, which also provide significant drive capability and three-state outputs. The need to parallel three-state drivers and registers and split drive lines, just for extra drive capability, can be reduced or eliminated by using hi-drive parts. And, in an obvious but not trivial switch, substituting a high-speed Schottky part for a low-power Schottky equivalent part can beef up drive capability considerably.

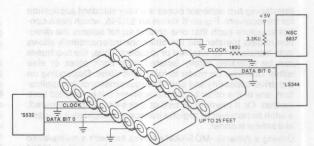
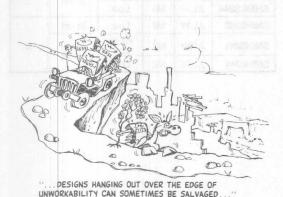


Figure 12. Flat-Cable Transmission Scheme Using Hi-Drive and Schmitt-Trigger-Input Interface Parts

Board-to-board signal transmission via flat cable is a particularly nice application for both hi-drive and Schmitt-triggerinput interface parts. The 32-milliamp outputs of, say, an \$532 are better matched to the characteristic impedance of flat cable (usually 100 to 120 ohms) than 20-milliamp outputs would be. An adequate scheme, in many cases, for the

transmission of data from board to board uses 3M or similar flat cable. Every second cable wire is grounded at both ends for shielding, so that signal wires alternate with ground wires ("signal-ground-signal-ground"), and there is at least one ground wire at each edge of the cable. Signal wires are driven by 32-mA hi-drive latches or registers, and the receivers are Schmitt-trigger-input buffers, and that's all there is to it—no resistors, capacitors, or black magic. For a strobe, clock, or control signal, a linear receiver such as a National Semiconductor 8837 is used together with a 180-ohm series resistor and a 3300-ohm shunt resistor to $V_{\rm CC}$, as shown in Figure 12. This overall scheme is compatible with some Digital Equipment Corporation buses, and is good for transmission distances of up to 25 feet.



Conclusion

Interface parts seem primitive alongside of LSI microprocessors and dynamic MOSRAMs, but they are inescapable and smart designers today have learned how to use them astutely. A powerful aid in doing so is to think of the set of interface parts as an array, which fits into a matrix whose dimensions are various circuit properties. Even though the rate of progress seems slow, the bit-density and functionality of interface parts is steadily increasing, and the time is approaching for designers to learn to take the next logical step and use 16-bit interface parts extensively in their systems, in order both to save cost and to improve overall system performance.

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8-Bit Buffers

SN54LS240 SN54S240 SN54LS241 SN54S241 **SN54LS244** SN54S244

Features/Benefits

- Three-state outputs drive bus lines
- Low current PNP inputs reduce loading
- · 8-bit data path matches byte boundaries
- Ideal for microprocessor interface
- Complementary-enable '241 combines multiplexer and driver functions 1/2 bas 182 drive appeal all-motio8

Description Stangard Mal edit to embedded A" S

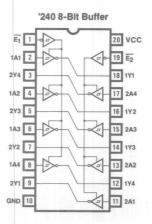
These 8-bit buffers provide high speed and high current interface capability for bus organized digital systems. The threestate drivers will source a termination to ground (up to 133 Ω) or sink a pull-up to VCC as in the popular 220 $\Omega/330~\Omega$ computer peripheral termination. The PNP inputs provide improved fan-in with 0.2 mA III on the low-power Schottky buffers and 0.4 mA III on the Schottky buffers.

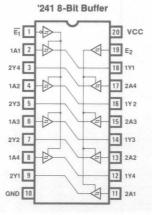
The '240 and '244 provide inverting and noninverting outputs respectively, with assertive low enables. The '241 also provides inverting and noninverting outputs, but with complementary (both assertive-low and assertive-high) enables, to allow transceive or multiplexer operation.

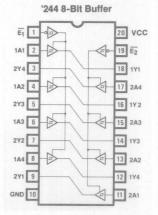
Ordering Information

PART NUMBER	PKG	TEMP	ENABLE	POLARITY	POWER
SN54LS240	J,L,W	Mil	Low	Invert	moe min
SN54LS241	J,L,W	Mil	High- Low	Non- Invert	LS
SN54LS244	J,L,W	Mil	Low	invert	
SN54S240	J,L,W	Mil	Low	Invert	
SN54S241	J,L,W	Mil	High- Low	Non- Invert	S
SN54L244	J,L,W	Mil	Low	mvert	

Logic Symbols







TWX: 910-338-2376

2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2374

Function Tables

'24	10		
1A	2A	17	2Y
L	L	Н	H
L	Н	Н	-saL
Н	L	L	Н

L	L L	L	L	П	Н
L	LS	L	Н	_ H _	- thL
L	L	Н	L.	L	Н
L	L.	H	Н	L	L
L	H	L	X	Н	Z
L	H	H	X	L	Z
H W	L	X	d L	Z	HAH
Н	L	X	H	Z	L
HO	н	- Y	Y	7	7

'241

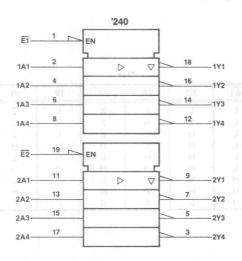
E1	E2	1A	2A	1Y	2Y
L	L	L	X	L	Z
L svi	E	Н	X	Н	Z
L	Н	1-L	L	L	L
L	Н	L	Н	L	H
L	Н	Н	L	Н	L
L	H	H	H.	Н	Н
H	H	X	J L	Z	FASL
Н	Н	X	H	Z	Н
H	L	X	X	Z	Z

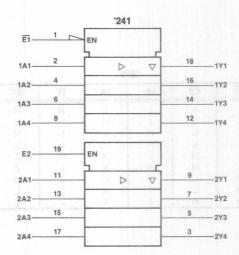
'244

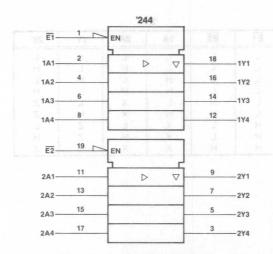
E1	E2	1A	2A	1Y	2Y
L	L	T	L	Ŀ	L
L	L	L	Н	L	Н
Lon	L	Н	L	H	sar L
L	L	Н	H	Н	Н
F sair	H	L	X	L	Z
L	Н	Н	X	Н	Z
H	L	X	L	Z	L
H	L	X	Н	Z	H
H	Н	X	X	Z	Z

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IEEE Symbols







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Absolute Maximum Ratings

Supply voltage V _{CC}	0.5 V to 7 V
Input voltage	1.5 V to 7 V
Off-state output voltage0.	5 V to 5 5 V
Off-state output voltage	5 V 10 5.5 V
Storage temperature -65°C	; to +150°C

Operating Conditions

SYMBOL	PARAMETER	MIN	MILITARY TYP	MAX	UNIT
VCC	Supply voltage	4.5	5 1109 110	5.5	V
TA	Operating free-air temperature	-55	INCE HE COLD OF THE	125	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PAR	AMETER	TEST C	ONDITIONS	MIN	MILITARY	MAX	UNIT	
VIL	Low-level in	put voltage				epanos rugas tuvel	0.7	V	
VIH	High-level in	nput voltage	Am 81-	e il MOM - Sc	2.0	epatiev om -bi	runni I	V	
VIC	Input clamp voltage		V _{CC} = MIN	I _I = -18 mA	y C	(-TAAA) ejuese	-1.5	V	
ΔV_{T}	Hysteresis (V _{T+} -V _{T_})	V _{CC} = MIN	X A37 × con	0.2	0.4	-Monj.	V	
I _{IL}	Low-level in	Low-level input current V _{CC} = N		V _I = 0.4 V	3 kur mermi manı -C		-0.2	mA	
I _{IH}	High-level input current		V _{CC} = MAX			Manuo Jught Star	20	μΑ	
1 ₁	Maximum in	put current	V _{CC} = MAX	V _I = 7 V			0.1	mA	
V _{OL}	Low-level or	utput voltage	V _{CC} = MIN V _{IL} = MAX V _{IH} = 2 V	I _{OL} = 12 mA	ogaslov kratuo lavel-wo.j			V	
Vон	High-level o	High-level output voltage		I _{OH} = -3 mA	2.4	3.4	High	HOV V	
VOH	Tilgii-level o			I _{OH} = -12 mA	2.0			To all	
lozL	011		VCC = MAX	V _O = 0.4 V			-20	μΑ	
IOZH	Off-state ou	tput current	V _{IL} = MAX V _{IH} = 2 V	V _O = 2.7 V	1000	um flumia-tenta lu	20	μΑ	
los	Output shor	t-circuit current*	V _{CC} = MAX	OLSE SEC	-40	matic)	-225	mA	
5		Outputs	4492	'LS240		17 17	27		
		High		'LS241, 'LS244	V 21	17 vi	27		
Am	Supply	Supply Outputs VCC = MA Outputs Open Outputs	VCC = MAX	'LS240	P	26	44	00 m	
'cc	Current			'LS241, 'LS244	et et	ughiC 27	46	mA	
			open	'LS240	200	29	50		
		Disabled	ner van billerie Mira	'LS241, 'LS244	o for is early a H	32	54	nicia tele	

^{*} Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load/Waveforms)	'LS240 MIN TYP MAX			'LS241, 'LS244 MIN TYP MAX		UNIT	
tPLH	Detects and delect			9	14		12	18	ns
tPHL	Data to output delay	C _L = 45 pF R _L = 667 Ω		12	18		12	18	ns
tPZL	Outrot anable delet			20	30	90110	20	30	ns
tPZH	Output enable delay			15	23		15	23	ns
tPZL	Output disable delay	11 08 - 181 - 19 0 F (p)		15	25	NGER U	15	25	ns
tPHZ	Output disable delay	$C_L = 5 pF R_L = 667 \Omega$		10	18	S 2.11 L	10	18	ns

Absolute Maximum Ratings

Supply voltage V _{CC} Input voltage	0.5 V to 7 V
Input voltage	1.5 V to 7 V
Off-state output voltage	-0.5 V to 5.5 V
Storage temperature	65°C to +150°C

Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN TYP MAX			UNIT
Vcc	Supply voltage	4.5	5	5.5	V
TA	Operating free-air temperature	-55	and his and halfs	125	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARA	PARAMETER		TEST CONDITIONS		MILITARY TYP	MAX	UNIT
VIL	Low-level inp	ut voltage					0.8	V
VIH	High-level inp	High-level input voltage						V
VIC	Input clamp v	oltage	VCC = MIN	I _I = -18 mA	11	STELLANDON HAS	-1.2	V
ΔVT	Hysteresis (V	T+-VT_)	VCC = MIN	ri) Millery	0.2	0.4	trigati	V
	Low-level	Any A		1002 - ~	V		-0.4	mA
- IL	input current Any E		V _{CC} = MAX	$V_{CC} = MAX$ $V_I = 0.5 V$		V In 100 fuchi level 4ro 1 -2		
TIH .	High-level input current		VCC = MAX	V _I = 2.7 V	50			μΑ
1	Maximum inpu	ut current	VCC = MAX	V _I = 5.5 V			1	mA
V _{OL}	Low-level outp	out voltage	V _{CC} = MIN V _{IL} = 0.8 V V _{IH} = 2 V	I _{OL} = 48 mA	0.55			V
		V _{CC} = MIN V _{IL} = 0.8 V	I _{OH} = -3 mA	2.4	3.4			
VOH	High-level out	High-level output voltage		I _{OH} =-12 mA	2.0	rano i Jugiuo level	ergilti i	V
lozL	0% -1-11-	0.	V _{CC} = MAX	V _O = 0.5 V			-50	μΑ
lozh	Off-state outp	out current	V _{IL} = 0.8 V V _{IH} = 2 V	V _O = 2.4 V		ciar da fugluo als	50	μΑ
los	Output short-	circuit current†	VCC = MAX	Mark British	-50		-225	mA
y-10 R	S- III	Outputs		'S240	V Sher	80	123	501
		High	-0	'S241, 'S244	82	95	147	
	Supply	Outputs	VCC = MAX	'S240	100		145	A
cc	Current	Low	Outputs	'S241, 'S244	W 31	uota 120	170	mA
Am 311		Outputs	open	'S240	P	100	145	80
0		Disabled	0	'S241, 'S244	80	120	170	

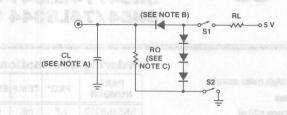
Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load/Waveforms)	'S2		'S241, 'S244			
			MIN TY	P MA	X MIN	TYP	MAX	UNIT
tPLH	Data to output delay	$C_L = 50 \text{ pF} R_L = 90 \Omega$	4.	5	7	6	9	ns
tPHL			4.	5	7	6	9	ns
tPZL	Output enable delay		1	0 1	5	10	15	ns
tPZH			6.	5 10	*	8	12	ns
tPZL	Output disable delay	C _L = 5 pF R _L = 90 Ω	1	0 1	5	10	15	ns
tPHZ					9	6	9	ns

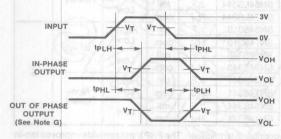
^{*} For the S210 add 2 ns for the E2 (Pin 19) enable.

Test Load

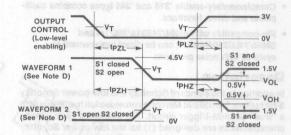


* The "TEST POINT" is driven by the output under test, and observed by instrumentation.

Test Waveforms



Propagation Delay



Enable and Disable

- Notes: A. C_L includes probe and jig capacitance.
 - B. All diodes are 1N916 or 1N3064.
 - C. For Series 54S, R_O = 1 K, V_T = 1.5 V. For Series 54LS, R_O = 5 K, V_T = 1.3 V.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
 Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - E. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
 - F. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz. Z_{OUT} = $50~\Omega$ and: For series 54S, $t_{R}\leq$ 2.5 ns, $t_{F}\leq$ 2.5 ns. For Series 54LS and PAL devices, $t_{R}\leq$ 15 ns, $t_{F}\leq$ 6 ns.
 - G. When measuring propagation delay times of three-state outputs, switches S1 and S2 are closed.

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8-Bit Buffers with Schmitt Trigger Inputs

SN54/74LS310 SN54/74S310 SN54/74LS340 SN54/74S340 SN54/74LS341 SN54/74S341 SN54/74LS344 SN54/74S344

Features

- Schmitt-trigger inputs guarantee high noise margin
- Three-state outputs drive bus lines
- Typical input and output capacitance ≤10 pf
- Low-current PNP inputs reduce loading
- 20-pin SKINNYDIP® saves space
- 8-bit data path matches byte boundaries
- Ideal for microprocessor interface
- Complementary-enable '310 and '341 types combine multiplexer and driver functions
- Pin-compatible with SN54/74S210/240/1/4 and SN54/74LS210/240/1/4; can be direct replacement in systems with noise problems

Description

In addition to the standard Schottky and low-power Schottky 8-bit buffers, Monolithic Memories provides full hysteresis with a "true" Schmitt-trigger circuit. The improved performance characteristics are designed (1) for the low power Schottky buffers, to be consistent with the SN54/74LS Ahex Schmitttrigger inverter, and to guarantee a full 400 m vnoise immunity; (2) for the Schottky buffers, to have low propagation delays, and to guarantee a full 500 my noise immunity. The Schmitt-trigger operation makes these LS/S buffers ideal for bus receivers in a noisy environment.

These 8-bit buffers provide high-speed and high-current interface capability for bus organized digital systems. The threestate drivers will source a termination to ground (up to 133Ω) or sink a pull-up to V_{CC} as in the popular 220Ω/330Ω computer

Ordering Information

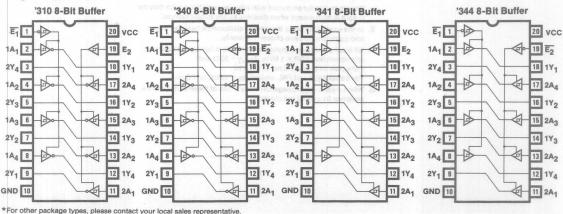
PART NUMBER	PKG*	TEMP	ENABLE	POLARITY	POWER
SN54LS310	J,F	mil	High-		
SN74LS310	N,J	com	Low	Mund	
SN54LS340	J,F	mil	Low	Invert	
SN74LS340	N,J	com	Low		LS
SN54LS341	J,F	mil	High-		LS
SN74LS341	N,J	com	Low	Non-	W 190
SN54LS344	J,F	mil		Invert	
SN74LS344	No	com	Low		
SN54S310	(SLF)	mil	High-	(CY10)	BI
SN74\$310	N,U	com	Low	1	
SN549340	J.E	mil	()	Invert	
SN745340	N,J	com	FOM	N EEA	49-91
SN54S341	J,F	mil	High-		S
SN748341	N,3	com	Low	Non-	
SN54S344	J,F	mil	1.	Invert	29 30 YU
SN745344	N,J	com	Low		THEFT

peripheral termination. The PNP inputs provide improved fan-in With 0.2 mA In for the low-power Schottky buffers and 0.25 mA IIL for the Schottky buffers.

The 340 and 344 provide inverting and non-inverting outputs respectively, with assertive-low enables. The '310 and '341 also provide inverting and non-inverting outputs respectively, but with complementary (both assertive-low and assertive-high) enables, to allow transceiver or multiplexer operation.

All of the 8-bit devices are packaged in the popular 20-pin SKINNYDIP®.

Logic Symbols

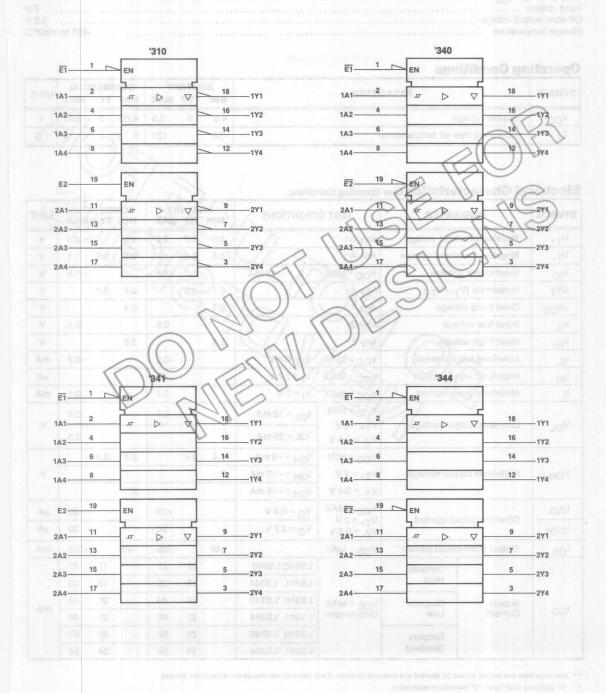


SKINNYDIP® is a registered trademark of Monolithic Memories.

TWX: 910-338-2376 2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2374



IEEE Symbols



Supply voltage V _{CC}	7 V
Input voltage	7 V
Off-state output voltage	
Storage temperature	65° to +150° C

Operating Conditions

SYMBOL	PARAMETER	PVE-	39.	TYP			MMER TYP		UNIT
Vcc	Supply voltage	\$11	4.5	5	5.5	4.75	5	5.25	V
TA	Operating free-air temperature	671	-55	7	125	0	1	75	1.0

Electrical Characteristics Over Operating Conditions

SYMBOL	PAR	AMETER	TEST C	ONDITIONS		TYP MAX		MERCIAL TYP MAX	TINU
V _{T+}	Positive thre	shold voltage	Any A*		1:5	1.7 2.0	1.5	1.7 2.0	V
V _{T-}	Negative thr	Negative threshold voltage		legative threshold voltage Any A* 0.6 0.9 1.1		0.6	0.9 1.1	V	
VIC	Input clamp	Input clamp voltage		I) = -18 mA	1.6	1.5		-1.5	V
ΔV_{T}	Hysteresis (Hysteresis (V _{T+} -V _{T-})			0.4	0.8	0.4	0.8	V
ΔV_{DB}	Dead band voltage		Any A*		0.4		0.4		V
V _{IL}	Input low voltage		Any E		1	0.8		0.8	V
VIH	Input high voltage		Any E*	11/1/	2.0	1/100	2.0		V
I _I L	Low-level input current		VCC MAX	V _I = 0.4 V		-0.2	10	-0.2	mA
Iн	High-level input current		Vec = MAX	V ₁ = 2.7 V	33	20	1/17	7	μΑ
Ч	Maximum in	put current	VCC = MAX	V _I = 7 V	1111	0.1	15.4	0.1	mA
	Low-level output voltage		VCC = MIN	I _{OL} = 12 mA	160	0.4	12	0.4	V
VOL			V _{T+} = 2 V V _{T-} = 0.6 V	I _{OL} = 24 mA	91	9		0.5	\ \ \
rvi-	51	St.		I _{OH} = -3 mA	2.4	3.4	2.4	3.4	12
VOH	High-level o	utput voltage	V _{T+} = 2 V	I _{OH} = -12 mA	2			6	V
			V _{T-} = 0.6 V	I _{OH} = -15 mA		L	2		
lozL		из -53	V _{CC} = MAX	V _O = 0.4 V		-20	- val-	-20	μА
lozh	Off-state out	tput current	$V_{T+} = 2 V$ $V_{T-} = 0.6 V$	V _O = 2.7 V	0	20	100	20	μΑ
los	Output short	-circuit current**	V _{CC} = MAX		-40	-225	-40	-225	mA
15/6	2 1	Outputs	P	'LS310,'LS340	3	17 27	-	17 27	
1 2 2 2		High		'LS341, 'LS344	E	18 35	-	18 35	
la a	Supply	oply Outputs		'LS310, 'LS340		26 44		26 44	ma A
cc	Current			'LS341, 'LS344		32 46		32 46	mA
		Outputs		'LS310, 'LS340		29 50		29 50	
		Disabled		'LS341, 'LS344		34 54		34 54	

^{**} Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

^{* &}quot;A" indicates data input, "E" indicates enable input.

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load/Waveforms)	'LS310, '			41, 'L TYP	S344 MAX	UNIT
tPLH	Data to Output dalay	Terry, 11 presentations	19	25		19	25	ns
^t PHL	Data to Output delay	C - 45 pF B - 667 O	19	25		19	25	ns
t _{PZL}	Output Enable delay	$C_L = 45 \text{pF}$ $R_L = 667 \Omega$	32	40		25	40	ns
^t PZH	Output Enable delay		23	35	510	24	35	ns
t _{PLZ}	Output Disable delay	$C_1 = 5 pF$ $R_1 = 667 \Omega$	18	30		21	30	ns
t _{PHZ}	Output Disable delay	$C_L = 5 pF$ $R_L = 667 \Omega$	15	25	alos y	18	25	ns

Absolute Maximum Ratings

Supply voltage V _{CC}	7.0 V
Input voltage	
Off-state output voltage	
Storage temperature -65° to +15	50°C

Operating Conditions

OVIADOL	/ / AS 1 1 1 21 88 88		MILITARY			COMMERCIAL		
SYMBOL	PARAMETER	MIN T		MAX	MIN	TYP	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
TA	Operating free-air temperature	-55		125	0		75	~°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PAR	AMETER	TEST C	CONDITIONS		TYP		MIN	MER		UNIT	
V _{T+}	Positive three	eshold voltage	Any A*	Any A*			2.05	1,6	1.8	2.0	V	
V _T -	Negative the	reshold voltage	Any A*	7-1	0.8	1.1	1.35	0.8	1.4	1,3	V	
V _{IC}	Input clamp	voltage	V _{CC} = MIN	1) = -18 mA	-7	10	-1.2	5		-1.2	V	
ΔV_{T}	Hysteresis (V _{T+} -V _{T-})	Any A*	1	0.5	0.7	11	0.5	0.7		V	
ΔV _{DB}	Dead band	Dead band voltage		11/2/10	0.15	and the same	1	0.3			V	
VIL	Input low vo	oltage	Any E		123	County)	0.8	1/	1/	0.8	V	
VIH	Input high v	oltage	Any E*		2.0			2.0	/		V	
IIL	Low-level input current		VCC = MAX	V _I = 0.5 V	Y A	71	-0.25			-0.25	mA	
IH	High-level in	put current	VCC = MAX	V = 2.7 V		U	50			50	μΑ	
Ц	Maximum in	put current	Vec = MAX	V ₁ = 5.5 V			1			1	mA	
VOL	Low-level output voltage		VC = MIN	I _{OL} = 48 mA			0.55				V	
OL			V _T = 0.8 V	IOL = 64 mA						0.55		
			V = MINI	I _{OH} = -1 mA		. Carl San	Vien.	2.7				
			V _{CC} = MIN	I _{OH} = -3 mA	2.4	3.4		2.4	3.4			
VOH	High-level o	utput voltage	V _{T+} = 2 V	I _{OH} = -12 mA	2						V	
			V _T -= 0.8 V	I _{OH} = -15 mA				2				
lozL	04 -1-1-		V _{CC} = MAX	V _O = 0.5 V		1 1210	-50			-50	μΑ	
lozh	Orr-state ou	tput current	V _{IH} = 2.0 V V _{IL} = 0.8 V	V _O = 2.7 V			50			50	μΑ	
los	Output short-circuit current**		V _{CC} = MAX		-50		-225	-50		-225	mA	
		Outputs		'S310,'S340		50	80		50	80		
		High		'S341, 'S344		80	130		80	130		
	Supply	Outputs	V _{CC} = MAX	'S310, 'S340		110	155		100	155		
Icc I	Current	Low	Outputs open	'S341, 'S344		130	180		130	185	mA	
		Outputs		'S310, 'S340		135	180	11.8	135	180		
		Disabled	No. of the last of	'S341, 'S344		155	180		150	200		

^{**} Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

[&]quot;A" indicates data input, "E" indicates enable input.

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER		TEST CONDITIONS (See Test Load/Waveforms)		310, 'S TYP	340 MAX		341, 'S		UNIT
t _{PLH}	Data to Output delev	H H	beld	ient)	11	15		16	22	ns
t _{PHL}	Data to Output delay	0 - 50 05	$R_I = 90 \Omega$	re vivi	16	22		10	15	ns
tPZL	Output Enable delay	C _L = 50 pF	C[- 30 bi H[- 9011		8	15		10	15	ns
t _{PZH}	Output Enable delay	H H J 2 1	(gailt	(Byzel)	6	12	evn/	1	12	ns
t _{PLZ}	Output Disable delay	C ₁ = 5 pF	R _I = 90 Ω		10	15	2	10	15	ns
t _{PHZ}	Output Disable delay	CL-3PF	UL- 9071		7	12	1	7	12	ns



SN54/74LS310/40/41/44 SN54/74S310/40/41/44

Function Tables

'310

	2	
V _{QC} = 8 V ₁ T _A = 28° C	'340	

ET :	E ₂	1Y OUTPUTS	2Y OUTPUTS
1 8	Н	z at t	Enabled (Inverting)
	L	Z	Z 0.06
	н	Enabled (Inverting)	Enabled (Inverting)
п	L	Enabled (Inverting)	Z 10

E ₁	E ₂	1Y OUTPUTS	2Y OUTPUTS
Н	н	Zeb tugtuO	orateO Z Hug
q H	D L	Z	Enabled (Inverting)
L	н	Enabled (Inverting)	Z HZd ₁
iqë -	O L	Enabled (Inverting)	Enabled (Inverting)

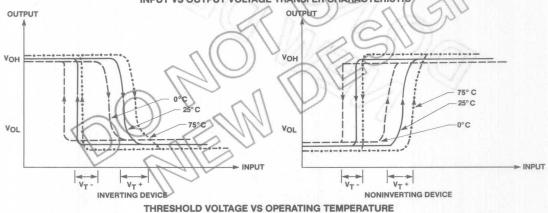
'344

E ₁ E ₂		1Y OUTPUTS	2Y OUTPUTS	
Н	Н	Z	Enabled	
H	L	Z	Z	
L	Н	Enabled	Enabled	
L	L	Enabled	Z	

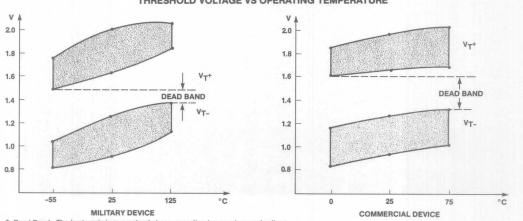
E ₁	E ₂	1Y OUTPUTS	2Y OUTPUTS
Н	Н	Z	// z
Н	L		Enabled
L	Н	Enabled	12
L	J	Enabled	Enabled
THE RESERVE	177		

Z ≡ High impedance (output off).

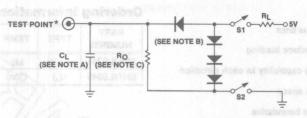
INPUT VS OUTPUT VOLTAGE TRANSFER CHARACTERISTIC





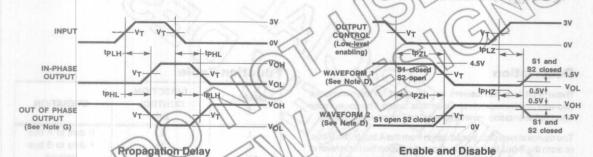


Test Load



* The "TEST POINT" is driven by the output under test, and observed by instrumentation.

Test Waveforms



Xevitosii

NOTES: A CL includes probe and jig capacitance.

B. All diodes are 1N916 or 1N3064.

- C. For Series 54/74S310/340/341/344 R_{O} = 5K, V_{T} = V_{T+} = 1.8 V for low-to-high input transition. For Series 54/74S310/340/341/344 R_{O} = 5K, V_{T} = V_{T-} = 1.1 V for high-to-low input transition. For Series 54/74LS310/340/341/344 R_{O} = 5K, V_{T} = V_{T+} = 1.7 V for low-to-high input transition. For Series 54/74L310/340/341/344 R_{O} = 5K, V_{T} = V_{T-} = 0.9 V for high-to-low input transition.
- D. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- E. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
- F. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_{OUT}=50\Omega$ and: For Series 54/74S, $t_{R}\leq$ 2.5 ns, $t_{F}\leq$ 2.5 ns. For Series 54/74LS and PALs, $t_{R}\leq$ 15 ns. $t_{F}\leq$ 6 ns.
- G. When measuring propagation delay times of 3-state outputs, switches S1 and S2 are closed. (Propagation delays are measured from the inputs crossing V $_{T+}$, V $_{T-}$ to the outputs crossing V $_{T}$)

Features/Benefits

- Three-state outputs drive bus lines
- Low current PNP inputs reduce loading
- . Symmetric -- equal driving capability in each direction
- 20-pin SKINNYDIP® saves space
- · 8-bit data path matches byte boundaries
- Ideal for microprocessor interface
- Pin-compatible with SN54/74LS645 -- improved speed, IIL and IOZL specifications

Ordering Information

PART NUMBER	TYPE	ТЕМР	POLARITY	POWER
SN54LS245	J,L,W	Mil	Non-	100
SN74LS245	N,J	Com	invert	A C

Description

These 8-bit bus transceivers are designed for asynchronous two-way communication between data buses. The control tune tion implementation minimizes external timing requirements

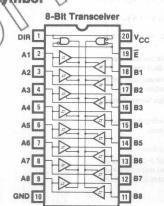
The device allows data transmission from the A bus to the B bus, or from the B bus to the A bus depending upon the logic level at the direction control (DIR) input. The enable input (E) can be used to disable the device, so that the buses are affectively isolated.

of the 8-bit devices are packaged in the popular 20-pin SKINNYDIP.

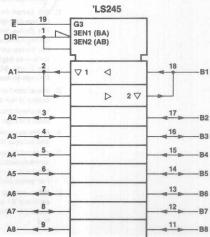
Function Table

ENABLE Ē	DIRECTION CONTROL DIR	OPERATION
7 AL		B data to A bus
/ L	Н	A data to B bus
Н	X	Isolated

ogic Symbol



IEEE Symbol



SKINNYDIP® is a registered trademark of Monolithic Memories

TWX: 910-338-2376

2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2374



12-30

8-Bit Buffer Transceiver SN54/74LS645 SN74LS645-1

FOR MORE DETAIL SEE SECTION 13

Features/Benefits

- Three-state outputs drive bus lines
- Low current PNP inputs reduce loading
- Symmetric equal driving capability in each direction
- 20-pin SKINNYDIP® saves space
- · 8-bit data path matches byte boundaries
- Ideal for microprocessor interface
- SN74LS645-1 rated at I_{OL} = 48 mA

Ordering Information

PART NUMBER	TYPE	TEMP	POLARITY	POWER
SN54LS645	J,L,W	Mil	Non	Un
SN74LS645	N,J	Com	Non-	TEC
SN74LS645-1	Tal	Com	The state of the s	1

Description

These 8-bit bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation minimizes external training requirements.

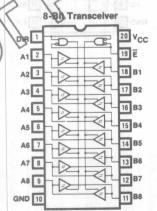
The device allows data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction control (RIR) input. The enable input (E) can be used to disable the viewer so that the buses are effectively isolated.

Function Table

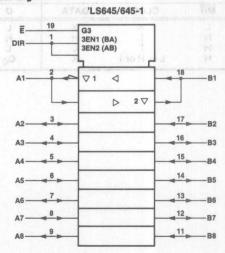
ENABLE	DIRECTION CONTROL DIR	OPERATION
418	L	B data to A bus
L	Н	A data to B bus
Н	X	Ísolated

All of the a bit devices are packaged in the popular 20-pin

Logic Symbok



IEEE Symbol



8-Bit Registers with Master Reset or Clock Enable

SN54LS273

Features/Benefits

- · 8-bit data path matches byte boundaries
- Ideal for microprogram instruction registers
- Ideal for microprogram interface
- Suitable for pipeline data registers
- Useful in timing, sequencing, and control circuits
- Three '273s may replace four '174s

Ordering Information

PART NUMBER	PKG	TEMP	POLAR- ITY	CONTROL OPTION	POWER
SN54LS273	J,L,W	Mil	Non- Invert	Master Reset	LS

Logic Symbols

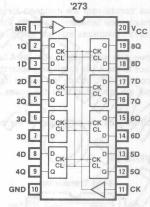
Description

These 8-bit registers contain eight D-type flip-flops, they feature very low I_{CC} (17 mA typical) on the low-power Schottky devices and very-high-speed operation on the Schottky devices. The '273 register is loaded on the rising edge of the clock (CK) and asynchronously cleared whenever the master reset line, MR, is low.

Function Table

	INPUTS	100	OUTPUT
MR	CLOCK	DATA	Q
L	X	X	L R L
Н	1 198	H F	H
Н	1 1020	SHORE L	70.00
Н	L or H or ↓	X	Q ₀

8-Bit Register with Master Reset



Operating Conditions

Absolute Maximum Ratings

SYMBOL	PARAMETER	TEST CONDITIONS (See Interface, Test Load/Waveforms)	FIGURE	MILITARY MIN TYP MAX	UNIT
VCC	Supply voltage			4.5 5 5.5	V
TA	Operating free-air tempe	rature		-55 125	°C
t	Width of clock	High-t _{WH}	1	20	ns
tw	Width of Glock	Low-t _{WL}		20	
twmr	Width of Master Reset	Low-t _{WMRL}	2	20	ns
trec		MR to CK	2	25 †	ns
- 3 14		Data input to CK	3	20 †	
t _{su}	Setup time	Setup time	4	25 †	
			4	10 1	ns
		Data input	3	51	
th	Hold time		4	51	ns
11				51	

¹¹ The arrow indicates the transition of the clock/enable input used for reference. 1 for the low-to-high transition. 1 for the high-to-low transition.

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	MILITARY TYP	MAX	UNIT
VIL	Low-level input voltage				e lange	0.7	V
VIH	High-level input voltage			2.0			٧
V _{IC}	Input clamp voltage	V _{CC} = MIN	I _I = -18 mA		Li II illinarii	-1.5	V
IIL	Low-level input current	V _{CC} = MAX	V _I = 0.4 V		at:	-0.4	mA
I _{IH}	High-level input current	V _{CC} = MAX	V _I = 2.7 V			20	μΑ
II .	Maximum input current	V _{CC} = MAX	V ₁ = 7 V			0.1	mA
V _{OL}	Low-level output voltage	V _{CC} = MIN V _{IL} = MAX V _{IH} = 2 V	I _{OL} = 4 mA	- MM - KD	0.25	0.4	V
VOH	High-level output voltage	V _{CC} = MIN V _{IL} = MAX V _{IH} = 2 V	I _{OH} = -400μA	2.5	3.4		V
los	Output short-circuit current*	V _{CC} = MAX		-20		-100	mA
lcc	Supply current†	V _{CC} = MAX Outputs open	'LS273	- Gi	17	27	mA

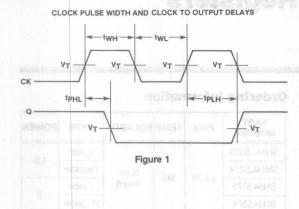
^{*} Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

SYMB	OL	PARAMETER		TEST CONDITIONS (See Test Load/Waveforms)	MIN	'LS273 TYP	MAX	UNIT		
fMA	MAX Maximum Clock frequency			30	40		MHz			
t _{PLF}	1	Olaska Ostara dalar						a Conditions	27	ns
tPHL	tpHL Clock to Output delay tpHL Master Reset to output delay		delay	C _L = 15 pF R _L = 2 KΩ	rain I	HETEMARKY		ns		
^t PHI			output delay	in Interface, Test FFGURE east/Weverboune)				ns		
V	5.5	3	4.5	Supply voltage			Voc			
				Operating free-sir temperature						

[†] ICC is measured after first a momentary ground, and then 4.5 V is applied to clock, while the following other input conditions are held: For the 'LS273—4.5 V on all data and master-reset inputs.





MASTER RESET PULSE WIDTH, MASTER RESET TO OUTPUT DELAY AND MASTER RESET TO CLOCK RECOVERY TIME FOR 'S273

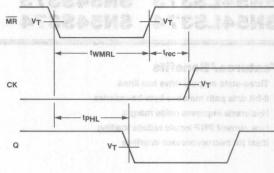
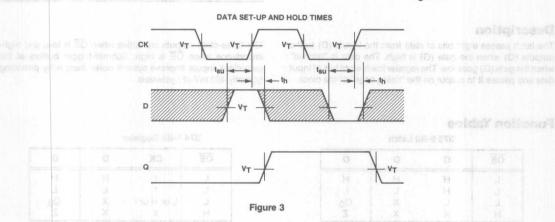
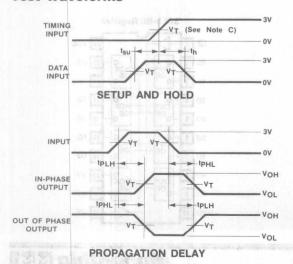


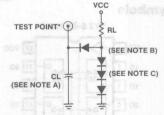
Figure 2



Test Waveforms



Test Load



* The "TEST POINT" is driven by the output under test, and observed by instrumentation.

LOAD CIRCUIT FOR
BI-STATE
TOTEM-POLE OUTPUTS

- Notes: A. C_L includes probe and jig capacitance.
 - B. All diodes are 1N916 or 1N3064.
 - C. For Series 54LS, V_T = 1.3 V.
 - D. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
 - E. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz. $Z_{\mbox{OUT}}$ = 50 Ω_{\odot}

8- Bit Latches, 8-Bit Registers

SN54LS373 SN54S373 **SN54LS374** SN54S374

Features/Benefits

- · Three-state outputs drive bus lines
- · 8-bit data path matches byte boundaries
- Hysteresis improves noise margin
- Low current PNP inputs reduce loading
- Ideal for microprocessor interface

Ordering Information

PART NUMBER	PKG	TEMP	POLARITY	TYPE	POWER
SN54LS373	3	La 129	Latch	1.0	
SN54LS374	11.147		Non- invert	Register	LS
SN54S373 SN54S374	J,L,W	Mil		Latch	
				Register	S

Description

The latch passes eight bits of data from the inputs (D) to the outputs (Q) when the gate (G) is high. The data is "latched" when the gate (G) goes low. The register loads eight bits of input data and passes it to output on the "rising edge" of the clock.

The three-state outputs are active when OE is low, and highimpedance when \overline{OE} is high. Schmitt-trigger buffers at the gate/clock inputs improve system noise margin by providing typically 400 mV of hysteresis.

Function Tables

'373 8-Bit Latch

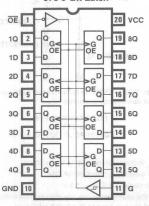
	ŌE	G	D	Q
F	L	Н	нД	Н
	L	Н	L	L
	L	L	X	Q ₀
	Н	X	X	Z

'374 8-Bit Register

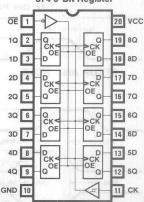
ŌĒ	СК	D	Q
L	1	Н	Н
L	1	L	L
L	L or H or I	X	Q ₀
Н	X	X	Z

Logic Symbols

'373 8-Bit Latch



'374 8-Bit Register



TWX: 910-338-2376



2175 Mission College Boulevard, Santa Clara, CA 95050 Tel: (408) 970-9700 TWX: 910-338-2374 12-36

Absolute Maximum Ratings

Supply voltage V _{CC} -0.5 V to 7 V
Input voltage
Off-state output voltage0.5 V to 5.5 V
Storage temperature -65°C to +150°C

Operating Conditions

SYMBOL	PARAMETER		MIN	MILITARY TYP	MAX	UNIT	
VCC	Supply voltage			4.5	▽ <5 0 —	5.5	V
TA	Operating free-air temperatur	re		-55		125	°C
108-	Width of Clask Cata	High	- 20	15			
W	Width of Clock/Gate Low	Low	200-	15		- X	ns
	Setup time	'LS373		54		9	
^T su	Setup time 'LS374	0.0	201			ns	
t _h	Hold time	'LS373	02-	201		18	-
	Hold time 'LS374			01		57	ns

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST C	ONDITIONS	MIN	MILITARY	MAX	UNIT
VIL	Low-level input voltage					0.7	V
VIH	High-level input voltage			2.0			٧
VIC	Input clamp voltage	VCC = MIN	I _I = -18 mA			-1.5	V
IIL	Low-level input current	VCC = MAX	V _I = 0.4 V			-0.4	mA
IН	High-level input current	VCC = MAX	V _I = 2.7 V			20	μΑ
1	Maximum input current	VCC = MAX	V _I = 7 V			0.1	mA
V _{OL}	Low-level output voltage	V _{CC} = MIN V _{IL} = MAX V _{IH} = 2 V	I _{OL} = 12 mA		0.25	0.4	V
V _{ОН}	High-level output voltage	V _{CC} = MIN V _{IL} = MAX V _{IH} = 2 V	I _{OH} = -1 mA	2.4	3.4		V
lozL	04	VCC = MAX	V _O = 0.4 V			-20	μΑ
lozh	Off-state output current	V _{IL} = MAX V _{IH} = 2 V	V _O = 2.7 V			20	μΑ
los	Output short-circuit current*	VCC = MAX		-30		-130	mA
la a	Supply gurrent	V _{CC} = MAX	'LS373		24	40	mA
Icc	Supply current	Outputs open	'LS374		27	40	IIIA

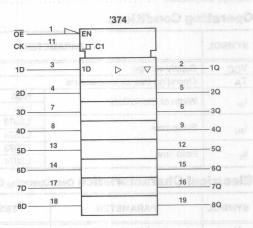
^{*} Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load/Waveforms)	'LS37	'LS373 MIN TYP MAX		'LS374 MIN TYP MAX		
fMAX	Maximum clock frequency				35 50		MHz	
tPLH	Data to output dalay		12	18			ns	
tPHL	Data to output delay		12	18			ns	
tPLH	Clock/Coto to output delevi	$C_L = 45 pF R_L = 667 \Omega$	20	30	15	28	ns	
tPHL	Clock/Gate to output delay		18	30	19	28	ns	
tPZL	Output enable delay		25	36	21	28	ns	
t _{PZH}	Output enable delay		15	28	20	28	ns	
tPLZ	Output disable delay	C - 5 = D - 667 O	15	25	14	25	ns	
tPHZ	Output disable delay	$C_L = 5 pF R_L = 667 \Omega$	12	20	12	20	ns	

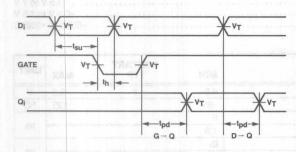
IEEE Symbols

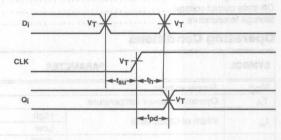
		'373		
OE —	11	ENG1		
1D —	3	1D ▷ ▽	2	—1Q
2D —	4		5	—2Q
3D —	7		6	3Q
4D —	8		9	— 4Q
5D —	13		12	5Q
6D —	14	and the second second	15	6Q
7D —	17		16	— 7Q
8D —	18	BATELISA SATE	19	— 8Q



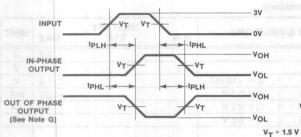
'373 Timing Diagrams

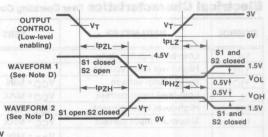
'374 Timing Diagrams





Test Waveforms



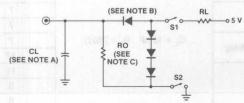


Propagation Delay

Enable and Disable

- Notes: A. C_L includes probe and jig capacitance.
 - B. All diodes are 1N916 or 1N3064.
 - C. For Series 54S, R_O = 1 K, V_T = 1.5 V. For Series 54LS, R_O = 5 K, V_T = 1.3 V.
 - D. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
 Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - E. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
 - F. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz. Z_{OUT} = $50~\Omega$ and: For series 54S, $t_R \leq$ 2.5 ns, $t_F \leq$ 2.5 ns. For Series 54LS and PAL devices, $t_R \leq$ 15 ns, $t_F \leq$ 6 ns.
 - G. When measuring propagation delay times of three-state outputs, switches S1 and S2 are closed.

Standard Test Load



* The "TEST POINT" is driven by the output under test, and observed by instrumentation.

Absolute Maximum Ratings

\$upply voltage V _{CC}	0.5 V to 7 V
Input voltage	1.5 V to 7 V
Off-state output voltage	0.5 V to 5.5 V
Storage temperature	-65°C to +150°C

Operating Conditions

SYMBOL	PA	RAMETER	MIN	MILITARY	MAX	UNIT
VCC	Supply voltage	- An and palent as a little of	4.5	5	5.5	V
TA	Operating free-air temperatur	e 🤲 🛪	-55		125	°C
	Width of Clock/Gate	High	6			
^L W	width of Clock/Gate	Low	7.3	6 4		ns
	Catum times	'S373	01			
lsu	Setup time	'S374	51			ns
	Hold time	'S373	104			
^t h	Hold time	'S374	21		Luine	ns

¹ The arrow indicates the transition of the clock input used for reference. 1 for the low-to-high transition, 1 for the high-to-low transition.

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST C	TEST CONDITIONS MIN TYP				UNIT
VIL	Low-level input voltage	94 p	ROV	-		0.8	V
VIH	High-level input voltage	1 MROFILLAN		2.0	X	TURNS	V
VIC	Input clamp voltage	VCC = MIN	I _I = -18 mA			-1.2	V
HIL WAR	Low-level input current	V _C C = MAX	V _I = 0.5 V			-0.25	mA
IIH -	High-level input current	VCC = MAX	V _I = 2.7 V		TV TV	50	μΑ
Israpis sa	Maximum input current	VCC = MAX	V _I = 5.5 V	71-71-71-71		(0.10	mA
V _{OL}	Low-level output voltage	V _{CC} = MIN V _{IL} = 0.8 V V _{IH} = 2 V	I _{OL} = 20 mA	yeleti na	specios (0.5	V
V _{ОН}	High-level output voltage	V _{CC} = MIN V _{IL} = 0.8 V V _{IH} = 2 V	I _{OH} = -2 mA	2.4	3.4		V
lozL	Off state output oursel	VCC = MAX	V _O = 0.5 V			-50	μΑ
lozh	Off-state output current	V _{IL} = 0.8 V V _{IH} = 2 V	V _O = 2.4 V	4		50	μΑ
los	Output short-circuit current*	V _{CC} = MAX	Office of his are discovery	-40		-100	mA
loo	Supply current	V _{CC} = MAX	'S373	6 .B.	105	160	mA
Icc	Cappiy Carront	Outputs open	'S374		90	140	III

^{*} Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

Switching Characteristics VCC = 5 V, TA = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load/Waveforms)	MIN	'S373 TYP	MAX	MIN	'S374 TYP	MAX	UNIT
fMAX	Maximum clock frequency				5.80	75	100	No. of Street, St.	MHz
tPLH	Data to autnut dalay	un (septomess)		7	12				ns
tPHL	Data to output delay			7	12				ns
tPLH	Clock/Gate to output delay	$C_L = 15 pF R_L = 280 \Omega$		7	14		8	15	ns
tPHL	Clock/Gate to output delay	Y 250	LOWEN S	-12	18		11	17	ns
tPZL	Output enable delay			11	18		11	18	ns
^t PZH	Output enable delay			8	15		8	15	ns
tPLZ	Output disable delay	C - F - F - 200 C		8	12		7	12	ns
tPHZ	Output disable delay	$C_L = 5 pF R_L = 280 \Omega$	and the large	6	9		5	9	ns

8-Bit Register With Clock Enable and Open-Collector Outputs SN54/74S383

Features

- 20-Pin SKINNYDIP® Saves Space
- 8-bit data path matches byte boundaries
- Only available TTL open-collector-output register
- Ideal for certain microprocessor system buses
- Suitable for pipeline data registers
- Excellent for multiple, physically-separated connections to buses in microprocessor-based systems
- Wired-OR or wired-AND logic with outputs

Description

This 8-bit register contains 8 D-type flip-flops and features very fast switching. The 'S383 register is loaded on the rising edge of the clock provided that the clock enable line, CK EN, is low. Like other 8-bit interface devices, the 'S383 is packaged in the popular 20-pin SKINNYDIP.

Ordering Information

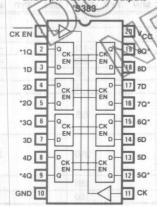
PART NUMBER	PKG	TEMP	POLAR-	CONTROL OPTIONS	POWER
SN54S383	J,L,W	Mil	Non-	Clock	1
SN74S383	N,J	Com	invert	Enable	13

Function Table 'S383

INPUTS		OUTPUT
CK EN CLOCK	DATA	9)
H	1X1	00
11-11-1	4//	H
LORHON	DX)	Qo

Logic Symbol

8-Bit Register with Clock Enable and Open-Collector Outputs



*Indicates Open-Collector Output

IEEE Symbol

		'S383		
CKEN —	11	> 2C1		
1D —	3	1D D Q	2	_1Q
2D —	4	3140 313 7441	5	—2Q
3D —	7	output voltage	6	—3Q
4D —	8		9	_4Q
5D —	13	laemeo segua e	12	—5Q
6D —	14		15	— 6Q
7D-	17	J190	16	_7Q
8D —	18		19	—8Q

Absolute Maximum Ratings

Supply voltage VCC	7.0 V
Input voltage	5.5 V
Off-state output voltage	5.5 V
Storage temperature -65° to +1	150°C

Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS (See Interface, Test Load/Waveforms)	FIGURE	MILITARY MIN TYP MAX	COMMERCIAL MIN TYP MAX	UNIT
VCC	Supply voltage	SW45383 LLW	10000000	4.5 5 5.5	4.75 5 5.25	V
TA	Operating free-air temp	perature		-55 125	0 75	V
. 4	Middle of sleek	High-t _{WH}	sidentaep ba	700 00/	2 ((1111 1))	ns
t _W Width of clock	Width of clock	Low-t _{WL}	1	especiale need 6	A STATE OF THE PARTY OF THE PAR	113
	Marie and the second se	Data input to CK	834	5.1	51	>
t _{su}	Setup time	Low CK EN to CK	2	91	91	ns
		High CK EN to CK	5 MC	91	91	1/11
97		Data input	1 1/2	31	31/	ist swi
th	Hold time	Low CK EN to CK	2	31	3 1 10-0 101	ns
()		High CK EN to CK		DA //	01	elugo

¹¹ The arrow indicates the transition of the clock/enable input used for reference: I for the low-to-bigh transition, 1 for the high-to-low transition.

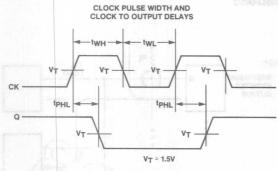
Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS MI		MIN	LITARY TYP MAX	MIN	MMER	CIAL	UNIT
VIL	Low-level input voltage		MA A	77	0.8	many.	7	0.8	V
VIH	High-level input voltage	1100	1	2		2	J KE YO		V
VIC	Input clamp voltage	VCG E MIN	I ₁ = -18mA	Jaketi.	-1.2	0 3 5	lor	-1.2	V
1 _{IL}	Low-level input current	VCC = MAX	V _I = 0.5V		-250	5		-250	μΑ
TH OF	High-level input current	VCC = MAX	V ₁ = 2.7V	OU LES	50		3 (1)	50	μΑ
11	Maximum input current	VCC = MAX	V _I = 5.5V	on III	1	0-11	108	1	mA
VOL	Low-level output voltage	V _{CC} = MIN V _{IL} = MAX V _{IH} = 2V	I _{OL} = 24mA	100 E	0.5	Po-12] DE-] OS-	0.5	V
loн 🌕	High-level output current	V _{CC} = MIN V _{IL} = MAX V _{IH} = 2V	V _{OH} = 5.5 V	os (s)	250		CS.	250	μА
loo	Supply current	V _{CC} = MAX	Outputs HIGH		160	-11		160	m/
ICC -	cappi, carrent	Outputs open	Outputs LOW	- NO 411	160	120	T CHAIN	160	me

Switching Characteristics VCC = 5 V, TA = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load/Waveforms)	MIN	'S383 TYP	MAX	UNIT
fMAX	Maximum Clock frequency		75	110		MHz
t _{PLH}	Clock to output delay	$C_L = 15 pF R_L = 280\Omega$		10	17	ns
t _{PHL}	Clock to output delay	is a water considered in six conflicts	and the Property of the Proper	14	22	ns

Test Waveforms



DATA AND CLOCK ENABLE SETUP AND HOLD TIMES

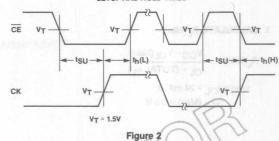
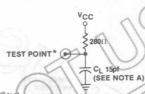


Figure 1

Test Load



* The "TEST POINT" is driven by the output under test. and observed by instrumentation.

LOAD CIRCUIT FOR OPEN-COLLECTOR OUTPUTS

Includes probe and jig capacitance.

Includes probe and jig capacitance.

In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.

All joint pulses are applied by generators having the following characteristics PRR

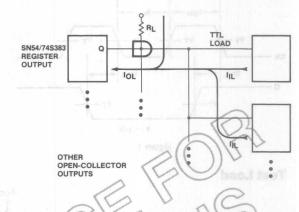
≤ NMHz, Zout = 500 and:

Por Series 54/74S, tp ≤2.5 ns, tr ≤2.5 ns.

Open Collector Bus Application Information For Determination of R_L For Wired-And Applications

1. CALCULATE RL (Min):

$$R_{L}(Min) = \frac{V_{CC} - V_{OL}(Max)}{I_{OL} - (TOTAL I_{IL})}$$



TTL

IIH

2 CALCULATE RL (Max):

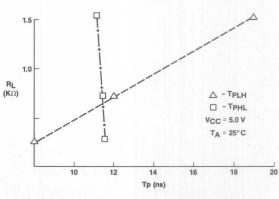
$$R_{L}(Max) = \frac{V_{CC} - V_{OH}(Min)}{(TOTAL I_{OH} + TOTAL I_{IH})}$$

where I_{OH} = 250 μ A at



OTHER OPEN-COLLECTOR **OUTPUTS**

SN54/74S383 REGISTER OUTPUT



RL vs. Tp FOR SN54/74S383

8-Bit Latches, 8-Bit Registers with Inverting Outputs

SN54/74LS533 SN54/74S533 SN54/74LS534 SN54/74S534

Features/Benefits

- Inverting outputs
- Three-state outputs drive bus lines
- 20-pin SKINNYDIP® saves space
- · 8-bit data path matches byte boundaries
- · Hysteresis improves noise margin
- Low current PNP inputs reduce loading
- · Ideal for microprocessor interface
- Pin-compatible with SN54/74LS373/4 or SN54/74S373/4 can be direct replacement when bus polarity must be changed

Description

In addition to the standard S and LS latches and registers, Monolithic Memories provides inverting outputs instead of non-inverting outputs. The inverting outputs are intended for bus applications that require inversion as in interfacing the Am2901A 4-bit slice to an assertive-low bus.

The latch passes eight bits of data from the inputs (D) to the outputs (Q) when the gate (G) is high. The data is "latched"

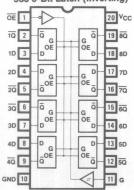
Function Tables

'533	8-Bit	Latch (Inverting)

			-
OE	G	9	Q
L	(H)	H	14
L	14) L	(A)
L	L	X	691
H	X	X	A XI

Logic Symbols

'533 8-Bit Latch (Inverting)



Ordering Information

PART NUMBER	PKG	TEMP	POLARITY	TYPE	POWER
54LS533 74LS533	J,W,L N,J	Mil Com		Latch	
54LS534 74LS534	J,W,L N,J	Mil Com	Invert	Register	3
54S533 74S533	J,W,L N,J	Mil Com	Invert	Latch	S
54S534 74S534	J,W,L N,J	Mil		Register	

when the gate (G) goes low. The register loads eight bits of input data and passes it to the output on the "rising edge" of the clock.

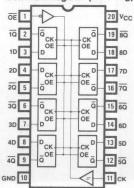
The three-state outputs are active when \overline{OE} is low, and high-impedance when \overline{OE} is high. Schmitt-trigger buffers at the gate/clock inputs improve system noise margin by providing typically 400 mV of hysteresis.

All of the 8-bit devices are packaged in the popular 20-pin SKINNYDIP

'534 8-Bit Register (Inverting)

ŌĒ	СК	D	Q
L	1	Н	Н
L	1	L	L
L	L or H or	X	Q ₀
Н	X	X	Z

'533 8-Bit Register (Inverting)



SKINNYDIP® is a registered trademark of Monolithic Memories.

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Monolithic Memories



12-45

IEEE Symbols



equite Maxing and Patings

Supply voltage V _{CC}	7 V
Input voltage	
Off-state output voltage	5.5 V
Storage temperature	65° to +150°C

Operating Conditions

SYMBOL	LITARY COMMERCIA TYP MAX MAR TYP M	PARAMETER	MIN	TYP	MAX	COI	MMER O		UNIT
V _{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
TA	Operating free-air temperatu	ire	-55		125	0		75	°C
	High	15			15	/		ns	
tw	t _w Width of Clock/Gate	Low	15		SMILLS	15	1	7	115
	1777 Days 1877	LS533	3 ↓			31	111		ns
t _{su}	Setup time	LS534	201		1	201	111	0	กล
th Hold time	1.1.1.2.256 (1975 T.T.)	LS533	888 104		(101	11		ns
	LS534	01	0	17	01	all all		110	

The arrow indicates the transition of the clock/enable input used for reference. I for the low-to-high transition, I for the high-to-low transition.

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CO	ONDITIONS	MILIT	I prome	MIN	MMER	CIAL	UNIT
VIL	Low-level input voltage	65		1	0.7	N	aval-we	0.8	V
VIH	High-level input voltage	8 611	7/1	2	1	2	vel-rigi	H	V
VIC	Input clamp voltage	VOC = MIN	= -18mA	1	-1.5	an dur	sla tuq	-1.5	aV
TIE 1	Low-level input current	Vcd = MAX	V = 0.4V		-0.4	ugai	nual-we	-0.4	mA
AIH D	High-level input current	VCC = MAX	VY = 8.8V	2	20	HELEN	vel-rigi	20	μΑ
A ₁	Maximum input current	Vec = MAX	W = 7V	1-1/	0.1	aden in	atomus	0.1	mA
V _{OL} Low-level outplut voltage	VCC = MIN	101 = 12mA	0.2	5 0.4	larian le	0.25	0.4	V	
OL	Low-level albit voltage	VIH = 2V	I _{OL} = 24mA				0.35	0.5	
Vон	High-level output voltage	VU = MAX	I _{OH} = -1mA	2.4 3.4	1		7		HOV
VOH	riigiriive conput vanage	VIH = 2V	I _{OH} = -2.6mA			2.4	3.1		V
IOZL	0% atota autorita di seria	V _{CC} = MAX V _{IL} = MAX	V _O = 0.4V	9177				-20	μΑ
IOZH	Off-state output current	V _{IH} = 2V	V _O = 2.7V	v. ITY	20			20	μΑ
los	Output short-circuit current *	V _{CC} = MAX	XAV + Do	-30	-130	-30	a Turqiyi	-130	mA
Ave. 108	Supply current	V _{CC} = MAX	LS533	36	6 48	Lange Co.	36	48	mA
1cc	Supply current	Outputs open	LS534	2	7 48		27	48	300

* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

Switching Characteristics VCC = 5 V, TA = 25°C

SYMBOL	PARAMETER	PARAMETER TEST CONDITIONS (See Test Load/Waveforms)		LS533 TYP	MAX	MIN	LS534 TYP	MAX	UNIT
fMAX	Maximum Clock frequency			- Violes	Dent 7	35	50		MHz
tPLH	Data to Output delay			17	25	too in	not estal	1	ns
^t PHL	Data to Output delay			12	25				ns
t _{PLH}	Clask/Cata to autout dalay	$C_L = 45pF R_L = 667\Omega$		20	35	ent Silv	19	30	ns
tPHL	Clock/Gate to output delay			18	35		15	30	ns
t _{PZL}	Output Enable delay			25	36	al can	21	30	ns
^t PZH	Output Enable delay			17	30		20	30	ns
t _{PLZ}	Output Disable delay	$C_1 = 5pF R_1 = 667\Omega$		18	29	sides.	18	29	ns
tPHZ	Cutput Disable delay	OL - 361 HL - 60/11		16	24		16	24	ns

Absolute Maximum Ratings

Supply voltage V _{CC}	7 V
Input voltage 5.5	5 V
Off-state output voltage	5 V
Storage temperature -65° to +150°	°C.

Operating Conditions

SYMBOL	AKU PENNIKOS VITATE. SE STYF HEM DUKE STYF	PARAMETER	MILITARY MIN TYP I	COMMERC MAX MIN TYP	MAX UNIT
VCC	Supply voltage	4.5	4.5 5	5.5 4.75 5	5.25 V
TA	Operating free-air temperate	ure	-55 Williams	125 0	75 °C
, Z	Width of Clock/Gate	High	6	6	ns
'W	Width of Clock/Gate	Low	7.3	7.3) I ns
mar - Line	Setup time	S533	01	01	ns
^T su	Setup time	S534	51	51	U
	Uple time	S533	101	100	ne
th	Hold time	S534	51	51	ns

The arrow indicates the transition of the clock/enable input used for reference. for the low-to-high transition. For the high-to-low transition.

Electrical Characteristics Over Operating Conditions

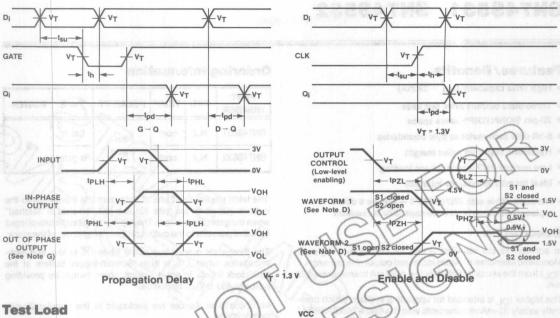
SYMBOL	PARAMETER	TEST CO	NDITIONS	MILITAI MIN TYP	MAX	MIN TYP MAX		UNIT
V _{IL}	Low-level input voltage	/			0.8	77	0.8	V
VIH	High-level input voltage		1	2/~	11	2	HI	V
VIC	Input clamp voltage	VCO = MIN.	I _I = -18mA	16	-1.2	s emalo fue	-1.2	V
AIL III	Low-level input current	VCC = MAX.	V _I = 0.5V	00)	-0.25	ugal faval-wo	-0.25	mA
A _{IH}	High-level input current	VCC MAX	V ₁ = 2.7V	A Comment	50	ich isval-dei	50	μΑ
Apr.	Maximum input current	VCC = MAX,	V = 5.5V		0 (124)	ugni mamore	1	mA
VOL	Low-level output voltage	V _{CC} = MIN, V _{IL} = 0.8V, V _{IH} = 2V	I _{OL} = 20mA		0.5	755	0.5	V
Vон	High-level output voltage	VCC = MIN, VII = 0.8V	I _{OH} = -2mA	2.4 3.4	بقعوده	SZZ,		V
	18 1	WH = 2V	I _{OH} = -6.5mA	WEST		2.4 3.1		
I _{OZL}	Off state suitant surrent	VCC = MAX,	V _O = 0.5V	T 0	-50		-50	μΑ
1 _{OZH}	Off-state output current	V _{IL} = 0.8V, V _{IH} = 2V	V _O = 2.4V	V	50	SQLO SES-0	50	μΑ
los of	Output short-circuit current *	V _{CC} = MAX	XAV = TO	-40	-100	-40	-100	mA
83	Supply current	V _{CC} = MAX,	S533	105	160	105	160	mA
1cc	Supply culterit	Outputs open	S534	90	140	90	140	MA

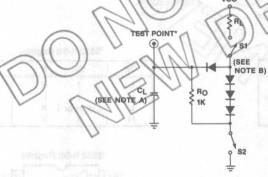
^{*} Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

Switching Characteristics VCC = 5 V, TA = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load/Waveforms)	MIN	S533 MIN TYP MAX		S534 MIN TYP MAX			UNIT
fMAX	Maximum Clock frequency			THE PARTY	AL HONE	75	100	14	MHz
^t PLH	Data to Output delay			9	18		144		ns
^t PHL	Data to Cutput delay			5	16	AND STATE	H7 515		ns
tPLH	Clask/Cata to autout dalay	$C_L = 15pF$ $R_L = 280\Omega$	- ENET	12	22	-	11	20	ns
t _{PHL}	Clock/Gate to output delay			7	20	1 (0) EUR	8	18	ns
t _{PZL}	Output Enable delay			11	20		11	20	ns
t _{PZH}	Output Erlable delay			8	17	S. C.B.C.	8	17	ns
t _{PLZ}	Output Disable delay	$C_1 = 5pF R_1 = 280\Omega$		8	16	- Designation	7	16	ns
^t PHZ	Output Disable delay	$C_L = 5pF$ $R_L = 280\Omega$		6	13	SHU BAY	5	13	ns

Test Waveforms





- * The "TEST POINT" is driven by the output under test, and observed by instrumentation.
- NOTES: A. C_L includes probe and jig capacitance.
 - B. All diodes are 1N916 or 1N3064.
 - C. For Series 54/74S, RO = 1K, VT = 1.5 V. For Series 54/74LS, RO = 5K, VT = 1.3 V.
 - D. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - E. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
 - F. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, Z_{OUT} = 50 Ω and: For Series 54/74S, $t_R \le 2.5$ ns, $t_F \le 2.5$ ns. For Series 54/74LS and PALs, $t_R \le 15$ ns. $t_F \le 6$ ns.
 - G. When measuring propagation delay times of 3-state outputs, switches S1 and S2 are closed.

8-Bit Latch, 8-Bit Register with 32 mA Outputs SN74S531 SN74S532

Features/Benefits

- High drive capability (I_{OL} = 32 mA)
- Three-state outputs drive bus lines
- 20-pin SKINNYDIP® saves space
- · 8-bit data path matches byte boundaries
- Hysteresis improves noise margin
- Low current PNP inputs reduce loading
- Ideal for microprocessor interface
- Pin-compatible with SN74S373/4 can be a direct replacement when high drive capability is required

Description

In addition to the standard S and LS latches and registers, Monolithic Memories provides increased output sink current (IOL) from the standard Schottky IOL of 20 mA to an improved 32 mA.

The higher IOL is intended for upgrading systems which presently satisfy 32-mA requirements with the SN54/74365A/366A/ 367A/368A hex buffers.

Ordering Information

PART NUMBER	PKG	TEMP	POLARITY	TYPE	POWER
SN74S531	N,J	com	Non-	Later	000
SN74S532	N,J	com	invert	Register	1

The latch passes eight bits of data from the inputs (D) to the outputs (Q) when the gate (G) is high. The data is "latched" when the gate (G) goes low. The register loads eight bits of input data and passes it to the output on the rising edge of the clock.

The three-state outputs are active when OE is low, and high-Impedance when OE is high Schmitt-trigger buffers at the gate/clock inputs improve system noise margin by providing typically 400 mV of hysteresis.

All of the 8-bit devices are packaged in the popular 20-pin SKINNYDIR®.

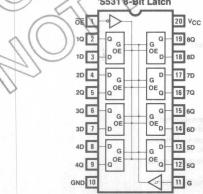
Function Tables

S531 8-Bit Latch

	ŌĒ	G B Q
	M	H H
1	1/1/	L X Q0

Logic Symbols

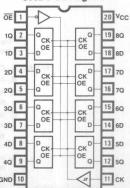
'S531 8-Bit Latch



'S532 8-Bit Register

-			-	
1	OE	CK	D	Q
F	L	15 1	H	H
	L	A A	L	L
	L	Lor Hor 1	X	Q ₀
1	H	X	X	Z

'S532 8-Bit Register



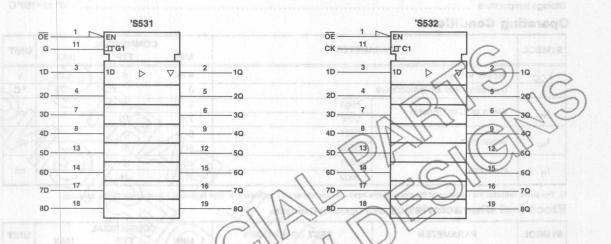
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IEEE Symbols



Absolute Maximum Ratings

Supply voltage V _{CC}	7 V
Input voltage	
Off-state output voltage	5.5 V
Storage temperature	-65° to +150°C

Operating Conditions

SYMBOL	C 100	PARAMETER	MIN	COMMERCIA! TYP	MAX	UNIT
VCC	Supply voltage	- 0)	4.75	5	(525	V
TA	Operating free air tempera	ture	0	//	75)	°C
h Width of Clock/Engblo	High	6	6		1	
^t W	Width of Clock/Enable	Low	7.3	73	7	ns.
3- 00		S531	01	101	- (17/
^t su	Setup time	S532	51	51	12	ns
t _h	Held time	S531	101	101	(6)	1
	Hold time	S532	21	24	1	ns

The arrow indicates the transition of the clock/enable input used for reference. I for the low-to-high transition, I for the high-to-low transition.

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CO	NOITIONS	MIN	COMMERCIAL TYP	MAX	UNIT
VIL	Low-level input voltage	(()	10 0	11		0.8	V
VIH	High-level input voltage	211	111	2			V
VIC	Input clamp voltage	YCG = MIN.	Am814 = 1	1100		-1.2	V
IIL	Low-level input current	VCO MAX,	V = 0.5V	Way of	173	-0.25	mA
¹ IH	High-level input current	VCC = MAX	N = 2.7V		111	50	μΑ
l ₁	Maximum input current	VCC = MAX	= 5.5V		ANDAM	1	mA
VOL	Low-level output voltage	VIH = 5A VIC = WIA'	I _{OL} = 32mA	19),		0.5	V
×of(High-level output voltage	V _{IL} = 0.8V, V _{IH} = 2V	I _{OH} = -6.5mA	2.4	3.1	1	V
!03L)		V _{CC} = MAX, V _{II} = 0.8V,	V _O = 0.5V		4	-50	μΑ
Tozh	Off state output current	$V_{IL} = 0.8V,$ $V_{IH} = 2V$	V _O = 2.4V		1	50	μΑ
los	Output short-circuit current *	V _{CC} = MAX,		-40		-100	mA
011	Supply current	V _{CC} = MAX,	S531		105	160	111
66//	Supply current	Outputs open	S532		90	140	mA

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

SYMBOL	OL PARAMETER TEST CONDITIONS (See Test Load/Waveforms)		MIN	S531 TYP	MAX	MIN	S532 TYP	MAX	UNIT
fMAX	Maximum Clock frequency					75	100		MHz
t _{PLH}	Data to Output delay			7	12				ns
t _{PHL}		C _L = 15pF R _L = 280Ω		7	12				ns
t _{PLH}	01 1 10 11 1 1 1 1 1 1 1 1 1 1 1 1 1 1			7	14		8	15	ns
t _{PHL}	Clock/Gate to output delay			12	18		11	17	ns
t _{PZL}	Outside Frankla dalay			11	18		11	18	ns
^t PZH	Output Enable delay			8	15		8	15	ns
t _{PLZ}	Output Disable delay	C - 5-5 B - 0000		8	12		7	12	ns
[†] PHZ	Output Disable delay	$C_L = 5pF$ $R_L = 280\Omega$		6	9		5	9	ns

'S532 Timing Diagrams **'S531 Timing Diagrams** CLK GATE th Qi G - 0 D-Q **Test Load** TEST POINT* (SEE NOTE B) "bentate" of each end introduct (60) showers CL (SEE NOTE A) (SEE NOTE O The "TEST POINT" is driven by the output under test, and observed by instrumentation. **Test Waveforms** OUTPUT CONTROL OV (Low-level tPLZenabling) ← tpzL → PRHL S1 and 4.5V VOH S2 closed 1.5V S1 closed WAVEFORM 1 S2 open (See Note D) VOL - VOL 0.5VA tPHZ __ **tPHL** tpi H -tpzH-0.5V ¥ -VOH WAVEFORM 2 S1 open S2 closed \$1 and 1.5V OUT OF PH OUTPUT Note G VOL OV S2 closed V_T = 1.3 V **Enable and Disable Propagation Delay** NOTES: A. CL includes probe and jig capacitance. B. All diodes are 1N916 or 1N3064. C. For Series 54/74S, $R_O = 1K$, $V_T = 1.5 V$.

- D. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- E. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
- F. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_{OUT} = 50\Omega$ and: For Series 54/74S, tp \leq 2.5 ns, tp \leq 2.5 ns. For Series 54/74LS and PALs, tp \leq 15 ns. tp \leq 6 ns.
- G. When measuring propagation delay times of 3-state outputs, switches S1 and S2 are closed.

8-Bit Latch, 8-Bit Register with Inverting, 32 mA Outputs

SN74S535 SN74S536

Features/Benefits

- Inverting outputs
- High-drive capability (IOL = 32 mA)
- Three-state outputs drive bus lines
- 20-pin SKINNYDIP® saves space
- · 8-bit data path matches byte boundaries
- Hysteresis improves noise margin
- Low current PNP inputs reduce loading
- Ideal for microprocessor interface
- Pin-compatible with SN74S533/4 can be a direct replacement when high-drive capability is required

Description

In addition to the standard S and LS latches and registers, Monolithic Memories provides increased output sink current (I_{OL}) from the standard Schottky I_{OL} of 20 mA to an improved 32 mA; also, inverting outputs instead of the standard noninvert-

The higher IOL is intended for upgrading systems which pres-

Ordering Information

PART NUMBER	PKG	TEMP	POLARITY	TYPE	POWER
SN74S535	N,J	Com	Invert	Latch	C
SN74S536	N,J	Com	HIVEIL	Register	3

ently satisfy 32-mA requirements with the SN54/74365/366/ 367/368 hex buffers. The inverting outputs are intended for bus applications that require inversion as in interfacing the Am2901A 4-bit slice to an assertive low.

The latch passes eight bits of data from the inputs (D) to the outputs (Q) when the gate (G) is high. The data is "latched" when the gate (G) goes low. The register loads eight bits of input data and passes it to the output on the rising edge of the clock.

The three state outputs are active when OE is low, and highimpedance when OE is high. Schmitt-trigger buffers at the gate/clock inputs improve system noise margin by providing typically 400 mV of hysteresis.

of the 8-bit devices are packaged in the popular 20-pin SKINNYDIP®.

Function Tables

S535 8-Bit Latch (Inverting)

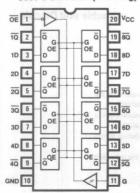
OB	G 2	Ø.
L	H //HV	
L	H /	H
L	L X	Q ₀
H	X X	Z

'S536 8-Bit Register (Inverting)

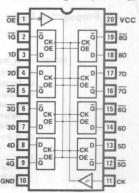
ŌĒ	CK	D	Q
L		Н	L
L		L	H
	LorHort	X	Qo
H	X	X	Z

Logic Symbols

'S535 8-Bit Latch (Inverting)



'S536 8-Bit Register (Inverting)



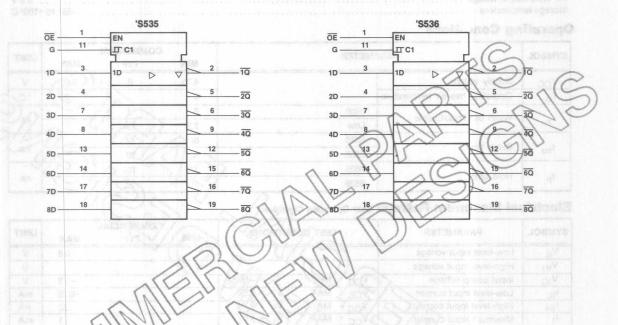
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TWX: 910-338-2376



2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2374 12-54

IEEE Symbols



Absolute Maximum Ratings

Supply voltage V _{CC}	1
Input voltage 5.5 N	
Off-state output voltage	1
Storage temperature -65° to +150°C	0

Operating Conditions

SYMBOL	PARAMETER			MIN	TYP	MAX	UNIT	
Vcc	Supply voltage		401	4.75	5	(5:25	V	
TA	Operating free air temperature		105	0	6	75)	°C/	
tw	Width of Clock/Enable	High	36	6	6	1	20	
		Low	net .	7.3	13	V	ne	
. (7)	S. M. L. M. A. M.	S535	(3)	01	01	1/	111	
t _{su}	Setup time	S536	700	51	51	100	ns	
t _h		S535	08	0)	101	1192	· ·	
	Hold time	S536	Sheri and a	51	(30)	10	ns	

Electrical Maximum Ratings Over Operating Conditions

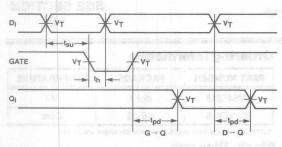
SYMBOL	PARAMETER	TEST CO	NOTIONS	MIN	COMMERCIAL	MAX	UNIT	
VIL	Low-level input voltage	10	10 1			0.8	V	
V _{IH}	High-level input voltage	1100	11	8/			V	
VIC	Input clamp voltage	VCC MIK	1 = 18mA	1720	772 19 19	-1.2	V	
IL	Low-level input current	YCG MAX	V) = 0.5V	300	//11	-0.25	mA	
¹ IH	High-level input current	VCC = MAX	V) = 27V		14173	50	μΑ	
11	Maximum input current	ACC = WAX	Vy 3 5.5V			1	mA	
VOL	Low-level output voltage	V _{CC} = MHA V _{IL} = 0.8V V _H = 2V	I _{OL} = 32mA	!S),		0.5	V	
VOM	Nightlevel output voltage	V _{IL} = 0.8V V _{IH} = 2V	I _{OH} = -6.5mA	2.4	3.1		V	
loze		V _{CC} = MIN V _{II} = 0.8V	V _O = 0.5V		4	-50	μΑ	
TOZH	Off-state output ourrent	V _{IL} = 0.8V V _{IH} = 2V	V _O = 2.4V	7		50	μА	
los /	Output short-circuit current *	VCC		-40		-100	mA	
2/1	Supply current	V _{CC} = MAX	S535		105	160	1/ma	
(gc//	Supply Current	Outputs open	S536		90	140	mA	

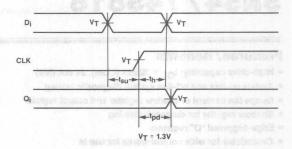
*Not mare than one output should be shorted at a time and duration of the short-circuit should not exceed one second. *Witching Charcteristics V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load/Waveforms)	MIN	S535 TYP	MAX	MIN	S536 TYP	MAX	UNIT
fMAX	Maximum Clock frequency					75	100		MHz
t _{PLH}	Data to Output dolay			9	18				ns
^t PHL	Data to Output delay Clock/Enable to output delay			5	16		III.		ns
^t PLH		$C_L = 15pF R_L = 280\Omega$		12	22		11	20	ns
tPHL				7	20		8	18	ns
^t PZL	Output Enable delay			11	20		11	20	ns
^t PZH	Output Enable delay			8	17		8	17	ns
^t PLZ	Output Disable delay	C - F-F B - 2800		8	16		7	16	ns
^t PHZ	Output Disable delay	$C_L = 5pF$ $R_L = 280\Omega$		6	13		5	13	ns

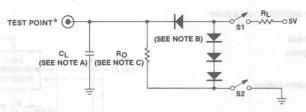
'S535 Timing Diagrams

'S536 Timing Diagrams



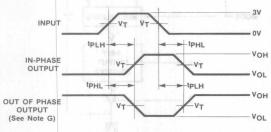


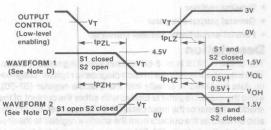
Test Load



* The "TEST POINT" is driven by the output under test, and observed by instrumentation.

Test Waveforms





Propagation Delay

V_T = 1.3 V

Enable and Disable

NOTES: A. C_L includes probe and jig capacitance.

- B. All diodes are 1N916 or 1N3064.
- C. For Series 54/74S, $R_O = 1K$, $V_T = 1.5 V$.
- D. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- E. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
- F. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, Z_{OUT} = 50Ω and: For Series 54/74S, $t_{R}\leq$ 2.5 ns, $t_{F}\leq$ 2.5 ns. For Series 54/74LS and PALs, $t_{R}\leq$ 15 ns. $t_{F}\leq$ 6 ns.
- G. When measuring propagation delay times of 3-state outputs, switches S1 and S2 are closed.

8-Bit Diagnostic Register SN54/74S818

FOR MORE DETAIL SEE SECTION 13

Features/Benefits

- High-drive capability: I_{OL} = 32 mA (Com), 24 mA (Mil)
- Assists on-line and off-line system diagnostic testing
- . Swaps the content of shadow register and output register
- Shadow register for diagnostic testing
- Edge-triggered "D" registers
- Cascadable for wide control words for use in microprogramming
- Features RAM write-back for writable control store initialization
- PNP inputs for low-input current
- 24-pin SKINNYDIP® saves space

Applications

- Register for microprogram control store
- Status register
- Data register
- Instruction register
- Address register
- Interrupt mask register
- Pipeline register
- General purpose register
- Parallel-serial/Serial-parallel converter

Description

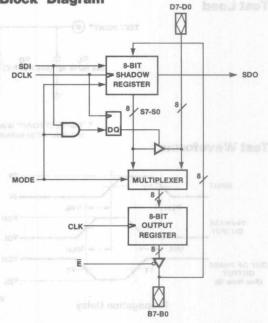
The SN54/74S818 is an 8-bit register with diagnostic features. There is a shadow register in each diagnostic register. Diagnostic data is shifted in serially into the shadow register (S7-S0), while the output register is loaded with either the content of the shadow register or the input data (D7-D0). Moreover, D7-D0 can also be used as the outputs from the shadow register to the data bus, while the outputs (B7-B0) can also be converted to inputs when disabled.

Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
SN54S818	JS,F,L	Mil
SN74S818	NS,JS	Com

NOTE: L package here is L28. The other packages are 24-pin.

Block Diagram



Function Table

INPUTS			OUTPUTS					
MODE	SDI	CLK	DCLK	B7-B0	S7-S0	SDO	OPERATION	
L	X	1	*	Bn← Dn	HOLD	S7	Load output register from input bus	1
L	X	*	t	HOLD	Sn← Sn-1 S0← SDI	S7	Shift shadow register data	2
L	X	†	t en	Bn← Dn	Sn ← Sn-1 S0 ← SDI	S7	Load output register from input bus while shifting shadow register data	1 & 2
Н	X	1	*	Bn ← Sn	HOLD	SDI	Load output register from shadow register	2,3,4
Н	L	*	t	HOLD	Sn ← Bn	SDI	Load shadow register from output bus	3
Н	L	1	1	Bn ← Sn	Sn ← Bn	SDI	Swap shadow register and output register	
Н	Н	*	1	HOLD	HOLD	SDI	Enable D7-D0 as outputs for RAM write-back	4

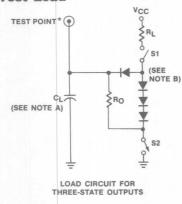
* Clock must be steady or falling.

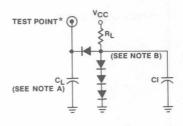
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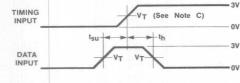
Test Load

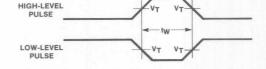




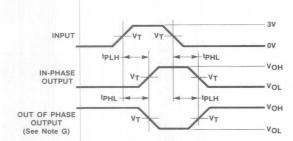
LOAD CIRCUIT FOR BI-STATE TOTEM-POLE OUTPUTS * The "TEST POINT" is driven by the output under test, and observed by instrumentation.

Test Waveforms

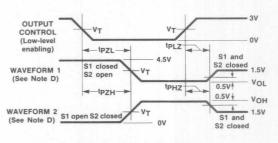




SETUP AND HOLD



PULSE WIDTH



PROPAGATION DELAY

ENABLE AND DISABLE

Notes: A. C_L includes probe and jig capacitance.

- B. All diodes are 1N916 or 1N3064.
- C. For Series 54, R_O = 1K, V_T = 1.5V. For Series 54LS, R_O = 5K, V_T = 1.3V.
- D. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
 - Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- E. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
- F. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz. Z_{OUT} = 50 Ω and: For Series 54, $t_R \leq$ 2.5 ns, $t_F \leq$ 2.5 ns. For Series 54S and PALs, $t_R \leq$ 15 ns, $t_F \leq$ 6 ns.
- G. When measuring propagation delay times of 3-state outputs, switches S1 and S2 are closed.

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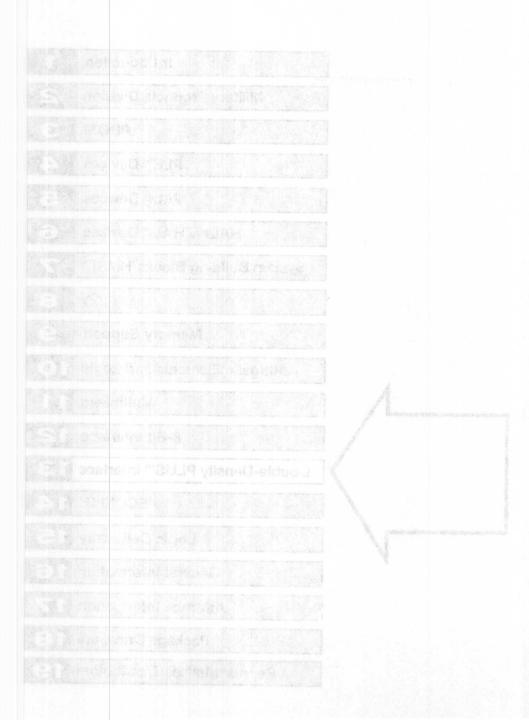


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CNEA/74LOEG	Latch Transceivers					Bit Latch/Register with Re				
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CNEA/741 CGAG	SN54/74LS646 8-Bit Bus Front-Loading-Latch Transceivers		74AC		Advanced CMOS-TTL	781.5887				
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	Transceive	rs		13-46 74AC		Readback—Advanced CN				
					riotel back	Compatible	13-122			
			COMO							
		hevilinal								

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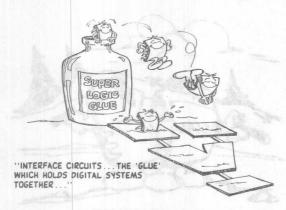
Double-Density PLUS Selection Guide

PART NUMBER	tsJ-grinsoJ P/	ART DESCRIPTION	N - 343	DOWED	DOL ADITY	OUTDUT	M Juli lie	
COMMERCIAL	ARCHITECTURE	FUNCTION	FEATURE	POWER	POLARITY	OUTPUT	OL	
74LS546	Transceiver	Register	nusian	LS	Noninvert	Three-state	32 mA	
74LS566	Transceiver	Register	Independent	LS	Invert	Three-state	32 mA	
74LS547	Transceiver	Latch	enable controls	LS	Noninvert	Three-state	32 mA	
74LS567	Transceiver	Latch	THEFT	LS	Invert	Three-state	32 mA	
74LS646	Transceiver	Front load latch	128/12	LS	Noninvert	Three-state	24 mA	
74LS647	Transceiver	Front load latch	Direction	LS	Noninvert	Open-collector	24 mA	
74LS648	Transceiver	Front load latch	control	LS	Invert	Three-state	24 mA	
74LS649	Transceiver	Front load Latch	TOAK JEST	LS	Invert	Open-collector	24 mA	
74LS651	Transceiver	Front load latch	13-34 PACT	LS	Invert	Three-state	24 m/	
74LS652	Transceiver	Front load latch	Independent enable controls	LS	Noninvert	Three-state	24 m/	
74LS653	Transceiver	Front load latch		LS	Invert	A: Open-collector	24 m/	
74LS654	Transceiver	Fr/load latch		LS	Noninvert	B: Three-state	24 m/	
74ACT547	Transceiver	Latch	Independent	CMOS	Noninvert	Three-state	12 m/	
74ACT567	Transceiver	Latch	enable controls	CMOS	Invert	Three-state	12 m/	
74ACT646	Transceiver	Front load latch	Direction	CMOS	Noninvert	Three-state	12 m/	
74ACT648	Transceiver	Front load latch	control	CMOS	Invert	Three-state	12 m/	
74ACT651	Transceiver	Front load latch	Independent	CMOS	Invert	Three-state	12 m/	
74ACT652	Transceiver	Front load latch	enable controls	CMOS	Noninvert	Three-state	12 m/	
74ACT793	Readback	Latch	Readback	CMOS	Noninvert	Three-state	12 m/	
74ACT794	Readback	Register	enable control	CMOS	Noninvert	Three-state	12 m/	
74LS793	Readback	Latch	Readback	LS	Noninvert	Three-state	24 m/	
74LS794	Readback	Register	enable control	LS	Noninvert	Three-state	24 m/	
74LS548	Two-stage pipeline	Register	Input, Output individual	LS	Noninvert	Three-state	32 m/	
74LS549	Two-stage pipeline	Latch	select controls	LS	Noninvert	Three-state	32 m/	
74S818	Pipeline	Register	Mode controls	S	Noninvert	Three-state	32 m/	

Small But Mighty; New Components **Give You More Logic in Less Chips***

Chuck Hastings and Suneel Rajpal

Interface circuits are generally thought of as unglamorous bread-and-butter items. They have the humble role of being the "glue" which holds digital systems together. Contemporary custom-LSI wizards often claim to be on the point of getting rid of all these bothersome little low-complexity circuits, and yet more interface circuits are sold with each passing year. According to recent estimates, during 1983 the personal computer industry alone consumed one-fourth as many interface circuits as all users consumed during 1982. Figure 1 graphically portrays a realistic scenario for interface for the next few years - everything else will shrink. so interface will grab an increasing share of board area



What this means to you is that, if interface does its part and does some shrinking too, you'll get some major shrinkage in your overall system. Interface is low-complexity stuff to start with, and over the years it has stubbornly resisted being shrunk. Nonetheless, today Monolithic Memories offers a broad line of interface parts which arose from commonly-encountered circumstances, and which — where they fit your design — shrink parts count by a factor of 2:1. Unsurprisingly, they are called "Double-Density PLUS Interface." Actually, under optimal conditions certain of these parts can shrink your parts count by as much as 4:1.

Double-Density PLUS™ Interface can do wonders to compress the physical size of your logic. Consider, for example, a simple sychronous cross-connection between two 8-bit microprocessor buses, capable of transferring information in either direction one byte at time. This crossconnection can be implemented using two 'LS374 8-bit noninverting registers, connected "back-to-back" - that is, each 'LS374 has all of its eight outputs tied respectively to the eight inputs of the other one. Together, these two parts total 40 pins and 2 (0.6*1.1) = 2 (0.66) = 1.32 square inches, allowing for 100 mils end clearance and 300 mils side clearance as is common practice in board layout.



DOUBLE-DENSITY PLUSTM INTERFACE CAN DO WONDERS TO COMPRESS THE PHYSICAL SIZE OF YOUR LOGIC ...

You may notice that, when these two parts are considered as a functional block, far fewer than 40 pins go to the outside world; there are only the 16 data pins corresponding to the two 8-bit buses, two clock pins, two output-enable pins, and power and ground. Now, since Monolithic Memories also noticed back-to-back 'LS374s as an attractive low-pin-count combination a couple of years ago, today you have the option of replacing both of these 'LS374's with a single 24-pin, 300-mil "SKINNYDIP®" 'LS546, which takes up only (0.6*1.3) = 0.78 square inches of your board — slightly more than half as much board area as the two 'LS374s. To summarize:

DESIGN	BOA	RD AREA	WIRE ENDS		
SOLUTION	Sq. In.	Normalized	Pin Count	Normalized	
Two 'LS374s	1.32	1.00	40	1.00	
One 'LS546	0.78	0.59	24	0.60	

Table 1. Board Area and Wire Savings Using 'LS546

*Note: This article is a portion of Monolithic Memories Conference Paper CP-112, which may be found in its entirety in the second edition of the Systems Design Handbook

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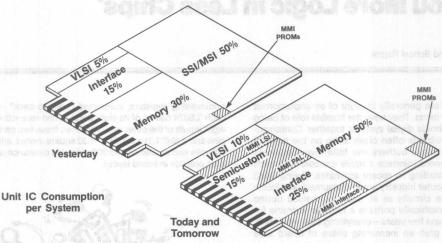


Figure 1. Logic Distribution on a Typical Board

You also pick up some other benefits along the way making this swap. The two registers within the 'LS546 are appreciably faster than the 'LS374s, and also have a higher output drive — 32 mA sinking current instead of 24 mA. The 'LS546 and 'LS566 have clock enables which operate independently for each register. The 'LS546 also has a cleaned-up "structured" pinout with the 8 pins for each data bus together, each bus having its own side of the 24-pin dual-inline package.

The 'LS546 is comprised of two non-inverting edge-triggered registers. If you are dealing with assertive-low buses and need inverting registers, use an 'LS566. If you prefer latches to registers, use either an 'LS547 (non-inverting) or an 'LS567 (inverting). All of these parts have a common "backto-back" internal architecture, as shown in Figure 2.

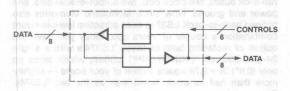


Figure 2. The 546/547/566/567 Block Diagram

Two more families of back-to-back parts also come in the same pinout: the 'LS646/7/8/9 family, and the 'LS651/2/3/4 family. These differ from each other in enable structure; the 'LS646 et. al. have a "direction-control line" so that you can't perform certain operations on both sides of the part simultaneously, whereas the 'LS651 et. al. have generally independent operations on both sides. In each of these families there are two non-inverting parts and two inverting parts; in each case, there is a three-state part and an open-collector part. All of the parts from both families are comprised of "front-loading-latch" individual elements (see



BACK-TO-BACK CONFIGURATION

Figure 3); a front-loading latch is an edge-triggered flipflop in parallel with a buffer, so that the data can be piped through the buffer to reach the output rapidly and then can be *subsequently* recorded in the flipflop. It is also possible, in a front-loading-latch structure, to pipe data temporarily around the flipflop to the output without *ever* recording it in the flipflop. The 'LS646/7/8/9 feature hysteresis on their data inputs as well as on their control inputs, which makes them function well in high-noise environments. The 'LS653/4 are open-collector in one direction, but three-state in the other direction.

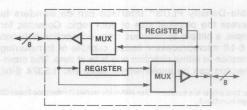


Figure 3. The '646-Series/'651-Series Block Diagram

Then there are two "readback" parts, which consists of a latch or register back-to-back with a buffer: the 'LS793 readback latch, and the 'LS794 readback register. Both of these are just 20-pin, and hence offer a full 2:1 saving in board area as well as in parts count. They have structured pinouts compatible with those of the 'LS573 and 'LS574, but a very different internal architecture; each of the 8 elements (latch or flipflop) has 2 outputs, one of which is totem-pole and goes to the presumed "output pin" of that element, and the other of which is three-state and goes back to the "input pin" for the element (see Figure 4). Thus, it is possible to read the contents of an 'LS793 or 'LS794 from its *input* lines by enabling its three-state outputs.

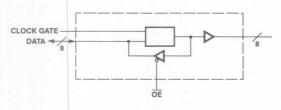


Figure 4. The '793/'794 Block Diagram

The 'LS793 and 'LS794 are intended for use in decentralized systems, for instance industrial-control systems in which a large number of slowly-changing setpoints and displays are under the control of a central microprocessor. The readback feature permits reading one of these, updating it, and replacing it. Without the readback feature, the system would have to keep a redundant copy of the setpoint or display value in main memory, which could cause additional system overhead due to the time-slicing of the microprocessor's activities, or even due to virtual-memory page-faulting in larger systems. Moreover, there is the reliability issue of whether the alleged redundant copy always agrees exactly with the real thing out there in the register controlling the actuator or the display, and what happens whenever it doesn't.

CONFIGURATION	LATCHES	REGISTERS
Back-to-Back L/R	'547('373) '567('533)	'546('374) '566('534)
Back-to-Back Front-Loading Latches	V2 3	'646/7('374) '648/9('534) '652/4('374) '651/3('534)
Readback L/R	'793('373)	'794('374)

Table 2. Double-Density PLUS Interface Product

Note that the bracketed part numbers represent the element *inside* the Double-Density PLUS Interface. For example, a '245 can replace two '244s and a '546 can replace two '374s. The same holds true for the '646 and '651 series. However the '793/'794 are the equivalent of a '373/'374 and a readback buffer such as a '244.

Table 2 is a summary of the Double-Density PLUS Interface product presently available from Monolithic Memories.

Two other common and intuitively-plausible combinations of a couple of 8-bit latches or registers are "nose-to-tail" (one after the other), and "side-by-side" (alternate). If two registers are used in a nose-to-tail combination, for instance, data from the inputs enters the first register when it is clocked, and the outputs of the first register are the inputs of the second register, and thus the same data finally reach the outputs of the combination when the second register is subsequently clocked. And, if two registers are used in a side-by-side combination, their inputs come from the same input bus, and their outputs go to the same output bus, but they can be controlled separately and the output bus can be driven from either one.

Although the nose-to-tail configuration and the side-by-side configuration seem quite different, with the provision of some internal multiplexing the same Double-Density PLUS™ Interface part can satisfy both requirements. Such a part is called a pipeline — register or latch, as the case may be. The internal architecture of a two-level pipeline is shown in Figure 5.

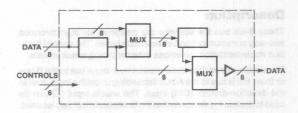


Figure 5. The '548/9 Block Diagram

The 'LS548, with the edge-triggered registers, and the 'LS549, with latches, follow the Figure 5 block diagram exactly. Their pinouts resemble those of 'LS546, 'LS646, and 'LS651 families. Their speeds are similar, and they also feature 32-mA-I_{OL} outputs.

Typical applications for Double-Density PLUS Interface include computer peripherals, minicomputers, and microcomputers. Applications for the open-collector parts are in the telecommunication and games areas. The drive of these parts enables them to drive heavily-loaded buses, and flat cables.

8-Bit Buffer **SN54LS245**

Features/Benefits

- Three-state outputs drive bus lines
- Low current PNP inputs reduce loading
- Symmetric equal driving capability in each direction
- 8-bit data path matches byte boundaries
- Ideal for microprocessor interface
- Pin-compatible with SN54LS645 improved speed, I_{IL} and I_{OZL} specifications

Ordering Information

PART NUMBER	TYPE	TEMP	POLARITY	POWER
SN54LS245	J,L,W	Mil	Noninvert	LS

Description

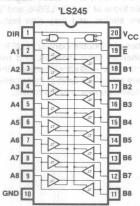
These 8-bit bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation minimizes external timing requirements.

The device allows data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction-control (DIR) input. The enable input (E) can be used to disable the device so that the buses are effectively isolated.

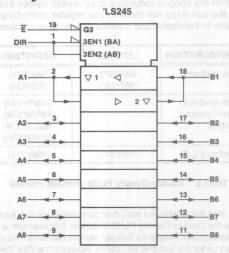
Function Table

ENABLE Ē	DIRECTION CONTROL DIR	OPERATION
ie system woul	n sautasi lastibasi e	B data to A bus
point or displa	pe out to Hado ture	A data to B bus
research property	a esnab r Xno uplum	Isolated

Logic Symbol



IEEE Symbol



TWX: 910-338-2376

2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2374



Absolute Maximum Ratings

Supply voltage VCC0.5 V to	07V
Input voltage	07V
Off-state output voltage	5.5 V
Storage temperature -65°C to +15	50° C

Operating Conditions

SYMBOL	PARAMETER	MIN	MILITARY TYP	MAX	UNIT
VCC	Supply voltage	4.5	5	5.5	٧
TA	Operating free-air temperature	-55		125	°C

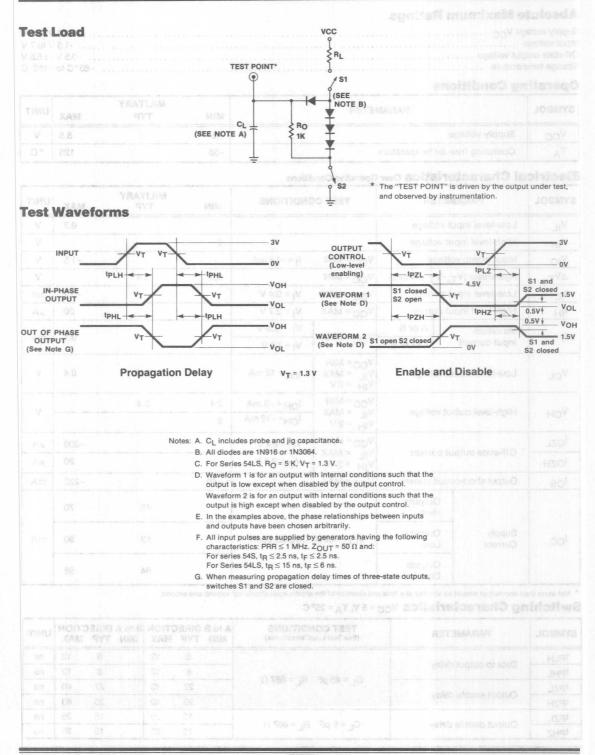
Electrical Characteristics Over Operating Conditions

SYMBOL	PARAME	TER	TEST CONDITIONS		MIN	MILITARY TYP	MAX	UNIT		
VIL	Low-level input	oltage					0.7	V		
VIH	High-level input	voltage	er eter	de de la companya de				V		
VIC	Input clamp volta	age	V _{CC} = MIN	I _I = -18 mA			-1.5	V		
ΔV_{T}	Hysteresis (V _{T+} -	V _{T_}) A or B	V _{CC} = MIN		0.2	0.4		V		
IIL	Low-level input of	current	V _{CC} = MAX	V _I = 0.4 V	W. J.	3-77	-0.2	mA		
1 _{IH}	High-level input	current	V _{CC} = MAX	V _I = 2.7 V	10,300		20	μΑ		
10V - 175	Maximum	A or B		V _I = 5.5 V	-	particular and the	0.1	mA		
VIII SECTO		DIR or E	V _{CC} = MAX	V _I = 7.0 V	17.7			mA		
V _{OL}	Low-level output	voltage	V _{CC} = MIN V _{IL} = MAX V _{IH} = 2 V		Geley	0.25	0.4	V		
4,310			V _{CC} = MIN	V _{CC} = MIN	V _{CC} = MIN	I _{OH} = -3 mA	2.4	3.4		
VOH	High-level output	voltage	V _{IL} = MAX V _{IH} = 2 V	I _{OH} =-12 mA	2			V		
lozL		Fa I. II	V _{CC} = MAX V _{IL} = MAX	V _O = 0.4 V	es A OL Idolo	yeld	-200	μΑ		
lozh	Off-state output	Off-state output current V _{IL} V _{IH}		V _O = 2.7 V	tail not in		20	μΑ		
los	Output short-circ	uit current*	V _{CC} = MAX	me neglectine spilet i in mein miles queses wol	-40		-225	mA		
lcc	Supply	Outputs High	al Ration temperature of Legion with your bests Joseph Technologies and	flw sombyet its net as 8 an Chilgo social wife place arthur shows the place	the valid Magazo Magazo	48	70			
		Outputs Low		. Outputs open	nepel (A. A. doeseno	62	90	mA		
	Outputs Disabled		3/18/2		108161	64	95			

^{*} Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load/Waveforms)	A to B MIN	DIRE	CTION	B to A MIN		CTION	UNIT
tPLH Date to autout dalay			8	12		8	12	ns	
tPHL	Data to output delay	0 - 45 - 5 D - 007 0		8	12		8	12	ns
tPZL	Output analyla dalau	$C_L = 45 \text{ pF} R_L = 667 \Omega$	27	40		27	40	ns	
tPZH	Output enable delay	ut enable delay	25	40		25	40	ns	
tPZL	Output disable delay	C - F - F - C - C - C - C		15	25		15	25	ns
tPHZ	Output disable delay	$C_L = 5 pF R_L = 667 \Omega$		15	25		15	25	ns



8-Bit Buffer Transceivers SN54LS645

Features/Benefits

- . Three-state outputs drive bus lines
- Low current PNP inputs reduce loading
- Symmetric equal driving capability in each direction
- · 8-bit data path matches byte boundaries
- Ideal for microprocessor interface

Ordering Information

PART NUMBER	TYPE	TEMP	POLARITY	POWER
SN54LS645	J,L,W	Mil	Noninvert	LS

Description

These 8-bit bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation minimizes external timing requirements.

The device allows data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction-control (DIR) input. The enable input (E) can be used to disable the device so that the buses are effectively isolated.

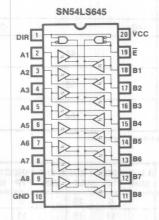
All of the 8-bit devices are packaged in the popular 20-pin SKINNYDIP.

Function Table

ENABLE E	DIRECTION CONTROL DIR	OPERATION
MM Loov	L	B data to A bus
XAME IV	eges/Hragou le	A data to B bus
VS H SV	X	Isolated

IEEE Symbol apartor augus invel-light

Logic Symbol



-NV	19	-	54LS		1	
Ē	1	G3				
DIR-	1	3EN1	(BA)		8-110	
		3EN2	(AB)			HZO
asy	2	19 11.0 11	aprile.	notic :	18	
A1-		- ▽ 1	4	2	1	—B1
	L	ripet	D	2 ▽		
				- v		
A2-	3	em equip			17	—В2
A3-	4				16	—В3
A4-	5	ill qtuO			_15_	—В4
~~		en paetu				54
A5-	6	is ishorte			14	-B5
A6-	7	3 113/11	WA15	0.46	13	—В6
A7-	8	193	THE	SEAS	12	B7
	9				- 11	-STATES OF
A8	< >				-	—B8

TWX: 910-338-2376

2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2374



Absolute Maximum Ratings

Supply voltage V _{CC}	0.5 V to 7 V
Input voltage	1.5 V to 7 V
Off-state output voltage	0.5 V to 5.5 V
Storage temperature	65°C to +150°C

Operating Conditions

SYMBOL	PARAMETER		MILITARY	\ast	UNIT
STMBUL	FARAMETER	MIN	MAX	ONT	
Vcc	Supply voltage	4.5	5	5.5	V
TA	Operating free-air temperature	-55		125	°C

Electrical Characteristics Over Operating Conditions

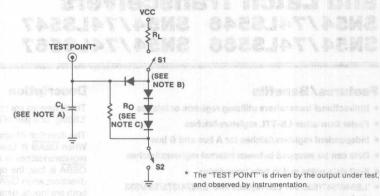
SYMBOL	PARAMET	ER	TEST C	ONDITIONS	MIN	MILITARY TYP	MAX	UNIT
VIL	Low-level input vo	oltage					0.7	V
VIH	High-level input v	oltage			2			V
VIC	Input clamp voltag	ge	V _{CC} = MIN	I _I = -18 mA			-1.5	V
ΔVT	Hysteresis (V _{T+} -V	/ _{T_}) A or B	V _{CC} = MIN		0.2	0.4		V
IIL	Low-level input cu	urrent	V _{CC} = MAX	V _I = 0.4 V			-0.2	mA
¹IH	High-level input c	urrent	V _{CC} = MAX	V _I = 2.7 V	Later 1		20	μΑ
MONTAR	Maximum	A or B	alexas.	V _I = 5.5 V	edit aseud a	der i etweeter	esim man	
I CHYPAR	input current	DIR or E	V _{CC} = MAX	V _I = 7.0 V	as painty is		0.1	mA
V _{OL}	Low-level output v	oltage	V _{CC} = MIN V _{IL} = MAX V _{IH} = 2 V	I _{OL} = 12 mA	d Bartina an noquiça qal alanna s	0.25	0.4	V
			V _{CC} = MIN	I _{OH} = -3 mA	2.4	3.4	lenn Mal A ar	100.112
Vон	High-level output v	oltage	V _{IL} = MAX V _{IH} = 2 V	I _{OH} =-12 mA	2		Aid	V
lozL	10 10 10 10 10 10 10 10 10 10 10 10 10 1	10 BL	V _{CC} = MAX	V _O = 0.4 V			-200	μΑ
lozh	Off-state output c	urrent	V _{IL} = MAX V _{IH} = 2 V	V _O = 2.7 V		e Sauvenie	20	μΑ
los	Output short-circui	t current*	V _{CC} = MAX		-40	· · · · · · · · · · · · · · · · · · ·	-225	mA
		Outputs High				48	70	
lcc		Outputs Low		. Outputs open	mail I	62	90	mA
58	476	Outputs Disabled				64	95	

^{*} Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

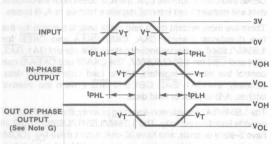
Switching Characteristics V_{CC} = 5 V, T_A = 25°C

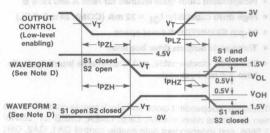
SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load/Waveforms)	A to B DIRE	CTION	B to A DIRE	CTION	UNIT
tPLH	tPLH Date to subsuit dalay		8	15	8	15	ns
tPHL	Data to output delay	C - 45 - F D - 667 O	11	15	11	15	ns
tPZL	Output enable delay	$C_L = 45 \text{ pF} R_L = 667 \Omega$	31	40	31	40	ns
tPZH	Output enable delay		26	40	26	40	ns
tPLZ	Output disable delay	disable delay	15	25	15	25	ns
tPHZ Output disable delay		$C_L = 5 pF R_L = 667 \Omega$	15	25	15	25	ns

Test Load



Test Waveforms





Propagation Delay

VT = 1.3 \

Enable and Disable

Notes: A. C_I includes probe and jig capacitance.

- B. All diodes are 1N916 or 1N3064.
- C. For Series 54LS, RO = 5 K, VT = 1.3 V.
- D. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
- F. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz. Z_{OUT} = 50 Ω and: For series 54S, $t_{\rm R} \leq$ 2.5 ns, $t_{\rm F} \leq$ 2.5 ns. For Series 54LS, $t_{\rm R} \leq$ 15 ns, $t_{\rm F} \leq$ 5 ns.
- G. When measuring propagation delay times of three-state outputs, switches S1 and S2 are closed.

8-Bit Bus Register Transceivers and Latch Transceivers SN54/74LS546 SN54/74LS547 SN54/74LS566 SN54/74LS567

Features/Benefits

- Bidirectional transceivers utilizing registers or latches
- Faster than other LS-TTL registers/latches
- Independent registers/latches for A bus and B bus
- Data can be swapped between internal registers/latches
- · 8-bit data paths match byte boundaries
- 'LS546/547/566/567 can replace two 'LS374/373/534/533 devices
- Independent clock/gate enables for rank A and rank B
- High drive capability: IOL = 32 mA (COM), 24 mA (MIL)
- 24-pin SKINNYDIP® saves space
- Three-state outputs drive bus lines
- The clock, clock-enable, and latch-enable inputs typically have 300 mV hysteresis

There are independent clock and clock enable controls for the two directions namely CKA, CKB, CKEĀ, CKEĀ for 'LS546/ 'LS566, and independent gate enable control GA1, GA2, GB1 and GB2 for 'LS547/'LS567. The CKA/B and CKEA/B can control the internal registers A/B to load data or hold data. Similarly, the GA1, GA2, GB1 and GB2 can govern the internal latches, A/B to pass or hold data.

Description

These devices are comprised of a pair of 8-bit registers ('LS546, 'LS566), or a pair of 8-bit latches ('LS547, 'LS567).

The direction of operation is controlled by OEAB and OEBA. When OEAB is Low and OEBA is High, the operation of the registers/latches is A-to-B direction; when OEAB is High and OEBA is low, the operation of the registers/latches is B-to-A direction; when OEAB and OEBA both are High, the A, B buses both are inputs, data will be stored into registers/latches; when OEAB and OEBA both are Low, the A, B buses both are outputs, data will transfer from internal registers/latches to A, B buses.

There are independent clock and clock enable controls for the two directions: namely CKA, CKB, $\overline{\text{CKEA}}$ and $\overline{\text{CKEB}}$ for 'LS546/'LS566, and independent gate enable control GA1, $\overline{\text{GA2}}$, GB1 and $\overline{\text{GB2}}$ for 'LS547/'LS567. The CKA/B and $\overline{\text{CKEA/B}}$ can control the internal registers A/B to load data or hold data. Similarly, the GA1, $\overline{\text{GA2}}$, GB1 and $\overline{\text{GB2}}$ govern the internal latches, A/B to pass or hold data.

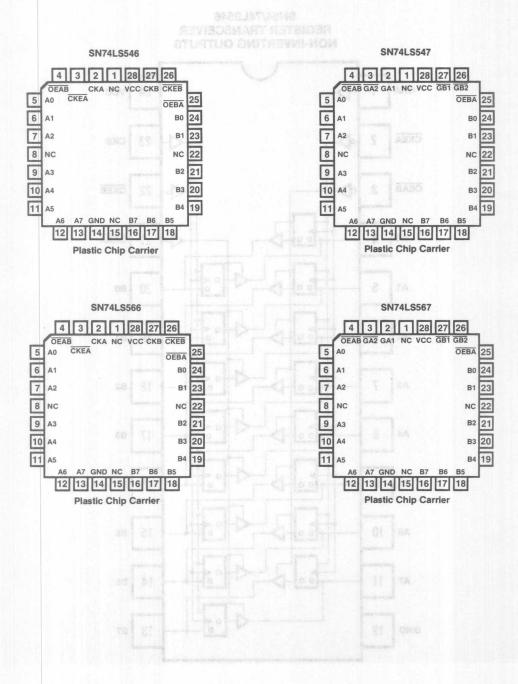
The 'LS546/'547 provide non-inverting polarity; the 'LS566/'LS567 provide inverting polarity. The 'LS546/'LS547/'LS566/'LS567 all have 3-state outputs, and have 32-mA output drive $I_{\mbox{\scriptsize OL}}$ (COM) over the commercial temperature range and 24-mA output drive $I_{\mbox{\scriptsize OL}}$ (MIL), over the military temperature range.

All of the devices are packaged in the popular 24-pin SKIN-NYDIP package.

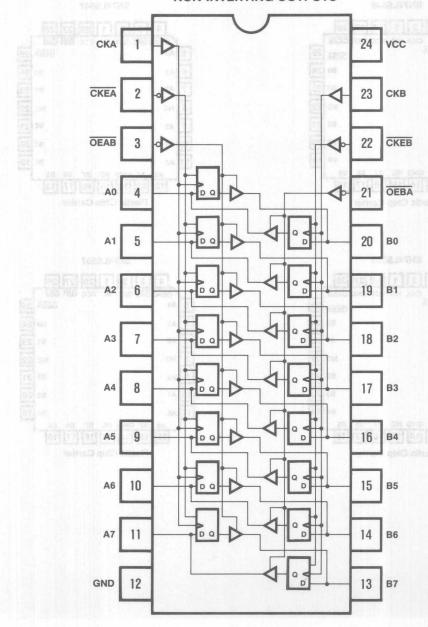
Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE	POLARITY	TYPE	POWER
SN54LS546	JS, W, L (28)	MII	(I to the painting that there are	Desistes	
SN74LS546	NS, JS, NL (28)	Com	Non-invert -	Register	
SN54LS547	JS, W, L (28)			Latab	
SN74LS547	NS, JS, NL (28)	Com		Latch	LS
SN54LS566	JS, W, L (28)	Mil	nio 4 i A S2 biss 78 yartonive	Di-t	LS
SN74LS566	NS, JS, NL (28)	Com	In	Register	
SN54LS567	JS, W, L (28)	Mil	Invert	Latab	
SN74LS567	NS, JS, NL (28)	Com		Latch	

Pin Configurations

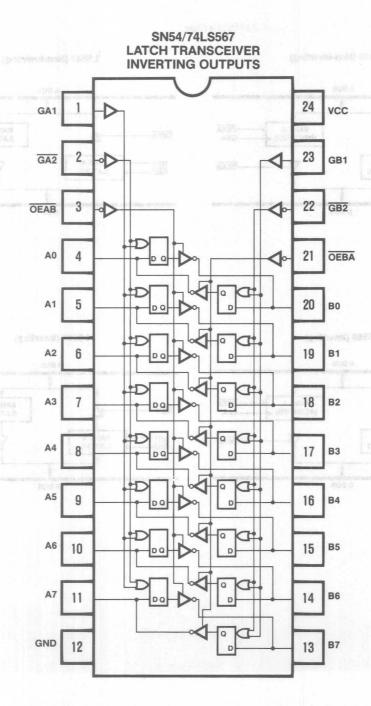


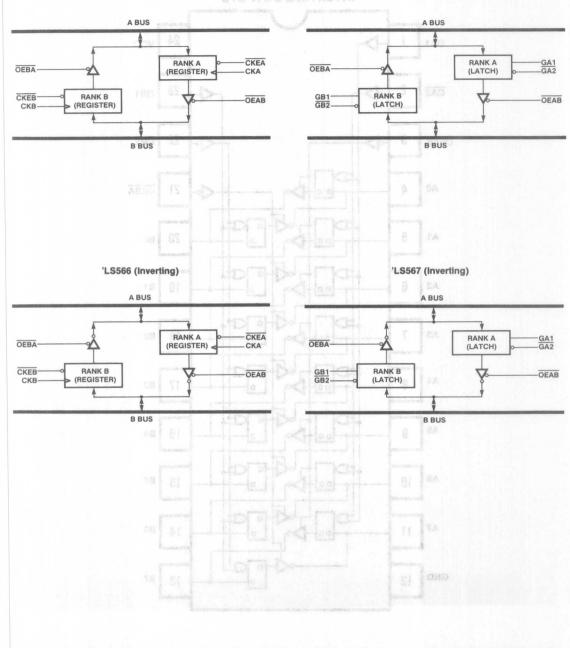
SN54/74LS546 REGISTER TRANSCEIVER NON-INVERTING OUTPUTS



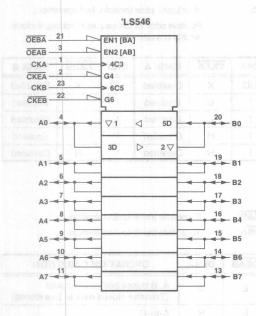
SN54/74LS547 LATCH TRANSCEIVER **NON-INVERTING OUTPUTS** 24 VCC GA1 2 GA2 GB1 3 22 OEAB GB2 21 OEBA A0 4 DQ 20 5 BO A1 6 19 A2 **B1** 7 18 A3 **B2** 8 17 **B3** A4 16 9 A5 **B4** 15 10 A6 **B5** 11 14 A7 B6 13 12 GND B7

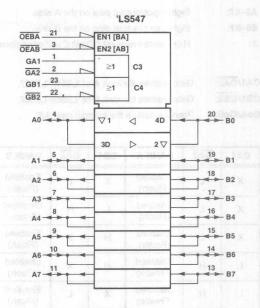
SN54/74LS566 REGISTER TRANSCEIVER **INVERTING OUTPUTS** 24 VCC CKA CKEA 2 23 CKB 3 OEAB 22 CKEB 21 **OEBA** A0 4 DQ 20 5 BO A1 19 6 B1 A2 18 B2 A3 17 8 **B3** 16 **B4** A5 10 15 B5 A6 A7 11 14 B6 12 13 GND B7

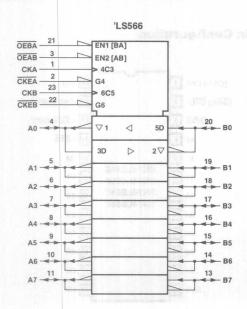


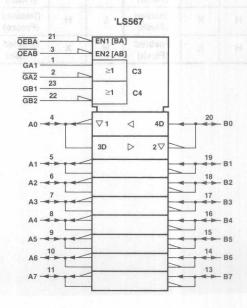


IEEE Symbols









SN54/74LS546 SN54/74LS547 SN54/74LS566 SN54/74LS567

Function Table Nomenclature Description

A0-A7: Eight input/output pins on the A side.

B0-B7: Eight input/output pins on the B side.

X: Hor L state irrelevant ("Don't Care" conditions).

GA1/GA2: Gate enables for rank A of 'LS547/'LS567.
GB1/GB2: Gate enables for rank B of 'LS547/'LS567.
QoA/QoB: Previous data of the internal rank A/B.

GA1	GA2	RANK A	GB1	GB2	RANK B
X	L	Enabled (Flush)	X	× Ly «	Enabled (Flush)
X	e L	Enabled (Flush)	L	Н	Disabled (Freeze)
X	ET L	Enabled (Flush)	Н	X	Enabled (Flush)
L	Н	Disabled (Freeze)	Н	Х	Enabled (Flush)
L	Н	Disabled (Freeze)	X	L	Enabled (Flush)
L	Н	Disabled (Freeze)	L	Н	Disabled (Freeze)
Н	Х	Enabled (Flush)	Х	L	Enabled (Flush)
Н	Х	Enabled (Flush)	, L	Н	Disabled (Freeze)
Н	X	Enabled (Flush)	H	X	Enabled (Flush)

CKEA/CKEB: Clock enable for rank A/B of 'LS546/'LS566.

CKA/CKB: Clock for rank A/B of 'LS546/'LS566.

UC: H or L or I case (nonclocked operation).

1: Positive edge of CK causes clocking, if clock

enable is asserted.

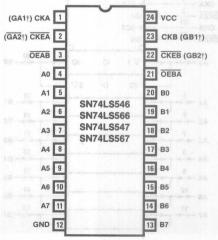
CKA	CKEA	RANK A	СКВ	CKEB	RANK B
UC	X	Disabled	UC	X	Disabled
1	L	Enabled	1 700	L	Enabled
1 00	45L	Enabled	1	Н.	Disabled
1	Н	Disabled	1	L	Enabled
†	Н	Disabled	1	Н	Disabled

OEAB: To enable the A-to-B operation.

OEBA: To enable the B-to-A operation.

OEAB	OEBA	OPERATION DIRECTION
L	L	A, B buses both are outputs (Transfer stored data to bus stored)
L	Н	A-to-B
Н	L	B-to-A
Н	Н	A, B buses both are inputs (storage)

Pin Configuration



†For SN74LS547, SN74LS567

Bus Operation For 'LS546

DIRECTION CLOCK CLOCK DATA I/O CONTROL ENABLE (A) ENABLE (B) BANK A **OPERATION** RANK B **BLOCK DIAGRAM** CKB CKEB OEAB OEBA A0-A7 B0-B7 CKA CKEA UC X QoA UC X QoB UC X QoA 1 L B bus 1 QoB UC X QoA H BUS UC X QoB 1 L A bus RANK В 1 B bus Storage Н Hos Input Input 1 L A bus L RANK † 1 L A bus H QoB BUS 1 H QoA UC X QoB 1 1 H QoA L B bus 1 1 H QoA H QoB UC X QoA UC X QoB UC X 1 B bus QoA L UC X QoA 1 H QoB BUS RANK 1 L Rank B UC X QoB В Output B-to-A 1 Н L of Input 1 L Rank B L B bus RANK Operation Rank B 1 L Rank B 1 H QoB 1 H QoA UC X QoB † 1 H QoA L B bus 1 Н QoA 1 H QoB UC X QoA UC X QoB 1 UC X QoA L Rank A UC † X H QoB QoA RANK B 1 L A bus UC X QoB Output A-to-B Input of 1 L A bus † L Rank A Operation Rank A Α 1 † QoB L A bus H 1 H QoA UC X QoB 1 H QoA † Rank A L 1 Н QoA 1 H QoB UC X UC X QoA QoB UC X 1 Rank A QoA L † QoB UC X QoA H RANK 1 UC X QoB L Rank B Output Output В Transfer Stored L Lan of of 1 L Rank B 1 L Rank A RANK Data Rank B Rank A 1 L Rank B 1 H QoB BUS 1 H QoA UC X QoB 1 1 Н QoA

1

Н

QoA

Rank A

QoB

L

H

Bus Operation For 'LS547

OPERATION	2000	CTION TROL	DATA	A I/O	BLOCK DIAGRAM		LE (A)	RANK A	and the second second	ATE SLE (B)	RANK B
OFERATION	OEAB	OEBA	A0-A7	B0-B7	BEOCK BIAGRAM	GA1	GA2	ABS	GB1	GB2	TIAIN L
MO X	QU	1 3	D X	34		L	Н	QoA	L	Н	QoB
		1 10	C X	l bu		L	Н	QoA	Н	X	B bus
	1		X	- au	A	L	Н	QoA	Х	L	B bus
	aU.	80.0	6 5		BUS RANK B	Н	X	A bus	L	Н	QoB
Storage	Н	H	Input	Input	RANK	Нап	X	A bus	Н	X	B bus
		Find			A B	Н	X	A bus	X	L	B bus
	du	Ao			BUS	X	L	A bus	L	Н	QoB
		4.3	0 1	1		X	L	A bus	Н	X	B bus
		A.	у н	1		X	L	A bus	X	L	B bus
Taga X	OU		T. K.	DU I		L	Н	QoA	L	Н	QoB
		1 43	X	Of		L	Н	QoA	Н	X	B bus
		AL	o x	, ou	A	L	Н	QoA	Х	L	B bus
	au-	9.81	Output		BUS RANK	Н	Х	Rank B	L	Н	QoB
B-to-A Operation	Н	Lon	of	Input	В	Н	Х	Rank B	Н	Х	B bus
DOC 1		B Mar	Rank B		RANK	Н	X	Rank B	X	L	B bus
	30	JA.	D H		B	X	L	Rank B	L	Н	QoB
		1 40	L H			X	L	Rank B	Н	X	B bus
	f	1	H	7		X	L	Rank B	X	L	B bus
- 860 1 X	DU		X	gun		L	Н	QoA	L	Н	QoB
		The state of		UC		L	Н	QoA	Н	X	Rank A
		40	0 ×	OU	A BUS	L	Н	QoA	X	L	Rank A
H00 X	Jou	aum		Output	RANK B	Н.	X	A bus	L	Н	QoB
A-to-B Operation	L	Н	Input	of	RANK	Н	X	A bus	Н	X	Rank A
FoC P	1.1	6.1	4 1	Rank A	A	Н	X	A bus	X	L	Rank A
	DU	Av	pt H	1	BUS	X	L	A bus	L	Н	QoB
		1	1	1		X	L	A bus	Н	X	Rank A
300 H		74.5	OH			X	L	A bus	X	L	Rank A
-450 X	60	1	1 X	100		L	Н	QoA	L	Н	QoB
		p .	×	l ou		L	Н	QoA	Н	Х	Rank A
	1	1 /3	D Y	. OU	A BUS	L	Н	QoA	Х	L	Rank A
Transfer	ou	A Albert	Output	Output	RANK	Н	Х	Rank B	L	Н	QoB
Stored	L	L ar	of	of	RANK	H*	X	Rank B	Н	X	Rank A
Data		1.3%	Rank B	Rank A	B BUS	H*	X	Rank B	X	L	Rank A
		1 1/20	P H		300	X	L	Rank B	L	Н	QoB
		l las	o. A			X*	L	Rank B	Н	X	Rank A
		LAG	C() +1			X*	L	Rank B	X	L	Rank A

^{*} NOTE: These controls for OEAB, OEBA, GA1, GA2, GB1 and GB2 can cause race conditions.

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Bus Operation For 'LS566

OPERATION	The Street Street Street Street	CTION	DATA	A 1/O	BLOCK DIAGRAM		DCK LE (A)	RANK A	CAP HOUSE PROPERTY	OCK SLE (B)	RANK E
OF EMAILOW	OEAB	OEBA	A0-A7	B0-B7	DEOOK DIAGIAM	CKA	CKEA	A LASTO	СКВ	CKEB	THE STATE OF
860 1		T Ao	DI H			UC	X	QoA	UC	X	QoB
		Ao	0 14			UC	X	QoA	1	L	B bus
	- X	Ao	6 1 K		A	UC	X	QoA	1	Н	QoB
		Eugli	A N	+ -	BUS	t	L	A bus	UC	X	QoB
Storage	н	Н	Input	Input	В	1	L	A bus	1	L	B bus
		and		E	RANK A	1	L	A bus	1	Н	QoB
SioO I	-	bes		X	BUS	†	Н	QoA	UC	X	QoB
		1 sud				1	Н	QoA	1	L	B bus
		0000		-		1	Н	QoA	1	Н	QoB
Eco F		T Ad	о н			UC	X	QoA	UC	X	QoB
and 8	111	+				UC	X	QoA	1	L	B bus
		Ac Ac	БН		A BUS	UC	X	QoA	1	Н	QoB
		8 30	Output	+	RANK B	1	L	Rank B	UC	X	QoB
B-to-A Operation	Н	L	of	Input		1	Light	Rank B	1	L	B bus
and B		836	Rank B	H	RANK A B	1	Lan	Rank B	1	Н	QoB
		E Mai		T X	BUS	1	Н	QoA	UC	X	QoB
		I A I		X		1	Н	QoA	1	L	B bus
		1 5 14		T V		1	Н	QoA	1	Н	QoB
800		Ale	ot H			UC	X	QoA	UC	X	QoB
		-	o H	+		UC	X	QoA	1	L	Rank A
	X	II At	O I H		A BUS	UC	X	QoA	1	Н	QoB
		SUS	A N	Output	BUS RANK	1	L	A bus	UC	X	QoB
A-to-B Operation	L	Н	Input	of	RANK	July 1	L	A bus	1	L	Rank A
A sheet to				Rank A	A	A Nos	L	A bus	1	Н	QoB
				X	BUS	1	Н	QoA	UC	X	QoB
	-	-		H X		1	Н	QoA	1	L.	Rank A
		808				1	Н	QoA	1	Н	QoB
E-C I		Ac	0 4			UC	X	QoA	UC	X	QoB
			B H			UC	X	QoA	1	L	Rank A
		Ac Ac	D 1	-	A BUS	UC	X	QoA	1	Н	QoB
Transfer			Output	Output	BUS RANK B	1	L	Rank B	UC	X	QoB
Stored	L	L	of	of	RANK	1	L	Rank B	1	L	Rank A
Data			Rank B	Rank A	HANK A DO	Atis	E de	Rank B	1	Н	QoB
				N X	BUS	1	Н	QoA	UC	X	QoB
		a an				1	Н	QoA	1	L	Rank A
		Q 80				1	Н	QoA	1	Н	QoB

Bus Operation For 'LS567

OPERATION		CTION TROL	DAT	A I/O	BLOCK DIAGRAM	Comment of the last	ATE (A)	RANK A	G/ ENAB	ATE LE (B)	RANK E
OPERATION	OEAB	OEBA	A0-A7	B0-B7	BEOCK BIAGNAM	GA1	GA2	A ABBO	GB1	GB2	
800 X	00	Ao	C X	pu		L	Н	QoA	L	Н	QoB
	1.1	'Ao	C X	00		L	Н	QoA	Н	X	B bus
		A.	X	DU	A	L	Н	QoA	X	L	B bus
	NO.	gurd	1 2		BUS RANK B	Н	X	A bus	L	Н	QoB
Storage	Н	Á	Input	Input	RANK	Н	X	A bus	Н	X	B bus
		Str:T	5		A	Н	X	A bus	X	L	B bus
	30	4.0	P. H	1	BUS	X	L	A bus	L	Н	QoB
	1	10				X	L	A bus	Н	X	B bus
		\$ C	O H			X	L	A bus	X	L	B bus
1600 3	1-91.	130		30		L	Н	QoA	L	Н	QoB
	1	Ac	O X	DU		L	Н	QoA	Н	X	B bus
		A.	O X	l ou	A BUS	L	Н	QoA	X	L	B bus
	31	8.8	Output		BUS RANK B	Н	X	Rank B	L	Н	QoB
B-to-A Operation	Н	Ľ	of	Input	RANK	Н	X	Rank B	Н	X	B bus
Operation		S(x)n	Rank B		A B	Н	X	Rank B	X	L	B bus
	00	I Ac	OLH		BUS	X	L	Rank B	L	Н	QoB
		45	DJ. H			X	L	Rank B	Н	X	B bus
		Ac.	11 11	1 1		X	L	Rank B	X	L	B bus
800 7		PV.	L A	00		L	Н	QoA	L	Н	QoB
		A.	D X	00		L	Н	QoA	Н	X	Rank A
		L AC	D X	ou	A BUS	L	Н	QoA	X	L	Rank A
) or	30%	PA J	Output	RANK B	8H	X	A bus	L	Н	QoB
A-to-B Operation	L	H	Input	of	RANK	Н	X	A bus	Н	X	Rank A
C POTATION 1		IBUS	A 1	Rank A	A B	Н	X	A bus	X	L	Rank A
	QL	L As	D H		BUS	X	L	A bus	L	Н	QoB
		LL A	D H			X	L	A bus	Н	X	Rank A
	1	l A	() (Cx			X	L	A bus	X	L	Rank A
300	1.2		D X	3 00		L	Н	QoA	L	Н	QoB
		, Ac	D X	1 ou		L	Н	QoA	Н	X	Rank A
	1	1	0 X	au	A BUS	L	Н	QoA	X	L	Rank A
Transfer	2	a de	Output	Output	RANK	1 H 1	X	Rank B	L	Н	QoB
Stored	L	E Para	of	of		H*	X	Rank B	Н	X	Rank A
Data		E Na	Rank B	Rank A	RANK	H*	X	Rank B	X	L	Rank A
	101		Q H		BBUS	X	L	Rank B	L	Н	QoB
		100	0 1 11			X*	L	Rank B	Н	X	Rank A
			81.4			X*	L	Rank B	X	L	Rank A

* NOTE: These controls for OEAB, OEBA, GA1, GA2, GB1 and GB2 can cause race conditions.

SN54/74LS546 SN54/74LS547 SN54/74LS566 SN54/74LS567

Absolute Maximum Ratings

Supply voltage V _{CC}	0.5 V to 7 V
Input voltage	
Off-state output voltage	0.5 V to 5.5 V
Storage temperature	-65°C to +150°C

Operating Conditions

SYMBOL		PA	RAMETER	WIX			TYP	RY MAX	I show III	MMER TYP	CIAL	UNI	
VCC	Supply volta	ge	Vuv-	W.L.		4.5	5	5.5	4.75	5	5.25	V	
TA	Operating from	ee-air tempera	ature	10	KANA DOV	-55		125	0	Lewy-	75	°C	
	16.0		Am 98	High	WS S MAY	11	11			8			
	147 411 - 4 - 1		'LS546, 'LS566	Low	CK	19			15	her lake			
TW	Width of clo	ck/gate	W 0547 W 0507	High	GA1,GB1	10		1	8	ugajo		ns	
624			'LS547, 'LS567	Low	GA2,GB2	18			16				
Ale Fair		(8)	'LS546	CKA,	СКВ	141	hno	ngo are	111 STE IIO				
Am nn			'LS547	GA1, 0	GB1	5↓			5↓				
			L3547	GA2,	GB2	151			151			801	
T _{su}	Setup time		'LS566	CKA,	СКВ	141			111			ns	
Set -			'LS567	GA1, GB1		13↓ 22†		131		oal			
			L3367	GA2, GB2				221					
		Marian Carrows	'LS546	CKA,	СКВ	01			01				
			'LS547	GA1, (GB1	13↓			13↓				
т.	Hold time		L3347	GA2, GB2		51			51			-	
Th	Hold tillle		'LS566	CKA,	СКВ	01			01			ns	
			'LS567	GA1, (GB1	11↓			111				
			GA2, GB2		GB2	51			51				
T _{suce}	Setup time for	or CKEA, CKE	B, ('LS546, 'LS566	only)		15†			111			ns	
T _{hce}	Hold time for	CKEA, CKE	3 ('LS546, 'LS566 or	nly)	14-15	51			41		Hims	ns	

[†] the arrow indicates the transition of the clock/gate input used for reference:

for the low-to-high transitions.

for the high-to-low transitions.

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAME	TER	TEST CO	NDITIONS		ILITARY TYP MAX	COMMER MIN TYP		UNIT	
VIL	Low-level input v	oltage		4 × 1000 000 000 000 000 000		0.8	enug	0.8	V	
VIH	High-level input	oltage			2		2		V	
VIC	Input clamp volta	ige	V _{CC} = MIN	I _I = -18 mA		-1.5		-1.5	V	
Lo	Low-level input of	urrent	V _{CC} = MAX	A or B		-250		-250	μΑ	
IL	Low-level illput c	ullelli	V _I = 0.4 V	All others		-400	Ni.	μΑ		
¹ IH	High-level input	current	V _{CC} = MAX	V _I = 2.7 V	20		0 2 20 0 100 40	20	μΑ	
HAC LAN	Maximum input	AorB	V _{CC} = MAX	V _I = 5.5 V	0.1		0.1		mA	
V 818	current		AGG - MAX	V _I = 7.0 V		0.1			-37	
V P	Low-level		V _{CC} = MIN	I _{OL} = 24 mA	otuse	0.5	it polizieg(V	
VOL	output voltage		V _{IL} = MAX V _{IH} = 2V	I _{OL} = 32 mA			0.35 0.5		V	
V	High-level V _{CC} = MIN		V _{CC} = MIN	I _{OH} = −1 mA	2.4	3.4	enter besettente		V	
VOH	output voltage		V _{IL} = MAX V _{IH} = 2V	I _{OH} = -2.6 mA	au l		2.4 3.1		V	
lozL	Ofr-state output	urrant	V MANY	V _O = 0.4 V		-250		-250	^	
IOZH	On-state output t	current	V _{CC} = MAX	V _O = 2.4 V		20		20	μΑ	
los	Output short-circ	uit current*	V _{CC} = MAX	THE STATE OF THE S	-30	-130	-30	-130	mA	
10	- 10	101	26.0 (14)	'LS546		180	amit quisi	180	ual	
loo	Supply current		V _{CC} = MAX	'LS547	0.3	180	180 18		mA	
cc	Supply Current		Outputs open	'LS566	But.	180		180	IIIA	
			180 1	'LS567		180		180		

^{*} Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

Switching Characteristics Over Operating Conditions

		anolillane	MILI	TARY	COMM	11 11/10	
SYMBOL	PARAMETER	TEST CONDITIONS	'LS546 MIN MAX	'LS547 MIN MAX	'LS546 MIN MAX	'LS547 MIN MAX	UNIT
f _{MAX}	Maximum clock frequency	PAR NAME OF STREET	33		43		MHz
t _{PLH} /t _{PHL}	CK to output delay ('LS546 only)	$C_1 = 45 \text{pF} R_L = 280 \Omega$	26	velat	21	X	ns
^t PLH ^{/t} PHL	GA1, GA2, GB1 or GB2 to output delay ('LS547 only)		jā 19,ĕ4 = J = 3 0	27	LSS66 only I A J. GAŽ, GI Z to outers	24	ns
t _{PLH} /t _{PHL}	Data D to output delay ('LS547 only)			23	Vec2J) yeld	18	ns
t _{PZL} /t _{PZH}	Output enable delay	C _L = 45 pF R _L = 280 Ω	25	25	21	21	ns
t _{PLZ} /t _{PHZ}	Output disable delay	C _L = 5 pF R _L = 280 Ω	22	22	19	19	ns

Switching Characteristics V_{CC} = 5 V, T_A = 25°C 2008 = AT M = 200V stall bit add as small stall stall be a small stall be

SYMBOL	PARAMETER	TEST CONDITIONS	'LS546 MIN MAX	'LS547 MIN MAX	UNIT
fMAX	Maximum clock frequency	yaner	50	estr.	MHz
^t PLH ^{/t} PHL	CK to output delay ('LS546 only)		valeb lugh 19	NC PHENN	ns
t _{PLH} /t _{PHL}	GA1, GA2, GB1 or GB2 to output delay ('LS547 only)		CAS, CB1 or C		ns
t _{PLH} /t _{PHL}	Data D to output delay ('LS547 only)		s D to output dell 567 anly)	1/	ns
t _{PZL} /t _{PZH}	Output enable delay	C _L = 45 pF R _L = 280 Ω	yelob eldan 19 o	19	ns
t _{PLZ} /t _{PHZ}	Output disable delay	$C_1 = 5 pF R_1 = 280 \Omega$	ulab aldaz 17.0	17	ns

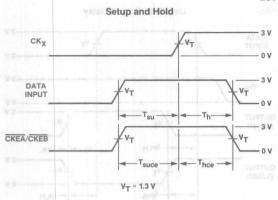
Switching Characteristics Over Operating Conditions

	BASEL YARS	1 0902 F 301(3)	MILI	TARY	COMM	10	
SYMBOL	PARAMETER	TEST CONDITIONS	'LS566 MIN MAX	'LS567 MIN MAX	'LS566 MIN MAX	'LS567 MIN MAX	UNIT
fMAX	Maximum clock frequency		33	Value	43		MHz
t _{PLH} /t _{PHL}	CK to output delay ('LS566 only)	$C_L = 45 \text{ pF} R_L = 280 \Omega$	26	JD	21		ns
^t PLH ^{/t} PHL	GA1, GA2, GB1 or GB2 to output delay ('LS567 only)			26	under or Service (12.347) and Grater (12.347)	24	ns
t _{PLH} /t _{PHL}	Data D to output delay ('LS567 only)	ee rome.	S To St. 1	29	Maria Juctivi	23	ns
t _{PZL} /t _{PZH}	Output enable delay	C _L = 45 pF R _L = 280 Ω	25	25	21	21	ns
^t PLZ ^{/t} PHZ	Output disable delay	C _L = 5 pF R _L = 280 Ω	22	22	19	19	ns

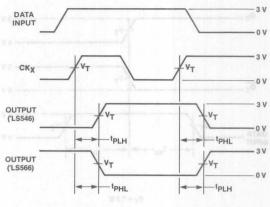
SYMBOL	PARAMETER	TEST CONDITIONS	'LS566 MIN MAX	'LS567 MIN MAX	UNIT
fMAX	Maximum clock frequency	vone:	50 H A: 010 H 50	reM y	MHz
^t PLH ^{/t} PHL	CK to output delay ('LS566 only)		19		ns
^t PLH ^{/t} PHL	GA1, GA2, GB1 or GB2 to output delay ('LS567 only)		5 to real place. Ted calley 1.5547		ns
t _{PLH} /t _{PHL}	Data D to output delay ('LS567 only)		n Die opien det Se7 only/	19	ns
t _{PZL} /t _{PZH}	Output enable delay	$C_L = 45 pF R_L = 280 \Omega$	vsleti siden 19.0	19	ns
t _{PLZ} /t _{PHZ}	Output disable delay	$C_L = 5 pF R_L = 280 \Omega$	vsieh odeat17.d	17	ns

Definition of Waveforms





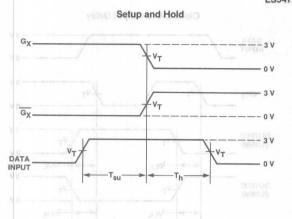
Clock CK to Output Delay



V_T = 1.3 V

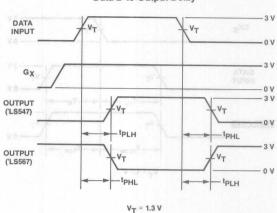
Definition of Waveforms

'LS547/567

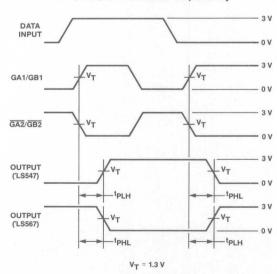


V_T = 1.3 V

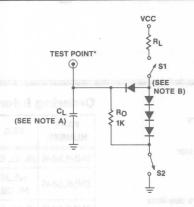
Data D to Output Delay



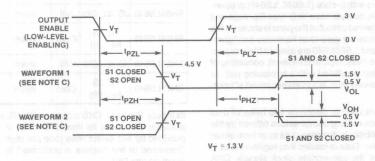
GA1, GA2, GB1 or GB2 to Output Delay



Test Load



* The "TEST POINT" is driven by the output under test, and observed by instrumentation.



ENABLE AND DISABLE

NOTES: A. CLincludes probe and jig capacitance.

- B. All diodes are 1N916 or 1N3064.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - D. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
 - E. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, Z_{out} = 50Ω and $t_R \leq$ 15 ns $t_F \leq$ 6 ns.
 - F. When measuring propagation delay times of 3-state outputs, switches S1 and S2 are closed.

8-Bit Bus Front-Loading-Latch Transceivers

SN54/74LS646 SN54/74LS648 SN54/74LS647 SN54/74LS649

Features/Benefits

- · Bidirectional bus transceivers and registers
- Independent registers for A and B buses
- · Real-time data transfer or stored data transfer
- 24-pin SKINNYDIP® saves space
- · 8-bit data path matches byte boundaries
- . Three-state or open-collector outputs drive bus lines

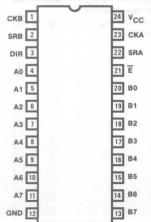
Description

The 8-bit bus transceivers with 3-state ("LS646, 'LS648) or open-collector ("LS647, 'LS649) outputs have 16 D-type flip-flops and multiplexers. The bus-oriented pinout of the parts is shown in the Pin Configuration. The internal gate-level hardware configurations for the 'LS646/647 and 'LS648/649 are given in their respective Logic Diagrams. The basic repeated element, consisting of an edge-triggered flip-flop paralleled with a bypassing path or "feed-through" into a two-way mux, is sometimes called a "front-loading latch"

A pair of multiplexers are used to distribute two bytes of data through the part. The data-routing combinations offered by the multiplexers provide flexibility in directing data to or from either bus, and/or either register. Data is loaded into registers A or B upon the rising edge of the appropriate clock signals. CKA clocks register A, which receives data from the B bus directly at

Pin Configurations

'LS646/647/648/649 8-Bit Bus Front-Loading-Latch Transceivers



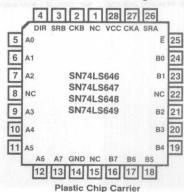
Ordering Information

PART NUMBER	PKG	TEMP	POLARITY	O/P	PWR
SN54LS646	JS,W,L (28)	Mil	Noninvert	Three-state	LS
SN54LS646	NS,JS NL (28)	Com	Noninvert	Three-state	LS
SN54LS647	JS,W,L (28)	Mil	Noninvert	Open-	LS
SN74LS647	NS,JS NL (28)	Com	Noninvert	collector	LS
SN54LS648	JS,W,L (28)	Mil	Invert	Three-state	LS
SN54LS648	NS,JS NL (28)	Com	Invert	Three-state	LS
SN54LS649	JS,W,L (28)	Mil	Invert	Open-	LS
SN74LS649	NS,JS NL (28)	Com	Invert	collector	LS

its inputs. Similarly, CKB clocks register B, which has the A bus available directly at its inputs. Control of the multiplexers is provided by two select lines (one per register), SRA and SRB. Command of the outputs is performed by enable line $\overline{\mathbb{E}}$, and direction line DIR.

When \overline{E} is High data from the buses can be stored into register A and B. When \overline{E} is Low and DIR is High, the direction of operation is from A to B; when \overline{E} and DIR are LOW, the direction of operation is from B to A.

SRA is used to select between register A and the B bus, and then to route the data to a controlled buffer connected to the A bus. Likewise, SRB selects between register B and the A bus, and then routes the data to the B bus through a controlled buffer.



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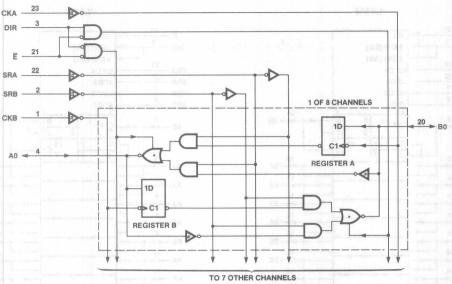
TWX: 910-338-2376

Monolithic Memories



Logic Diagrams

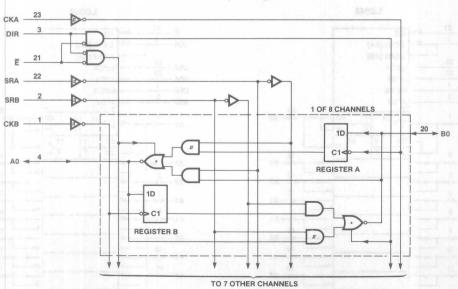
'LS646/647 (Non-Inverting)



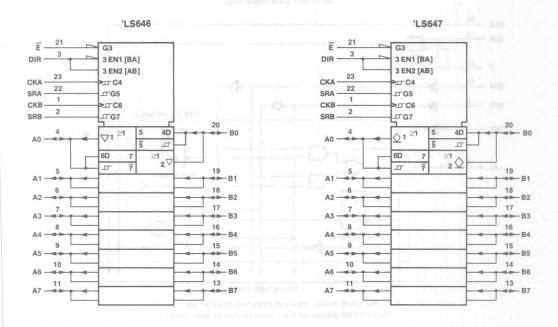
* For the 'LS646 devices, the A and B bus outputs are 3-state.

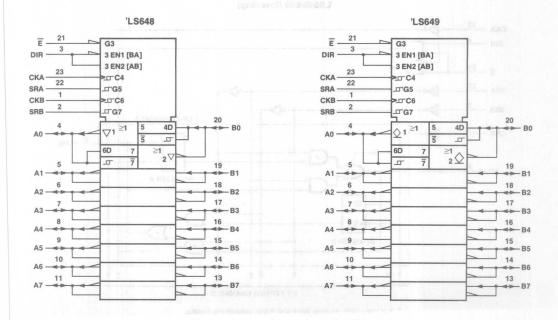
For the 'LS647 devices, the A and B bus outputs are open-collector.

'LS648/649 (Inverting)

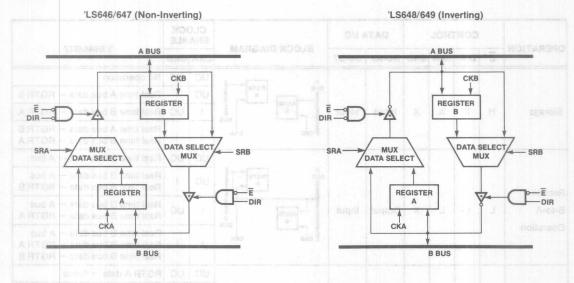


* For the 'LS648 devices, the A and B bus outputs are 3-state.
For the 'LS649 devices, the A and B bus outputs are open-collector.





Block Diagrams



* For the 'LS646/648 devices, the A and B bus outputs are 3-state. For the 'LS647/649 devices, the A and B bus outputs are open-collector.

Function Table **Nomenclature Description**

E: FITTOR	To enable the A-to-B or B-to-A operation.
DIR:	To select the direction of operation.

E	DIR	OPERATION DIRECTION
L	A L	paud A ametines B-to-A
L	Hua	A-to-B
Н	X	A and B buses both are inputs (storage

SRA/SRB: To select the output data coming from the A/B register if SRA/SRB is a High level; otherwise, directly from the input data bus.

A0-A7: Eight input/output pins on the A side. B0-B7: Eight input/output pins on the B side.

CKA/CKB: Clock for Register A/B.

X: H or L state irrelevant ("Don't Care" conditions). 1: Positive edge of CK causes clocking, if clock enable

is asserted.

UC: H or L or I case (nonclocked operation).

RGTR: Register.

Bus Operation for 'LS646/647

		CONTROL DATA I/O			A I/O	ENA		DCK	11 0040/047															
OPERATION	Ē	DIR	SRA	SRB	A0-A7	B0-B7	BLOCK DIAGRAM	CKA	СКВ	'LS646/647														
		8563					A	UC	UC	No operation														
			1				BUS RGTR	UC	1	Real time A bus data → RGTR E														
Storage	Н	X	X	X	Input	Input	RGTR B B BUS	1.	UC	Real time B bus data → RGTR A														
		2000	7	1			скв ска	1	t	Real time A bus data → RGTR B Real time B bus data → RGTR A														
1212 81	18	12 /		1/10	LES ATA	1	8742	UC	UC	Real time B bus data → A bus														
Real time			r	iai ai a	105		A BUS RGTR A	UC	t	Real time B bus data → A bus Real time B bus data → RGTR B														
B-to-A	L	L	L	X	Output	Input	RGTR B B BUS	1	UC	Real time B bus data → A bus Real time B bus data → RGTR A														
Operation		a cuo se	SUS:			aller in	скв ска	1	1	Real time B bus data → A bus Real time B bus data → RGTR A Real time B bus data → RGTR B														
								UC	UC	RGTR A data → A bus														
Stored data				(j) 7/4 <u>0</u>	stata 6 eks o-rego em	atectuc a aboqua a	A BUS RGTR	uc	5 F	RGTR A data → A bus RGTR A data → RGTR B														
B-to-A	L	L	Н	X	Output	Input	RGTR B BUS	†	uc	Real time B bus data → RGTR A RGTR A data → A bus														
Operation												OT ASSE	-1 -50	-T-863	-T-86	-T -643		-T -64			СКВ СКА	t	t	Real time B bus data → RGTR A RGTR A data → A bus RGTR A data → RGTR B
seivisido le	e ren	H B	al 81	SVAR	i i neter	081		UC	UC	Real time A bus data → B bus														
Real time		id sin ett re	n Kuci Ionici	u granii Surghijo	edly from at impute	nito griš	A BUS RGTR A	UC	-al-a	Real time A bus data → B bus Real time A bus data → RGTR B														
A-to-B	L	Н	X	weters service	Input	Output	RGTR	T T	UC	Real time A bus data → B bus Real time A bus data → RGTR A														
Operation		oio a	ri, ina seano	islent KOtos	r L state Hivè edgi	6 F 609	BUS CKA	ORR	G AC	Real time A bus data → B bus Real time A bus data → RGTR A Real time A bus data → RGTR B														
rafi	8800	biento	digao	(t) essa	3 ino / 1	oH:	200	UC	UC	RGTR B data → B bus														
Stored data					, salan	gef)	A BUS RGTR A	UC	Na da	Real time A bus data → RGTR B RGTR B data → B bus														
A-to-B	L	н	X	н	Input	Output	RGTR	1	UC	RGTR B data → B bus RGTR B data → RGTR A														
Operation							CKB CKA	t	t	Real time A bus data → RGTR B RGTR B data → B bus RGTR B data → RGTR A														

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Bus Operation for 'LS648/649

OPERATION	CONTROL DATA I/O			A I/O			BLE	A CONTRACTOR OF THE STATE OF TH		
OPERATION	Ē	DIR	SRA	SRB	A0-A7	B0-B7	BLOCK DIAGRAM	CKA	СКВ	'LS648/649
							A	UC	UC	No operation
		in all		YAR	TLSM		BUS RGTR	UC	t t	Real time A bus data → RGTR E
Storage	Н	X	X	X	Input	Input	RGTR B B BUS	1	UC	Real time B bus data → RGTR A
		29.	0 8		83		CKB CKA	6100	oet a	Real time A bus data → RGTR E Real time B bus data → RGTR A
Lan Lan		- 14			-1-		ngift	UC	UC	Real time B bus data → A bus
Real time			8				A BUS RGTR	UC	1	Real time $\overline{\underline{B}}$ bus data \rightarrow A bus Real time $\overline{\underline{B}}$ bus data \rightarrow RGTR $\overline{\underline{B}}$
B-to-A	L	L.	L	Х	Output	Input	RGTR B	1	UC	Real time \overline{B} bus data \rightarrow A bus Real time B bus data \rightarrow RGTR A
Operation			9			0	CKB CKA	1	eta	Real time B bus data → A bus Real time B bus data → RGTR A Real time B bus data → RGTR B
		in cons	and and	doid an	Treld	Unicest etc.		UC	UC	RGTR Ā data → A bus
Stored data						busted it select	A BUS RGTR	uc	† sai	RGTR A data → A bus RGTR A data → RGTR B
B-to-A	L	r Lo	Н	Х	Output	Input	RGTR B BUS	t	UC	Real time B bus data → RGTR A RGTR Ā data → A bus
Operation		3	11.0				CKB CKA	1	1 89	Real time B bus data → RGTR A RGTR Ā data → A bus RGTR Ā data → RGTR B
LYLES	Hira me		8.7			Am	81- = 1 WM = 0.21	UC	UC	Real time A bus data → B bus
Real time		5.0	1	5.1	10		A BUS RGTR A	UC	T _{ine}	Real time A bus data → B bus Real time A bus data → RGTR B
A-to-B	L	Н	X	L	Input	Output	RGTR	1	UC	Real time $\overline{\underline{A}}$ bus data \rightarrow B bus Real time $\overline{\underline{A}}$ bus data \rightarrow RGTR A
Operation			1 3.00	85.0			CKB CKA	1	ta lii 1 epsi	Real time A bus data → B bus Real time A bus data → RGTR A Real time A bus data → RGTR B
Para de la constante de la con	or v		1				THE SHEET SHEET HE	UC	UC	RGTR B data → B bus
Stored data		5		7			A BUS RGTR A	UC	1	Real time A bus data → RGTR B RGTR B data → B bus
A-to-B	L	Н	x	н	Input	Output	RGTR B B	1	UC	RGTR B data → B bus RGTR B data → RGTR A
Operation			8% 7%		LO-		CKB CKA	1	1	Real time A bus data → RGTR B RGTR B data → B bus RGTR B data → RGTR A

Absolute Maximum Ratings

Supply voltage V _{CC}	0.5 V to 7 V
Input voltage	
Off-state output voltage	-0.5 V to 5.5 V
Storage temperature -65	°C to +150°C

Operating Conditions

SYMBOL	PARAMETER MIN TYP MAX		COMMERCIAL MIN TYP MA	LIMIT	
VCC	Supply voltage	P.8	4.5 5 5.	5 4.75 5 5.2	5 V
TA	Operating free air temp	perature	-55 12	5 0 7	5 °C
t _w Width of clock	High	20	20		
	Width of Clock	Low	20	20	ns
8,ET93 -	Setup time	'LS646	20 t	20 t	
^I su	Setup time	'LS648	20 1	20 t	ns
A RITOR	Hold time	'LS646	01	0 1	-A-01
th	Hold time	'LS648	0 t	0 1	ns
ГОН	High-level output curre	ent	-1	2 -1	5 mA
loL	Low-level output curre	nt	1	2 2	4 mA

¹ In the arrow indicates the transition of the clock input used for reference. 1 for the low-to-high transitions. I for the high-to-low transitions.

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER			TEST	CONDITIONS	MILITARY MIN TYP MAX		CON	UNIT			
VIL	Low-level input vo	oltage	1 70	3	680 5			0.7		1	0.8	V
V _{IH}	High-level input v				2			2			V	
VIC	Input clamp volta	VCC	= MIN	I _I = -18 mA			-1.5			-1.5	V	
∆ V _T	Hysteresis (V _{T+} -V	VCC=	MIN		0.1	0.4		0.2	0.4		V	
ehr an	Low-level input co	VCC	= MAX	V _I = 0.4 V			-0.4			-0.4	mA	
IH de	High-level input of	urrent	VCC	= MAX	V _I = 2.7 V			20		1	20	μΑ
ARTER -	Maximum input	A or B	Vac	= MAY	V _I = 5.5 V	- Constant	-,0	0.1			0.1	mA
and &	current	All others	V _{CC} = MAX		V _I = 7 V		0.1				0.1	
ATTOR -	at bime A bus data h	0H 1	VCC = MIN		I _{OL} = 12 mA		0.25	0.4	100	0.25	0.4	
VOL	Low-level output voltage		VIL = MAX VIH = 2 V		IOL = 24 mA		-	1	1	0.35 0.5		V
But the			VCC	= MIN	I _{OH} = -3 mA	2.4	3.4	17	2.4	3.4		
VOH	High-level output	voltage	VIL	= MAX = 2 V	IOH = MAX	2		T	2		a le	V
lozL	Trail data - B bus	19	VCC	= MAX	V _O = 0.4 V	i daem	el lei	-400			-400	μΑ
lozh	Off-state output of	urrent	VIL	= MAX = 2 V	V _O = 2.7 V			20			20	μΑ
los	Output short-circ	uit current*	+	= MAX	8404	-40		-225	-40		-225	mA
A	William - state & Artis	08			Outputs High			145		T	145	-
				'LS- 646	Outputs Low			165		-	165	-
lcc s			V _{CC} =		Outputs Disabled	16		165		165		mA
	Supply current	Supply current			Outputs High			145			145	
				'LS- 648	Outputs Low			165			165	
				010	Outputs Disabled						165	

^{*} Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load/Waveforms)	'LS646 MIN MAX	'LS648 MIN MAX	UNIT
t _{PLH}		perioden en e	18	18	ns
tPHL	Data to output delay		20	25	ns
t _{PLH}	011-44-1-1-		25	25	ns
tPHL	Clock to output delay		35	40	ns
t _{PLH}	Select to output delay	O - 45-5 D - 6670	40	55	ns
tPHL	(data input High)	C _L = 45pF R _L = 667Ω	35	40	ns
tPLH	Select to output delay		50	40	ns
t _{PHL}	(data input Low)		25	40	ns
tpZL	Output enable delay		65	pota lo atbliv 55	ns
^t PZH	Output enable delay		55	50	ns
t _{PLZ}	Output disable delay	C - 5-5 D - 6670	35	amii quiee 35	ns
t _{PHZ}	Output disable delay	$C_L = 5pF R_L = 667\Omega$	35	45	ns
tPZL	Direction anable delay	C - 45-F D - 6670	60	45	ns
t _{PZH}	Direction enable delay	$C_L = 45pF$ $R_L = 667\Omega$	agaflov 45	up level-dg/H 40	ns
t _{PLZ}	Direction disable delay	C - 50E D - 6670	30	tuo leval-woul 30	ns
t _{PHZ}		$C_L = 5pF$ $R_L = 667\Omega$	30	Diana and Managara 35	ns

SYMBOL		TEST CONDITIONS	1921	MIL	C	MC	N. S. C. C. C. C.
	PARAMETER	(See Test Load/Waveforms)	'LS646 MIN MA	'LS648 MIN MAX	"LS646 MIN MAX	'LS648 MIN MAX	UNIT
^t PLH	Data to output delay	Amete au	им = 2	5 18	25	18 mai 18	ns
^t PHL	Data to output delay		2	5 25	25	25	ns
t _{PLH}	Clock to output delay	V ₁ = 0.4 V	2	8 25	28	25	ns
t _{PHL}	Clock to output delay	V 5.2 = A'	3	5 40	35	40	ns
^t PLH	Select to output delay †	C _L = 45pF R _L = 667Ω	4	0 55	40	55	ns
t _{PHL}	(data input High)	C[- 45pr H[- 66/11	3	5 40	35	amua 40	ns
t _{PLH}	Select to output delay †	An 21 = 101	5	0 40	50	40	ns
tPHL	(data input Low)	Ant kil = joi	MAM = 3	0 40	30	40	ns
tPZL	Output enable delay		6	5 55	65	55	ns
t _{PZH}	Cutput enable delay	vaa-dev	XAM = 5	5 50	55	50	ns
tPLZ	Output disable delay	C 5nF D - 6670	V 5 = 4	5 35	45	35	ns
t _{PHZ}	Output disable delay	$C_L = 5pF R_L = 667\Omega$	4	5 50	45	50	ns
t _{PZL}	Direction enable delay	$C_1 = 45pF R_1 = 667\Omega$	6	0 45	60	45	ns
t _{PZH}	Direction enable delay	CL - 43PF RL - 66/11	4	5 40	45	40	ns
t _{PLZ}	Direction disable delay	C 5nE P 6670	4	30	40	30	ns
tPHZ	Direction disable delay	$C_L = 5pF$ $R_L = 667\Omega$	4	5 45	45	45	ns

[†] See Figure 4.

Absolute Maximum Ratings

The state of the s
Supply voltage, V _{CC}
Input voltage,
Off-state output voltage
Storage temperature

Operating Conditions

SYMBOL	PARAM	ETER (stage of Higher stage)	MILITARY MIN TYP MAX	COMMERCIAL MIN TYP MAX	UNIT
Vcc	Supply voltage		4.5 5 5.5	4.75 5 5.25	V
TA	Operating free air temperature		-55 125	0 75	°C
		High	20	20	200
t _W	Width of clock	Low	20	20	ns
70 11 12		'LS647	20 t	20 1	124
tsu	Setup time	'LS649	20 t	201	ns
TA . (28)	8	'LS647	0 †	0 1	BHT.
t _h	Hold time	'LS649	0 †	0 1	ns
VOH	High-level output voltage		5.5	5.5	V
loL	Low-level output current		12	24	mA

^{↑ ↓} The arrow indicates the transition of the clock input used for reference. ↑ for the low-to-high transitions. ↓ for the high-to-low transitions.

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMET	ER	186	TEST	CONDITIONS		ILITAF TYP		COMMER MIN TYP	UNIT	
VIL	Low-level input ve	oltage	894	1.86	(emar) son't 2 section T as	43.		0.7	ANNE	0.8	V
VIH	High-level input v	oltage	AAA VAN			2	1827 . 1		2		V
Vic	Input clamp volta	ge	Vcc	MIN	I _I = -18 mA			-1.5	crop of sie	-1.5	V
ΔV _T	Hysteresis (V _{T+} -V	′ _{T-})	V _{CC} =	MIN		0.1	0.4		0.2 0.4		V
1 _{IL}	Low-level input c	urrent	VCC	= MAX	V _I = 0.4 V		vel	-0.4	luc of stack	-0.4	mA
ТН	High-level input of	urrent	Vcc	= MAX	V _I = 2.7 V			20		20	μΑ
10 36	Maximum input	A or B	V	= MAX	V _I = 5.5 V	0	PURC	0.1	luc of foels	0.1	mA
11	current	All others	,CC	- IVIAA	V ₁ = 7 V			0.1	Transport suggests	0.1	IIIA
811	l lug	04	Vcc	= MIN	I _{OL} = 12 mA		0.25	0.4	0.2	5 0.4	1.19
VOL	Low-level output	voltage	VIL	= MAX = 2 V	IOL = 24 mA			2000	0.3	5 0.5	V
Гон	High-level output	current	V _{CC} V _{IL} V _{IH}	= MIN = MAX = 2 V	V _{OH} = 5.5 V ³		Y	100	utput enab	100	μА
The The	I FIA	50	BA		Outputs High			130	THE U SHI 1912	130	SHST
4 7			100	'LS- 647	Outputs Low			150		150	isel
n Da	as .		V _C C=		Outputs Disabled	-	No.	150		150	mA
'cc	Supply current		MAX		Outputs High			130		130	SIG
0.00			100	'LS- 649	Outputs Low	10	N Kalut	150		150	ZHet.
College Constitution					Outputs Disabled		CLUB TO THE	150		150	IR duB

^{*} Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

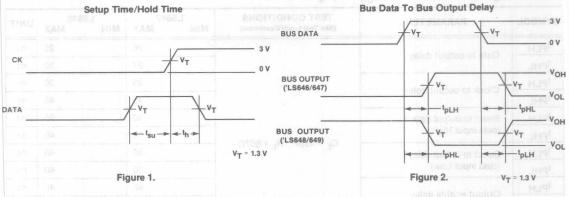
SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load/Waveforms)	'LS647 MIN MAX	'LS649 MIN MAX	UNIT
t _{PLH}	Date to a start delay	N. C.	26	25	ns
t _{PHL}	Data to output delay	70	27	30	ns
tPLH	Clask to authort dalar	TOT OF BUE	35	30	ns
tPHL	Clock to output delay		45	45	ns
^t PLH	Select to output delay†		50	55	ns
t _{PHL}	(data input High)	TUTTUO SUE	45	45	ns
t _{PLH}	Select to output delay†	$C_L = 45pF R_L = 667\Omega$	60	45	ns
t _{PHL}	(data input Low)		30	40	ns
t _{PLH}	Output enable delay		40	40	ns
t _{PHL}	Output enable delay	Bus Guiput Propagation Dalay T	50	50	ns
t _{PLH}	Direction anable delay		35	30	ns
tPHL	Direction enable delay	1 × +	40	45	ns

Switching Characteristics Over Operating Range

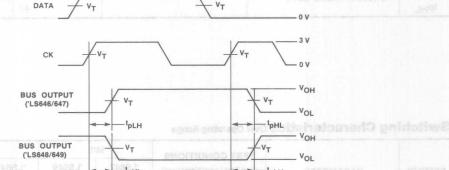
		TEST CONDITIONS	M	IIL TUNTUO	CC		
SYMBOL	PARAMETER	(See Test Load/Waveforms)	'LS647 MIN MAX			'LS649 MIN MAX	UNIT
t _{PLH}	Data to sutant dalan	TW STREET	32	35	32	35	ns
^t PHL	Data to output delay		27	30	27	30	ns
t _{PLH}	Clock to output dolor.		35	40	35	40	ns
t _{PHL}	Clock to output delay		45	45	45	45	ns
t _{PLH}	Select to output delay†		50	55	50	55	ns
^t PHL	(data input High)	- C _L = 45pF R _L = 667Ω	45	45	45	45	ns
t _{PLH}	Select to output delay†		60	50	60	50	ns
t _{PHL}	(data input Low)		30	40	30	40	ns
^t PLH	Output enable delay		40	45	40	45	ns
^t PHL	Output enable delay		50	50	50	50	ns
^t PLH	Direction enable delay		40	45	40	45	ns
tPHL	Direction enable delay		40	45	40	45	ns

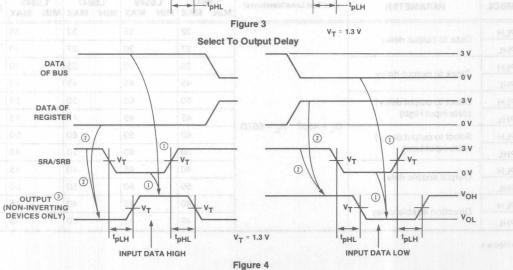
† See Figure 4.

Test Waveforms



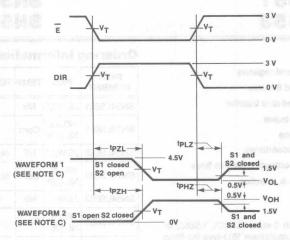
CK To Bus Output Propagation Delay Time



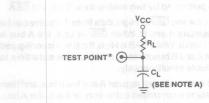


- NOTES: 1. When SRA/SRB is low, the input data will transfer to output bus.
 - 2. When SRA/SRB is high, the data of register will transfer to output bus.
 - 3. For the inverting devices, the timing is similar, but the output is opposite to that for the non-inverting devices.

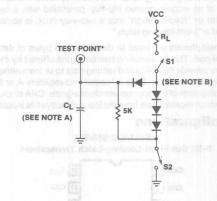
Enable/Disable/Direction-Change Delay



Test Loads



Load Circuit For Open-Collector Outputs



Load Circuit For Three-State Outputs

- * The "TEST POINT" is driven by the output under test, and observed by instrumentation.
- Notes: A. C_L includes probe and jig capacitance.
- B. All diodes are 1N916 or 1N3064.
 - C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - D. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
 - E. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz. Z_{OUT} = 50 Ω and t_R = 15 ns t_F \leq 6 ns.
 - F. When measuring propagation delay times of three-state outputs, switches S1 and S2 are closed.

Features/Benefits

- · Bidirectional bus transceivers and registers
- · Independent registers for A and B buses
- · Real-time data transfer or stored data transfer
- Simultaneous outputs on both buses
- 24-pin SKINNYDIP® saves space
- · 8-bit data path matches byte boundaries
- Three-state or open-collector outputs drive bus lines
- 'LS653/4 are open-collector in A direction, three-state in B direction

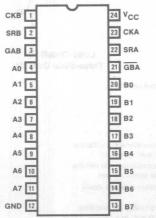
Description

These 8-bit bus transceivers with 3-state ('LS651, 'LS652) or open-collector ('LS653, 'LS654) outputs have 16 D-type flip-flops and multiplexers. The bus-oriented pinout of the parts is shown in the Pin Configuration. The internal gate-level hardware configurations for the 'LS651/653 and 'LS652/654 are given in their respective Logic Diagrams. The basic repeated element, consisting of an edge-triggered flip-flop paralleled with a bypassing path or "feed-through" into a two-way mux, is sometimes called a "front-loading latch."

A pair of multiplexers are used to distribute two bytes of data through the part. The data-routing combinations offered by the multiplexers provide flexibility in directing data to or from either bus, and/or either register. Data is loaded into registers A or B upon the rising edge of the appropriate clock signals. CKA clocks register A, which receives data from the B bus directly at its inputs.

Pin Configurations

'LS651/652/653/654 8-Bit Bus Front-Loading-Latch Transceivers



Ordering Information

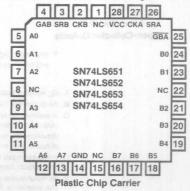
PART NUMBER	PKG	TEMP	POLARITY	OUTPUTS	POWER
SN54LS651	JS,W,L*	Mil	Invert	Three-state	LS
SN74LS651	NS,JS, NL (28)	Com	Invert	Three-state	LS
SN54LS652	JS,W,L*	Mil	Noninvert	Three-state	LS
SN74LS652	NS,JS, NL (28)	Com	Noninvert	Three-state	LS
SN54LS653	JS,W,L*	Mil	Invert		LS
SN74LS653	NS,JS, NL (28)	Com	Invert	A bus open- collector;	LS
SN54LS654	JS,W,L*	Mil	Noninvert	B bus three-state	LS
SN74LS654	NS,JS, NL (28)	Com	Noninvert	tinee-state	LS

^{*} L package here is L28. The other packages are 24-pin.

Similarly, CKB clocks register B, which has the A bus available directly at its inputs. Control of the multiplexers is provided by two select lines (one per register), SRA and SRB. Command of the outputs is performed by two enable lines, GAB and $\overline{\text{GBA}}$.

When GAB is Low and GBA is High, data from the buses can be loaded into registers A and B. When GBA is Low, the A bus is configured for output. When GAB is High, the B bus is configured for output. The A and B buses can be enabled at the same time, to operate as outputs simultaneously.

SRA is used to select between register A and the B bus, and then to route the data to a controlled buffer connected to the A bus. Likewise, SRB selects between register B and the A bus, and then routes the data to the B bus through a controlled buffer.

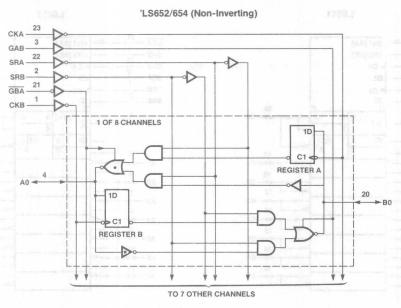


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TWX: 910-338-2376

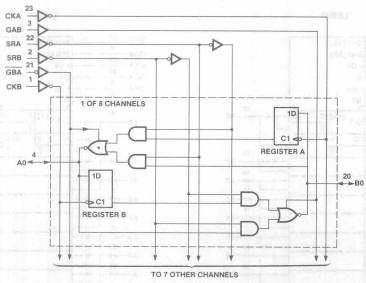
Monolithic MMI Memories

Logic Diagrams



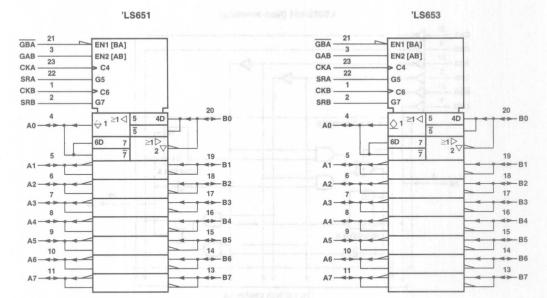
* For the 'LS652 devices, the A bus outputs are 3-state. For the 'LS654 devices, the A bus outputs are open-collector. The B bus outputs are 3-state for both devices.

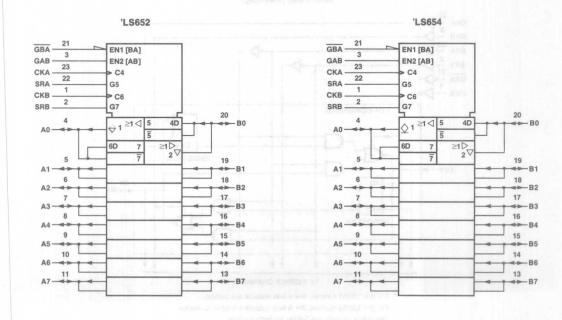
'LS651/653 (Inverting)



* For the 'LS651 devices, the A bus outputs are 3-state. For the 'LS653 devices, the A bus outputs are open-collector. The B bus outputs are 3-state for both devices.

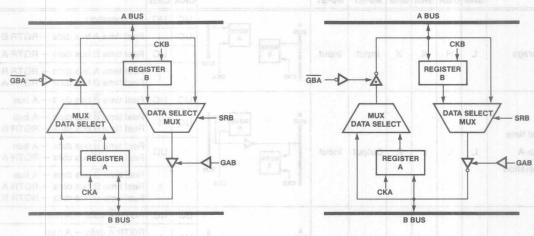
IEEE Symbols





'LS652/654 (Non-Inverting)

'LS651/653 (Inverting)



^{*} For the 'LS651/652 devices, the A bus outputs are 3-state.

For the 'LS653/654 devices, the A bus outputs are open-collector.

The B bus outputs are 3-state for both devices.

Function Table Nomenclature Description

GAB: To enable the A-to-B operation.
GBA: To enable the B-to-A operation.

GAB	GBA	OPERATION DIRECTION
L	Epcl	B to A S HTOA OU CAU
Lan	H	A and B buses both are inputs (storage)
Н	E SERVI	A and B buses both are outputs (Transfer stored data to bus)
Н	Н	A to B

SRA/SRB: To select the output data coming from the A/B register if SRA/SRB is High level; otherwise, directly

from the input data bus.

A0-A7: Eight input/output pins on the A side.

B0-B7: Eight input/output pins on the B side.

CKA/CKB: Clock for Register A/B.

X: H or L state irrelevant ("Don't Care" conditions).

Positive edge of CK causes clocking, if clocking

enable is asserted.

UC: H or L or I case (nonclocked operation).

RGTR: Register.

t: A

Bus Operation for 'LS651/653

OPERATION		CON	TROL		DAT	A I/O	BLOCK DIAGRA	B.ff		BLE	LS651/653
OPERATION	GAB	GBA	SRA	SRB	A0-A7	B0-B7	BLOCK DIAGRAI	IVI	CKA	СКВ	LS051/053
		10000000	USA	avede:	special district	sassasan.		WE CHES	UC	UC	No operation
			1				BUS RGTR A		UC	1	Real time A bus data → RGTR E
Storage	L	Н	X	X	Input	Input	RGTR B	В	1	UC	Real time B bus data → RGTR A
		E STEEL	158		À	() - E	скв с	BUS	1	RETA T	Real time A bus data → RGTR E Real time B bus data → RGTR A
				-				-	UC	UC	Real time B bus data → A bus
Real time	19.186 19.13	2		Z	XUH UBB ATAG	\$	A BUS RGTR A	1	UC	ASTA D	Real time \overline{B} bus data \rightarrow A bus Real time \overline{B} bus data \rightarrow RGTR \overline{B}
B-to-A	L	L	L	X	Output	Input	RGTR	В	t	UC	Real time B bus data → A bus Real time B bus data → RGTR A
Operation	ĺ		L		0		скв сн	BUS	t	t	Real time B bus data → A bus Real time B bus data → RGTR A Real time B bus data → RGTR B
extransition	e Julia	ALL PROPERTY.	edere Eu	untinous B	provide the	ALC: TRACE		DEPENDENCE.	UC	UC	RGTR A data → A bus
Stored data					.0153	l-É pre tiu	A BUS RGTR		UC	, 1	RGTR A data → A bus RGTR A data → RGTR B
B-to-A	L	L	н	X	Output	Input	RGTR	B BUS	1 10	uc	Real time B bus data → RGTR A RGTR A data → A bus
Operation							СКВ С	KA	t	t	Real time B bus data → RGTR A RGTR A data → A bus RGTR A data → RGTR B
									UC	UC	Real time A bus data → B bus
Real time						1.54 384	A BUS RGTR A	1	UC	1	Real time A bus data → B bus Real time A bus data → RGTR B
A-to-B	170	Н	X	L	Input	Output		В	t	UC	Real time \overline{A} bus data \rightarrow B bus Real time \overline{A} bus data \rightarrow RGTR A
Operation					astuqrii ii astuqal ti		скв ски	BUS	T038	g ist	Real time \overline{A} bus data \rightarrow B bus Real time \overline{A} bus data \rightarrow RGTR \overline{A} Real time \overline{A} bus data \rightarrow RGTR \overline{A}
(3700)000	Same?	rino.	in the	paper) restern	letele J	PACE DESIGN	18		UC	UC	RGTR B data → B bus
Stored data			es XI		gbs ova	807 Pos	A BUS RGTR A	1	UC	eni, di	Real time A bus data → RGTR E RGTR B data → B bus
A-to-B	Н	н	X		Input	Output	RGTR B	В	\$1.0	UC	RGTR B data → B bus RGTR B data → RGTR A
Operation					.tela.	956	скв ск.	BUS A	t	t	Real time A bus data → RGTR E RGTR B data → B bus RGTR B data → RGTR A
									UC	UC	RGTR A/B data → A/B bus
Transfer							BUS RGTR		UC	t	RGTR Ā/B data → A/B bus RGTR Ā data → RGTR B
Stored	Н	L	н	н	Output	Output	RGTR		1	UC	RGTR A/B data — A/B bus RGTR B data — RGTR A
Data							СКВ	BUS	1	1	RGTR A/B data → A/B bus RGTR A data → RGTR B RGTR B data → RGTR A

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Bus Operation for 'LS652/654

OPERATION		CON	TROL		DAT	A I/O	DI OOK DIACDAM		OCK	ngotov tur
OPERATION	GAB	GBA	SRA	SRB	A0-A7	B0-B7	BLOCK DIAGRAM	СКА	СКВ	'LS652/654
								UC	UC	No operation
		8-00		YES	TLIGA		BUS RGTR	UC	1	Real time A bus data → RGTR B
Storage	L	Н	X	X	Input	Input	RGTR B B	1	UC	Real time B bus data → RGTR A
	d	615	8		8 8		СКВ СКА	1	1	Real time A bus data — RGTR B Real time B bus data — RGTR A
								UC	UC	Real time B bus data → A bus
Real time		9					A BUS RGTR A	UC	1	Real time B bus data — A bus Real time B bus data — RGTR B
B-to-A	L	L 6	L	Х	Output	Input	RGTR	1	UC	Real time B bus data - A bus Real time B bus data - RGTR A
Operation							в ви	t t	t	Real time B bus data - A bus Real time B bus data - RGTR A Real time B bus data - RGTR B
Am 31 -								UC	UC	RGTR A data → A bus
Stored data	Photo Photo		1,5		-		A BUS RGTR	UC	1	RGTR A data → A bus RGTR A data → RGTR B
B-to-A	L	L	Н	X	Output	Input	RGTR	g Date:	UC	Real time B bus data → RGTR A RGTR A data → A bus
Operation	E 100 1971	Arrod Irani	1 36	8 97 8 97	ATM F Marc Care		CKB CKA	1	t	Real time B bus data → RGTR A RGTR A data → A bus RGTR A data → RGTR B
		7 6	1					UC	UC	Real time A bus data → B bus
Real time			8.8			Ayrı	A BUS RGTR A	UC	1	Real time A bus data → B bus Real time A bus data → RGTR B
A-to-B	Н	Н	Х	L	Input	Output	RGTR	1	UC	Real time A bus data → B bus Real time A bus data → RGTR A
Operation			1.0				CKA CKA	t	S no /	Real time A bus data → B bus Real time A bus data → RGTR A Real time A bus data → RGTR B
	and a second						X Ald *	UC	UC	RGTR B data → B bus
Stored data	0E.0	7.5		-			A BUS RGTR A	UC	1	Real time A bus data → RGTR B RGTR B data → B bus
A-to-B	Н	Н	X	Н	Input	Output	RGTR B	1	UC	RGTR B data → B bus RGTR B data → RGTR A
Operation			00A 0S				CKB CKA	1	1.000	Real time A bus data → RGTR B RGTR B data → B bus RGTR B data → RGTR A
- AND - CAS-		0.5	150	-	139-		A744 - 90	UC	UC	RGTR A/B data → A/B bus
Transfer			1 GMI			18	BUS RGTR A	UC	1	RGTR A/B data → A/B bus RGTR A data → RGTR B
Stored	Н	L	Н	Н	Output	Output	RGTR	t	UC	RGTR A/B data → A/B bus RGTR B data → RGTR A
Data			i dai			es stiled	Виз	†	1	RGTR A/B data → A/B bus RGTR A data → RGTR B RGTR B data → RGTR A

Absolute Maximum Ratings

Supply voltage V _{CC}	0.5 V to 7 V
Input voltage	
Off-state output voltage	-0.5 V to 5.5 V
Storage temperature -65	°C to +150°C

Operating Conditions

SYMBOL	elsb aud el eme lene PARAM	IETER Management	MILITARY MIN TYP MA	COMMERCIA MIN TYP M	LIMIT
Vcc	Supply voltage	6363 BRO B	4.5 5 5.	5 4.75 5 5	.25 V
TA	Operating free air temperature		-55 12	5 0	75 °C
	Width of alack	High	20	20	ns
t _W Width of clock	- step and 8 smb lng 9	Low	20	20	ns
, sud A	- Fleat time 8 bus data	'LS651	20 t	20 t	1
^I su	Setup time	'LS652	20 †	20 t	ns
and A	Rea time 6 bus data	'LS651	0 †	0 1	
th	Hold time 1998	'LS652	0 †	01	ns
ГОН	High-level output current		-1	2	-15 mA
loL	Low-level output current		1	2	24 mA

¹ The arrow indicates the transition of the clock input used for reference. The for the low-to-high transitions. I for the high-to-low transitions.

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMET	TER	308	TEST	CONDITIONS		TYP	-	COMMERCIAL MIN TYP MAX			UNIT
VIL	Low-level input ve	oltage						0.7			0.8	V
VIH	High-level input v	oltage							2	-		V
VIC	Input clamp volta	ge ou	Vcc	= MIN	I _I = -18 mA			-1.5			-1.5	V
1 _{IL}	Low-level input c	urrent	Vcc	= MAX	V _I = 0.4 V			-0.4			-0.4	mA
Л _{ІН} ТОН	High-level input of	urrent	Vcc	= MAX	V _I = 2.7 V	Dign:		20	H	H	20	μΑ
Bud El	Maximum input	A or B	V 8	- MAY	V _I = 5.5 V			0.4	MIST		0.1	m A
Astan	current All other		V _{CC} = MAX		V _I = 7 V			0.1			0.1	mA
		asi au lai	V _{CC} = MIN V _{IL} = MAX V _{IH} = 2 V		I _{OL} = 12 mA		0.25	0.4		0.25	0.4	
VOL	Low-level output	voltage			I _{OL} = 24 mA					0.35	0.5	V
.,	eus 8 - Leith E R 1.	A L	V _{CC} = MIN V _{IL} = MAX V _{IH} = 2 V		I _{OH} = -3 mA	2.4	3.4		2.4	3.4	siel	V B-01-A
VOH	High-level output	voltage			IOH = MAX	2		X	2	H		
IOZL	- stab and A smit to		V _{CC} = MAX V _{IL} = MAX V _{IH} = 2 V		V _O = 0.4 V			-400			-400	μΑ
lozh	Off-state output of	urrent			V _O = 2.7 V			20		H	20	μΑ
los	Output short-circ	uit current*	V _{CC}	= MAX		-40		-225	-40		-225	mA
800	BOY - BIRD SYA ETS	ng .			Outputs High			145			145	
				'LS- 651	Outputs Low			165			165	
disd			V _{CC} =		Outputs disabled	humbur.	5 4	165		14	165	mA
Icc	Supply current		MAX		Outputs High			145	4		145	IIIA
£1/0	BYA - stab BYARTI		1	'LS- 652	Outputs Low			165			165	816
0				-	Outputs disabled			165			165	160

^{*} Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load/Waveforms)	'LS651 MIN MAX	'LS652 MIN MAX	UNIT
tPLH	0.30-1 (10), 2 (4), 4 (4)	m - mar - marada da a a mar		15 evulsio 15	ns
t _{PHL}	Data to output delay		15	20	ns
t _{PLH}	Olask ta sutant dalan		20	20	ns
tPHL	Clock to output delay		30	30	ns
tPLH	Select to output delay †	C - 45°5 D - 6670	35	35	ns
tPHL	(data input High)	$C_L = 45pF R_L = 667\Omega$	20	affey viggas 25	ns
t _{PLH}	Select to output delay †		35	ат тападо 35	ns
t _{PHL}	(data input Low)		30	20	ns
t _{PZL}	GBA to		25	25	ns
^t PZH	A bus output enable delay		20	20	ns
t _{PLZ}	GBA to	C - 5=5 D - 6670	25	25	ns
t _{PHZ}	A bus output disable delay	$C_L = 5pF$ $R_L = 667\Omega$	35	35	ns
tPZL	GAB to	C - 45-5 D - 6670	30	30	ns
t _{PZH}	B bus output enable delay	$C_L = 45pF R_L = 667\Omega$	and Al aperior 25	os leval rigin 25	ns
t _{PLZ}	GAB to	$C_L = 5pF R_L = 667\Omega$	sud (a) manua 25	to level apple 25	ns
tPHZ	B bus output disable delay	OL - SPF RL - 00/11	35	35	ns

[†] See Figure 4.

Switching Characteristics Over Operating Range

		TEST CONDITIONS	N	IIL	CC		
SYMBOL	PARAMETER	(See Test Load/Waveforms)	'LS651 MIN MAX	'LS652 MIN MAX	'LS651 MIN MAX	'LS652 MIN MAX	UNIT
t _{PLH}	Data to autout dalau		20	20	15	20	ns
^t PHL	Data to output delay	5 11	20	25	17	22	ns
t _{PLH}	Clock to output delay		25	25	22	22	ns
t _{PHL}			35	35	30	30	ns
tPLH	Select to output delay †	C - 45-5 D - 6670	40	40	35	35	ns
t _{PHL}	(data input High)	$C_L = 45pF$ $R_L = 667\Omega$	25	30	25	28	ns
^t PLH	Select to output delay †		40	40	35	35	ns
t _{PHL}	(data input Low)		35	25	30	22	ns
t _{PZL}	GBA to		30	30	25	25	ns
t _{PZH}	A bus output enable delay		25	25	20	20	ns
t _{PLZ}	GBA to	0 - 5-5 0 - 0070	35	30	30	28	ns
t _{PHZ}	A bus output disable delay	$C_L = 5pF$ $R_L = 667\Omega$	40	45	40	40	ns
t _{PZL}	GAB to	0 - 45-5 B - 0070	35	35	30	32	ns
t _{PZH}	B bus output enable delay	$C_L = 45pF R_L = 667\Omega$	30	30	25	25	ns
tPLZ	GAB to	0 - F-F D - 0070	35	35	30	30	ns
^t PHZ	B bus output disable delay	$C_L = 5pF$ $R_L = 667\Omega$	40	45	35	40	ns

[†] See Figure 4.

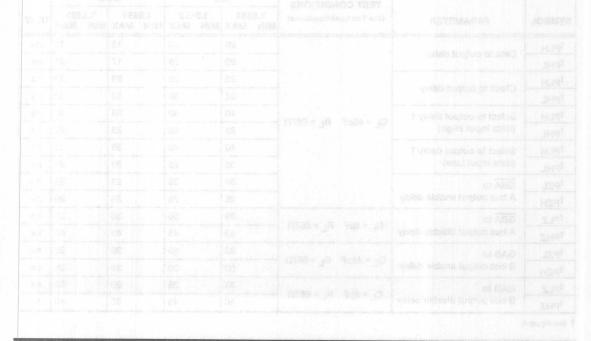
Absolute Maximum Ratings

Supply voltage VCC	0.5 V to 7 V
Input voltage	
Off-state output voltage	0.5 V to 5.5 V
Storage temperature	-65°C to +150°C

Operating Conditions

SYMBOL	39 P.	PARAMETER		COMMERCIAL MIN TYP MAX	UNIT	
VCC	Supply voltage		4.5 5 5.5	4.75 5 5.25	V	
TA	Operating free air temper	ature	-55 125	0 75	°C	
AC 109 1 100		High	20	20	"Disking	
^t w	Width of clock	Low	20	20	ns	
1 5	e 20	'LS653	20 1	20 1	-CAF	
^t su	Setup time	'LS654	20 †	20 1	ns	
- 0	11-110	'LS653	0 t Valido eldisat	01	SHA	
^t h	Hold time	'LS654	0 1	01	ns	
VOH	High-level output voltage	(A bus only)	5.5	5.5	V	
ГОН	High-level output current	(B bus only)	-12	-15	mA	
loL	Low-level output current		12	24	mA	

[↑] In he arrow indicates the transition of the clock input used for reference. ↑ for the low-to-high transitions, I for the high-to-low transitions.



Electrical Characteristics Over Operating Conditions as a 1.44 a

SYMBOL	PARAMET	ER		TEST CONDITIONS		MILIT MIN TY		COMMI MIN TY		UNIT	
VIL	Low-level input vo	oltage					0.7		0.8	V	
VIH	High-level input v	oltage				2	nadam a	2		V	
VIC	Input clamp volta	ge	Vcc -	MIN	I _I = -18 mA		-1.5		-1.5	V	
I _{IE} 08	Low-level input co	urrent	V _{CC}	MAX	V _I = 0.4 V	2000	-0.4	0.00	-0.4	mA	
hH 💮	High-level input of	urrent	VCC	MAX	V _I = 2.7 V	A face a	20		20	μΑ	
80 ns	Maximum input	A or B	V	= MAX	V _I = 5.5 V	10000	0.1		0.1	mA	
100	current	All others	vcc.	- IVIAA	V _I = 7 V		0.1		0.1	4191	
8D - 08	30	· altana	Vcc:	MIN	I _{OL} = 12 mA	0.	25 0.4	0.	25 0.4	piqf	
VOL	Low-level output	voitage	V _{IL} = MAX V _{IH} = 2 V		I _{OL} = 24 mA		fau	A 60 100.	35 0.5	V	
en de	High-level output	voltage	V _{CC} = MIN		I _{OH} = -3 mA	2.4 3.	4	2.4 3	4	1619)	
VOH	(B bus only)		VIL :	= MAX = 2 V	IOH = MAX	2	7 80 at areha	2	Maria I	V	
ГОН	High-level output (A bus only)	current	Vcc:	MIN MAX	V _{OH} = 5.5 V	(ripihi su)	100	ect to Ba god delay	100	μΑ	
IOZL	Off-state output cu	ırrent	V _{CC}	MAX	V _O = 0.4 V		-400	d il co tale	-400	μΑ	
lozh	(B bus only)	mont	VIL :	= MAX = 2 V	V _O = 2.7 V (B bus only)	777 23 30 4	20	and dust	20	μΑ	
los	Output short-circ (B bus only)	uit current*	V _{CC}	= MAX		-40	-225	-40	-225	mA	
					Outputs High	Un fuel	145	Licinio vill	145	1154	
			'LS- 653		Outputs Low		165		165	159	
80 80					Outputs disabled	velon	165	CT B	165	mA	
Icc	Supply current	V _{CC} =		Outputs High		145		145			
				'LS- 654	Outputs Low	a sepal(o.)-ne Black esta su	165	eser tiller tilse	165	FI 107	
					Outputs disabled		165		165	10 T 1008	

^{*} Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

Switching Characteristics V_{CC} = 5 V, T_A = 25°C Stored proteins and the state of the state of

SYMBOL	PARAMETER	TEST CONDIT		'LS653 MIN MAX	'LS654 MIN	MAX	UNIT
t _{PLH}	7.0			e (mil 25 u	Low-level inp	25	ns
t _{PHL}	Data to A bus output delay			apatio 20.	High-level in	25	ns
t _{PLH}	8.4-	Am 81- = 1	MIM = 100	/ en15	Input clamp v	15	ns
tPHL	Data to B bus output delay		XAM = pol	/ Insmu15	Low-level inp	20	ns
t _{PLH} 08	Olaska A kasa a tadaka		MAM = op	/ morro 30	High-level inp	30	ns
t _{PHL}	Clock to A bus output delay			8 to A 30	ani membalii	30	ns
^t PLH			X/M = po	arento IIA 20	inemus	20	ns
t _{PHL}	Clock to B bus output delay		CG = MIN	30		30	ns
t _{PLH}	Select to A bus †	Amas a rel	XAM* JA	45	No leval-woll	45	ns
^t PHL	output delay (data input High)	C _L = 45pF R _L	= 66/11	25		30	ns
^t PLH	Select to A bus †			40	(vino euri 8)	45	ns
tPHL	output delay (data input Low)		A.Z. HI,	30		25	ns
t _{PLH}	Select to B bus †		CO = MIN	, January 351	luo leval-rigiri	35	ns
t _{PHL}	output delay (data input High)			25	(A bits only)	25	ns
t _{PLH}	Select to B bus †		XAM = go	35		35	ns
t _{PHL}	output delay (data input Low)	V 7 S = 5V		30	(who sud 8)	20	ns
tPLH	GBA to		V 2= HI	35		35	ns
t _{PHL}	A bus output enable delay			25	treds tuging	30	ns
tPZL	GAB to			30	Then here at	30	ns
^t PZH	B bus output enable delay	THE THE PROPERTY.	12 July 1	25		25	ns
t _{PLZ}	GAB to	C - 50E B	- 6670	25		25	ns
t _{PHZ}	B bus output disable delay	C _L = 5pF R _L	- 00/11	35	Supply ours	35	ns

^{*} For A bus, the test load will refer to the open-collector test load. See Figure 6.
For B bus, the test load will refer to the three-state test load. See Figure 7.

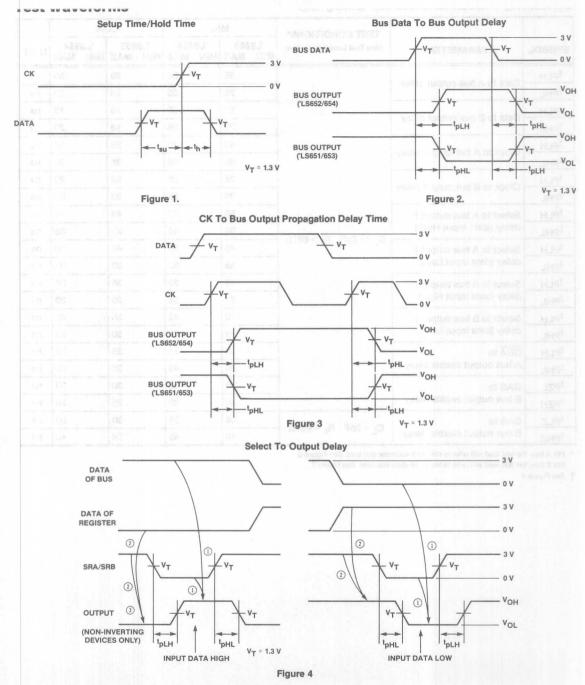
† See Figure 4.

Switching Characteristics Over Operating Range

	Dela Torbus Curpii Delav	TEST CONDITIONS*	TIONS* MIL		CC	MC	
SYMBOL PARAMETER	(See Test Load/Waveforms)	'LS653 MIN MAX	'LS654 MIN MAX	'LS653 MIN MAX	'LS654 MIN MAX	UNIT	
t _{PLH}			30	30	28	30	ns
t _{PHL}	Data to A bus output delay	YURBUD BUB	25	30	23	28	ns
tPLH		(658/55963)	20	20	18	18	ns
t _{PHL}	Data to B bus output delay		20	25	18	20	ns
tPLH	Clask to A bus a task to dalar	70/1750/300	40	40	35	35	ns
t _{PHL}	Clock to A bus output delay	100000000000000000000000000000000000000	40	40	35	35	ns
tPLH	Olask to D bus a to talk		25	25	23	23	ns
t _{PHL}	Clock to B bus output delay		35	35	30	30	ns
t _{PLH}	Select to A bus output †	Propagation Delay 11 as	50	50	45	48	ns
tPHL	delay (data input High)		30	40	25	35	ns
t _{PLH}	Select to A bus output †	$C_L = 45pF$ $R_L = 667\Omega$	45	55	43	50	ns
tPHL	delay (data input Low)	e and the second	35	30	30	28	ns
t _{PLH}	Select to B bus output †		40	35	35	35	ns
t _{PHL}	delay (data input High)	7	25	35	25	30	ns
t _{PLH}	Select to B bus output †		40	45	35	40	ns
^t PHL	delay (data input Low)	. 7	35	25	30	23	ns
t _{PLH}	GBA to		40	35	35	35	ns
t _{PHL}	A bus output enable delay		30	40	28	35	ns
^t PZL	GAB to		35	35	30	33	ns
^t PZH	B bus output enable delay		30	30	25	28	ns
t _{PLZ}	GAB to	$C_1 = 5pF R_1 = 667\Omega$	35	35	30	30	ns
^t PHZ	B bus output disable delay	OL - 3011	40	45	38	40	ns

^{*} For A bus, the test load will refer to the open-collector test load. See Figure 6.
For B bus, the test load will refer to the three-state test load. See Figure 7.

[†] See Figure 4.



- NOTES: 1. When SRA/SRB is low, the input data will transfer to output bus.
 - 2. When SRA/SRB is high, the data of register will transfer to output bus.
 - 3. For the inverting devices, the timing is similar, but the output is opposite to that for the non-inverting devices.

Enable/Disable Delay

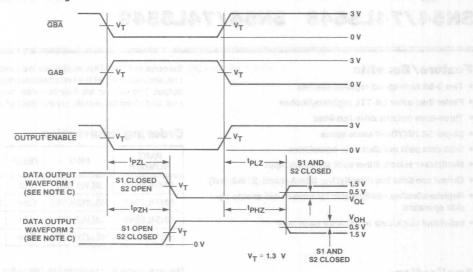
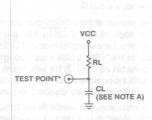
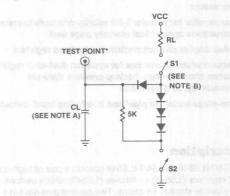


Figure 5

Test Loads



Load Circuit For Open-Collector Outputs



Load Circuit For Three-State Outputs

- * The "TEST POINT" is driven by the output under test, and observed by instrumentation.
- Notes: A. C₁ includes probe and jig capacitance.
 - B. All diodes are 1N916 or 1N3064.
 - C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

 Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - D. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
 - E. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz. Z_{OUT} = 50 Ω and $\,t_{R}$ = 15 ns t_{F} \leq 6 ns.
 - F. When measuring propagation delay times of three-state outputs, switches S1 and S2 are closed.

8-Bit Two-Stage Pipelined Register/Latch

SN54/74LS548 SN54/74LS549

Feature/Benefits

- Two 8-bit high-speed registers/latches
- · Faster than other LS-TTL registers/latches
- Three-state outputs drive bus lines
- 24-pin SKINNYDIP® saves space
- · 8-bit data path matches byte boundaries
- · Multiplexer selects either rank at input/output
- Output can drive bus directly: IOL 32 mA (com), 24 mA (mil)
- · Registers/latches configurable for nose-to-tail or side-byside operation
- · Individual clock/gate enables for each rank

the outputs Y7-Y0. This multiplexer is controlled by the OUTSEL line, and allows either the first or second register/latch data to be output. The outputs are fully buffered, provide high-drive current, and allow three-state control through the OE line.

Ordering Information

PART NUMBER	PKG	TEMP	TYPE	POWER
SN54LS548	JS,W,L(28)	Mil	Register	LS
SN74LS548	NS,JS,NL(28)	Com	Register	LS
SN54LS549	JS,W,L(28)	Mil	Latch	LS
SN74LS549	NS,JS,NL(28)	Com	Latch	LS

Applications

- · Registers for pipelined arithmetic units or digital signal processors
- Bus monitor for popular 8-bit microprocessors to restart instructions upon virtual memory page fault
- Video display character/attribute pipelined registers
- Sequence/state generator for systems: dual-rank registers/ latches allow storing a backup previous state for redundancy, or diagnostics
- Two-stage buffer for pipelined interfacing input/output

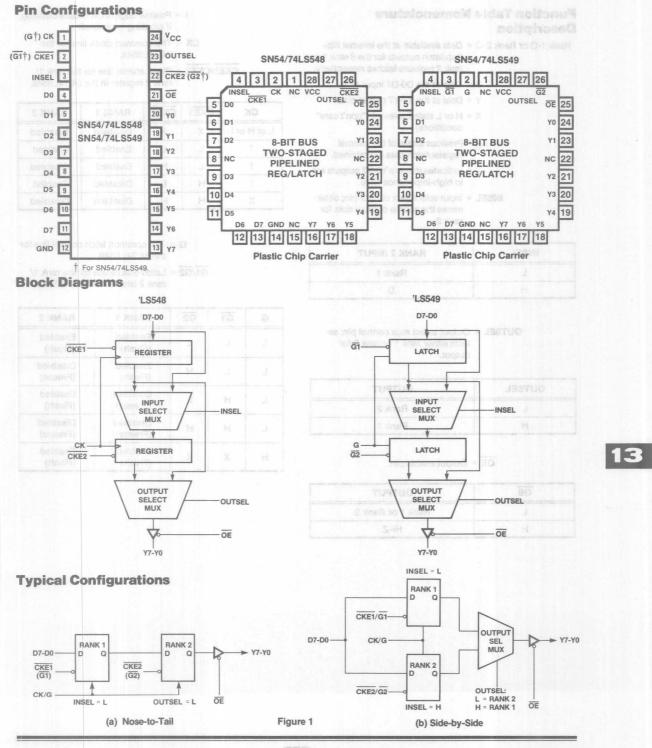
Description

The 54/74LS548 and 54/74LS549 contain a pair of high-speed 8-bit registers ('LS548) or latches ('LS549) which perform various pipeline storage functions. Two control pins govern a pair of internal multiplexers, as shown in the block diagrams; using these, several useful data paths can be configured. The input selection multiplexer determines the source of data to the second register/latch, as controlled by the INSEL line. In this way, data from either the D7-D0 inputs, or the outputs of the first register/ latch, are stored in the second register/latch. The output selection multiplexer determines the source of data that will be sent to

The arrangement of registers/latches within the 'LS548/'LS549 can be thought of a two 8-bit storage ranks, rank 1 and rank 2. The 'LS548 has a common clock line CK, and separate clock enables CKE1 and CKE2 for rank 1 and rank 2 respectively. In contrast, the 'LS549 operates as a flow-through latch, and has separate latch enables $\overline{G1}$ and $\overline{G2}$ for each rank, as well as a common latch-enable input G.

In the 'LS548, data present at the D7-D0 inputs are stored in rank 1 on the positive edge of CK, if CKE1 has been previously asserted. Data for rank 2 are stored similarly, if CKE2 is asserted prior to the clock. In the 'LS549, data pass through the latches when the latch controls (G1 or G2) for either rank are enabled simultaneously with the common latch enable G. Data remain in a rank when the latch controls are disabled, or 'unasserted'.

The clock/gate control lines are used with the INSEL and OUT-SEL controls for flexible data storage and movement operations. Two representative examples are shown in Figure 1 (a) and 1 (b). The first example is a classical 2-stage pipelined register, or 'nose-to-tail' configuration. Data at D7-D0 are first stored in rank 1, then stored in rank 2 on the next clock/gate. If the clock/gate enable for either rank becomes unasserted, then the previouslystored data are simply retained. In the second example, data at D7-D0 are stored in either or both ranks if the respective clock/gate enable signals are asserted. In this 'side-by-side' configuration, data sent to the Y7-Y0 outputs are selected from either rank 1 or rank 2, under control of the OUTSEL line.



Function Table Nomenciature Description

Flank 1-Q or Rank 2-Q = Data available at the internal flipflop/latch outputs for the 8 rank 1 or rank 2 registers/latches respectively.

D = Data at the D0-D7 input pins.

Y = Data at the Y0-Y7 output pins.

X = H or L state irrelevant ("don't care" conditions)

Q₀ = Previous states of the internal register/latch data are retained.

Z = Indicates that the Y0-Y7 outputs are in high-impedance state.

INSEL = Input select mux control pin; determines the source of input data for rank 2.

INSEL	RANK 2 INPUT
L	Rank 1
Н	D

OUTSEL = Output select mux control pin; selects either rank 1 or rank 2 for output.

OUTSEL	OUTPUT
L see	Rank 2
Н	Rank 1

OE = Output enable pin.

ŌĒ	OUTPUT
L	Rank 1 or Rank 2
Н ===	Hi-Z

if clocking is enabled.

CK = The common clock line for the 54/74LS548.

CKE1/CKE2 = Clock enable line for the rank 1/ rank 2 register in the 54/74LS548.

СК	CKE1	CKE2	RANK 1	RANK 2
L or H or l	X	X	Disabled	Disabled
arr 1	L	s.L	Enabled	Enabled
1	L	Н	Enabled	Disabled
1	Н	L	Disabled	Enabled
X	Н	н	Disabled	Disabled

G = The common latch control line for the 54/74LS549.

G1/G2 = Latch enable line for the rank 1/ rank 2 latch in the 54/74LS549.

G	G1	G2	RANK 1	RANK 2
L	L	L	Enabled (Flush)	Enabled (Flush)
L	L	н	Enabled (Flush)	Disabled (Freeze)
L	Н	L	Disabled (Freeze)	Enabled (Flush)
L	Н	н	Disabled (Freeze)	Disabled (Freeze)
Н	X	х	Enabled (Flush)	Enabled (Flush)

'LS548 Function Table

СК	CKE1	RANK 1	CKE2	INSEL	RANK 2
L or H	Х	Q0	х	X	Q0
1	Н	Q0	Н	X	Q0
1	L	D	Н	X	Q0
1	L	D	L	L	Rank 1-Q
1	L	D	L	Н	D
1	Н	Q0	D Les	L-	Rank 1-Q
1	Н	Q0	L	Н	D

'LS549 Function Table

G	G1	RANK 1	G2	INSEL	RANK 2
L	L	D	L	L	Rank 1-Q
L	L	D	L	Н	D
L	L	D	Н	X	Q0
L	Н	Q0	L	L	Rank 1-Q
L	Н	Q0	L	Н	D
L	Н	Q0	Н	Х	Q0
Н	X	D	X	L	Rank 1-Q
Н	X	D	X	Н	D

'LS548/549 Output Function Table

OUTSEL	OE	Y
L	L	Rank 2-Q
Н	L	Rank 1-Q
Х	Н	Hi-Z

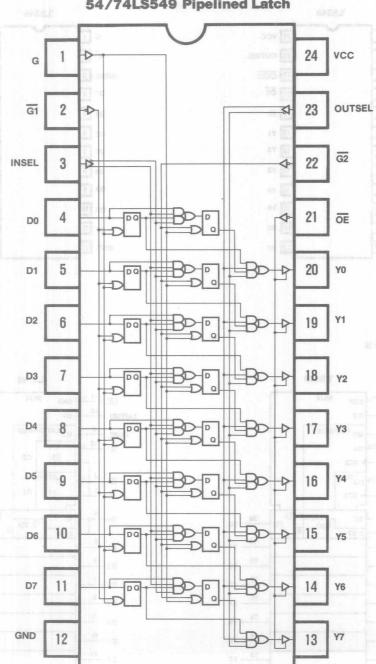
Logic Diagram 54/74LS548 Pipelined Register 24 VCC CK 2 CKE1 23 OUTSEL CKE2 INSEL 3 12 21 D0 OE 20 D1 5 Y0 19 D2 D3 8 D4 D5 9 16 Y4 10 15 Y5 D6 D7 **Y6**

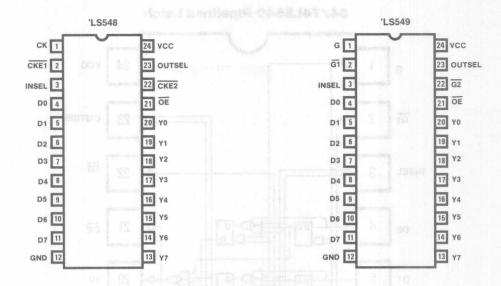
Y7

GND

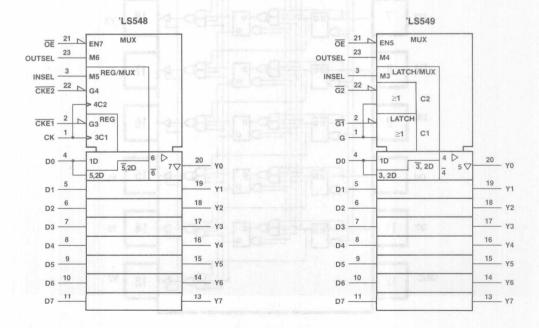
Logic Diagram

54/74LS549 Pipelined Latch





IEEE Symbols



Absolute Maximum Ratings

Supply voltage V _{CC}	0.5 V to 7 V
Input voltage	
Off-state output voltage	
Storage temperature	65°C to +150°C

Operating Conditions

SYMBOL	т. О ру	RAMETE	R V 3.8 = 1V	Visit = 30\	MIN	TYP	MAX	COMMERCIAL MIN TYP MAX			UNIT
V _C C	Supply voltage		Am 28 = 101	MiM = gg	4.5 5 5.5		4.75 5 5.25		V		
TA	Operating free-air temper	ature	Aro as a set	XAM = 147	-55		125	0	E-1-MID.	75	°C
		Llink	'LS548	CK	15			11			
N.	W W COV O O O	High	'LS549	G	15			luo lays			ns
tw	Width of CK, G, G1, G2		'LS548	CK	15			11			
00		Low	'LS548	<u>G</u> 1, <u>G</u> 2	18			16			ns
Au OS	The state of the s		'LS548	CK	201	108	MIN CERTE	151	assent.	2	real .
t _{su}	Setup time for Data			G	10↓			61			ns
Am 05			'LS549	G1, G2	171		41		SO		
Am -	001		'LS548	CK	Of		te	Ot	daguil		ool
th	Hold time for Data		CPUCD 1	G	12↓			101	40.1510/9800		ns
		LS549		<u>G1</u> , <u>G2</u>	51	als be	nod- ed-	5 5 5 10 0 20 800 0 0 0 0		0101011	
t _{su-CKEX}	Setup time for clock enab	Setup time for clock enables CKE1, CKE2 ('LS548 only)						101	M		ns
th-CKEX	Hold time for clock enable	e CKE1, C	KE2, ('LS548 on	ly)	81			51			ns
t _{su-INSEL}	Setup time for INSEL ¹							25			ns
th-INSEL	Hold time for INSEL ²				0			0			ns

NOTES: 1. This is the minimum setup time needed for INSEL prior to the rising edge of the clock/GX, and to the falling edge of the G, to ensure data transfer to rank 2.

^{2.} This is the minimum hold time needed for INSEL after the rising edge of the clock/ \overline{GX} , and to the falling edge of the G, to ensure data transfer to rank 2.

the arrow indicates the transition of the clock/gate input used for reference:

for the low-to-high transitions,

for the high-to-low transitions.

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER TEST CONDITIONS Low-level input voltage			LITARY TYP MAX	COMMER MIN TYP		UNIT		
VIL			Low-level input voltage		0.8		8.0 = 1 = 0.8		V
V _{IH}	High-level input voltage			1911743444 A. C.	2.0		2.0	INCHES.	V
VIC	Input clamp volta	age	V _{CC} = MIN	I _I = -18 mA		-1.5		-1.5	V
	Law lavel input a		V _{CC} = MAX	D or Y		-250		-250	
IIL	Low-level input of	urrent	V _{CC} = MAX V _I = 0.4 V	All others		-400		-400	μΑ
I _{IH}	High-level input	current	V _{CC} = MAX	V _I = 2.7 V		20	Condit	20	μΑ
Elju Ja	Maximum input current	D or Y All others	V _{CC} = MIN	V ₁ = 5.5 V V ₁ = 7 V	SMARA	0.1		0.1	mA
V Ag	Low-level output		V _{CC} = MIN V _{IL} = MAX	I _{OL} = 32 mA	31		0.35 0.5		V
VOL	Low-level output	voltage	V _{IH} = 2V	I _{OL} = 24 mA	enne	0.5	Operating In		A
Vall	High-level output voltage		V _{CC} = MIN V _{IL} = MAX	I _{OH} = -1 mA	2.4	3.4			V
VOH	High-level output	voltage	V _{IH} = 2V	I _{OH} = -2.6 mA		3.6 62	2.4 3.1		V
lozL	81		V _{CC} = MAX	V _O = 0.4 V	80.1	-20		-20	
lozh	Off-State output of	current	V _{IL} = MAX V _{IH} = 2V	V _O = 2.7 V		20		20	μА
los	Output short-circ	uit current*	V _{CC} = MAX	1,8549	-30	-130	-30	-130	mA
	Supply Comment		V _{CC} = MAX	'LS548		150		150	
lcc	Supply Current	Supply Current		'LS549		160	of made brate	160	mA

^{*} Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

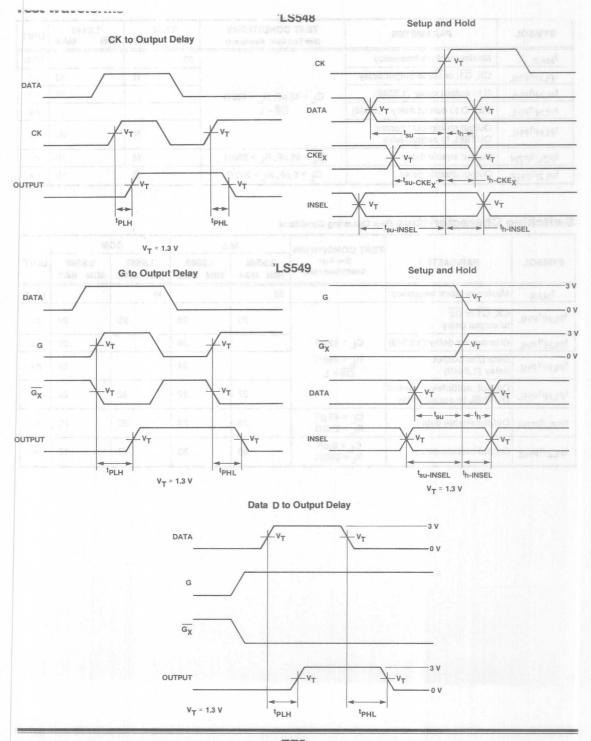


Switching Characteristics V_{CC} = 5 V, T_A = 25°C

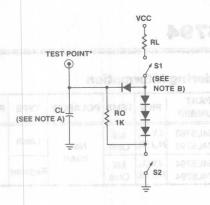
SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load/Waveforms) 'LS548 MIN MAX		'LS549 MIN MAX	UNIT
f _{MAX}	Maximum clock frequency	360	50		MHz
t _{PLH} /t _{PHL}	CK, G1, or G2 to output delay		18	22	ns
t _{PLH} /t _{PHL}	G to output delay ('LS549)	$C_{I} = 45 pF, R_{I} = 280 \Omega$	and .	23	ns
t _{PLH} /t _{PHL}	Data D to output delay ('LS549)	OE = L		16	ns
t _{PLH} /t _{PHL}	Output multiplexer control OUTSEL to output delay		20	20	ns
t _{PZL} /t _{PZH}	Output enable delay	$C_L = 45 pF, R_L = 280 \Omega$	18	18	ns
t _{PLZ} /t _{PHZ}	Output disable delay	C _L = 5 pF, R _L = 280 Ω	15	15	ns

Switching Characteristics Over Operating Conditions

SYMBOL		TEST CONDITIONS (See Test Load/Waveforms)	N	IIL y	CC		
	PARAMETER		LS548 MIN MAX	'LS549 MIN MAX	'LS548 MIN MAX	'LS549 MIN MAX	UNIT
fMAX	Maximum clock frequency	Ð	33		45		MHz
^t PLH ^{/t} PHL	CK, G1 or G2 to output delay		25	26	20	24	ns
t _{PLH} /t _{PHL}	G to output delay ('LS549)	C _L = 45 pF R _L = 280 Ω OE = L		28	1	25	ns
t _{PLH} /t _{PHL}	Data D to output delay ('LS549)			24		18	ns
^t PLH ^{/t} PHL	Output multiplexer control OUTSEL to output delay	ATAIL	27	27	22	22	ns
^t PZL ^{/t} PZH	Output enable delay	C _L = 45 pF R _L = 280 Ω	23	23	20	20	ns
t _{PLZ} /t _{PHZ}	Output disable delay	C _L = 5 pF R _I = 280 Ω	20	20	17	17	ns



Standard Test Load



OUTPUT ENABLE (Low-level enabling) S1 and -tp71 -> S2 closed WAVEFORM 1 S1 closed - 1.5 V - 0.5 V (SEE NOTE C) S2 open VOL -tpzH-> WAVEFORM 2 S1 open (SEE NOTE C) S2 closed V_T = 1.3 V

Load Circuit for Three-state Outputs

'LS548/549 Enable and Disable

* The "TEST POINT" is driven by the output under test, and observed by instrumentation.

Notes: A. C_L includes probe and jig capacitance.

- B. All diodes are 1N916 or 1N3064.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

 Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - D. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
 - E. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz. Z_{OUT} = 50 Ω and t_{R} = 15 ns $t_{F} \leq$ 6 ns.
 - F. When measuring propagation delay times of three-state outputs, switches S1 and S2 are closed.

8-Bit Latch/Register with Readback

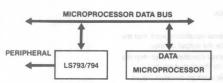
SN54/74LS793 SN54/74LS794

Features/Benefits

- . I/O port configuration enables output data back onto input bus
- · 8-bit data path matches byte boundaries
- Ideal for microprocessor interface

Description

These 8-bit latches/registers are useful for I/O operations on a microprocessor bus. An image of the output data can be read back by the CPU. This operation is important in control algorithms which make decisions based on the previous status of output controls. Rather than storing a redundant copy of the output data in memory, simply reading the register as an I/O port allows the data to be retrieved from where it has been stored in an 'LS793/4, for verification and/or updating.



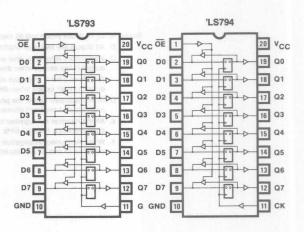
The data is loaded in the registers on the low-to-high transition of the clock (CK), for the 'LS794. The data is passed through the 'LS793 when the gate, (G), is High, and it is "latched" when G changes to Low. The output enable, OE is used to enable data on D7-D0. When OE is low the output of the latches/registers is enabled on D0-D7, enabling D as an output bus so that the host can perform a read operation. When OE is High, D7-D0 are inputs to the latches/registers configuring D as an input bus.

The output drive of these commercial parts for any output pin is IOL = 24 mA.

Ordering Information

PART NUMBER	PKG	TEMP	POLARITY	TYPE	POWER	
SN54LS793 SN74LS793	J,W,L, N,J,NL	Mil Com	Non-	Latch	LS	
SN54LS794 SN74LS794	J,W,L, N,J,NL	Mil Com	invert	Register	LO	

Logic Symbols



'LS793 Function Table

G	ŌĒ	Q	D
L	L	Q ₀ **	Output, Q
L	Н	Q ₀ **	Input
H [†]	L	D*	Output, Q*
Н	Н	D	Input

^{*} In this case the output of the latch feeds the input, and a "race" condition results

LS794 Function Table

СК	ŌĒ	Q	D
LorHor↓	L	Qn	Output, Q
LorHorl	Н	Q ₀	Input
1	L	Qn	Output, Q'
1	Н	D	Input

^{*} In this case the output of the register is clocked to the inputs and the overall Q output is unchanged at Q₀.

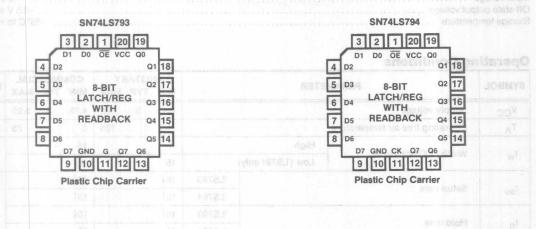
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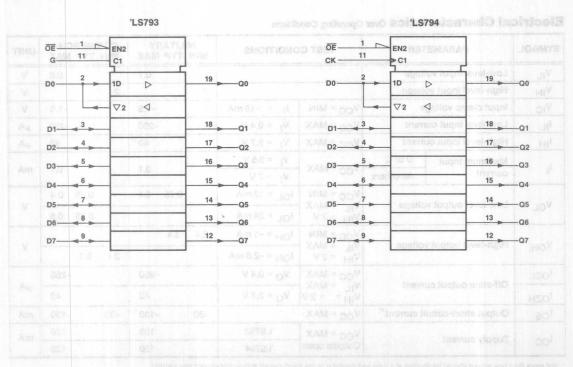
^{*} Qo represents the previous "latched" state.

[†] This transition is not a normal mode of operation and may produce hazards

Pin Configurations



IEEE Symbols



Supply voltage V _{CC}	0.5 V to 7 V
Input voltage	1.5 V to 7 V
Off-state output voltage	0.5 V to 5.5 V
Storage temperature	-65°C to +150°C

Operating Conditions

SYMBOL	PARAMETER				TYP	RY MAX	COM	/MER	CIAL	UNIT
Vcc	Supply voltage		4.5	5	5.5	4.75	5	5.25	V	
TA	Operating free air temperature	re				125	0	CALL STATE	75	°C
	W. W. 2001 J. 100 J. 100 V.	High		15		15			ns	
t _w	w Width of Clock/Gate	Low ('LS794	only)	15			15			113
	Plactic Chip Carrier		'LS793	15↓	Yelva	e O glett	10↓			3
tsu	Setup time		'LS794	151		151				
	t _h Hold time		'LS793	10↓			10↓			ns
^t h			'LS794	of			of			

The arrow indicates the transition of the clock/gate input used for reference. for the low-to-high transitions, for the high-to-low transitions.

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAME	TER	TEST C	ONDITIONS	MILITARY MIN TYP MAX		COMMER MIN TYP		UNIT	
V _{IL}	Low-level input vo	Itage			161	0.7		0.8	V	
VIH	High-level input vo	oltage			2		2		V	
VIC	Input clamp voltag	je	V _{CC} = MIN	I _I = -18 mA		-1.5	\$77	-1.5	V	
IL 10-	Low-level input cu	irrent	V _{CC} = MAX	V ₁ = 0.4 V	81,	-250	3,0	-250	μΑ	
IH so-	High-level input co	urrent	V _{CC} = MAX	V _I = 2.7 V	TE.	40	1	40	μΑ	
	Maximum input	D or Q	V - MAY	V _I = 5.5 V	25	0.1	0.1		mA	
h som	current	All others	V _{CC} = MAX	V ₁ = 7 V	22	0.1	-	MA		
L			V _{CC} = MIN	I _{OL} = 12 mA	167	0.25 0.4	0.25	0.4		
VOL	Low-level output voltage		$V_{IL} = MAX$ $V_{IH} = 2 V$	I _{OL} = 24 mA	i er		0.35	0.5	V	
., 30-			V _{CC} = MIN	I _{OH} = -1 mA	2.4	3.4		70		
VOH	High-level output	voltage	V _{IL} = MAX V _{IH} = 2 V	I _{OH} = -2.6 mA		Laurence de la company	2.4 3.1		V	
lozL			V _{CC} = MAX	V _O = 0.4 V		-250	-250			
lozh	Off-state output current		V _{IL} = MAX V _{IH} = = 2 V	V _O = 2.7 V		40	40		μΑ	
los	Output short-circu	uit current*	V _{CC} = MAX		-30	-130	-30	-130	mA	
	Completerment		V _{CC} = MAX	'LS793		120		120	mA	
ICC	Supply current		Outputs open	'LS794		120	120			

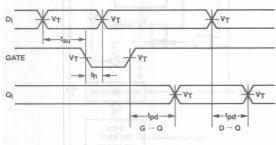
^{*} Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second

Switching Characteristics V_{CC} = 5V, T_A = 25°C

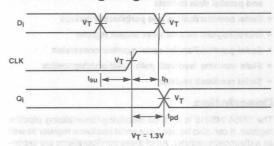
SYMBOL	PARAMETER	TEST CONDITIONS (See Interface Test Load/Waveforms)		S793	MAX	'LS79	4 MAX	UNIT
fMAX	Maximum clock frequency	and the contract of the first section of the sectio	produces and	W 2017	2 - 2 2 5 1 10	35 50	Surf & UTG	MHz
^t PLH	Data to output delay	d galtelatü		12	18	ditens8	Lasti	ns
t _{PHL}	Data to output delay	C = 45pE D = 200 ()	(proje	12	18	agi validaq	an eviti	ns
t _{PLH}	Clock/gate to output delay	C _L = 45pF R _L = 280 Ω		17	25	C3mA et 9 n	20	ns
^t PHL	Clock/gate to output delay	1186A6M8	1014250	12	25	14	20	ns
t _{PZL}	Output enable delay [†]	(1.00 PC PC PC) PARTICIPATION CONTRACTOR	elenin	15	20	15	20	ns
t _{PZH}	Output enable delay			11	20	11	20	ns
t _{PLZ}	Output disable delay [†]			8	20	8	20	ns
t _{PHZ}	Output disable delay	C _L = 5pF R _L = 280 Ω		9	20	9	20	ns

[†] For the 'LS793, G should remain LOW during these tests.

'LS793 Timing Diagrams



'LS794 Timing Diagrams



The case when gate is HIGH and data flows through the part is specified as Data to Output delay in the Switching Characteristics table. (V_T = 1.3V).

OUTPUT

ENABLE (Low-level

enabling)

WAVEFORM 1

(See Note A)

WAVEFORM 2

(See Note A)

Test Loads

FOR D OUTPUTS-ENABLE AND DISABLE TEST POINT FOR DI* R2 280 \(\Omega \) 5V \(\cdot \omega \) \$\frac{1}{2} \(\text{lk} \(\Omega \) \$\frac{1} \(\text{lk} \\ \Omega \) \$\frac{1}{2} \(\text{lk} \\ \Omeg

FOR Q OUTPUTS

TEST POINT FOR QI*

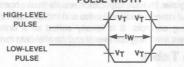
RL = 280 \(\Omega \)

45pF \(\omega \)

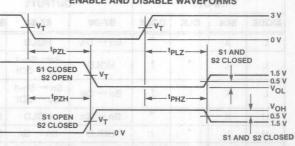
1k\(\Omega \)

The "TEST POINT" is drived by the output under test, and observed by instrumentation.

PULSE WIDTH



ENABLE AND DISABLE WAVEFORMS



For the 'LS793, the latch control "G" should be low while testing the enable and disable times, so that the output (Q) does not change. ($V_T = 1.3V$).

NOTES: A. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

8-Bit SERDE 18 JAT A SM SN 54/74S818 **Pipeline Register**

Features/Benefits

- High drive capability. IOL = 32 mA (Com)
- Alternate source to Am29818
- · Serial-parallel/Parallel-serial pipeline register
- · Independent pathing and clocking controls
- Expandable in multiples of 8 bits
- Three-state outputs
- PNP inputs for low-inputcurrent
- 24-pin SKINNYDIP® saves space

Applications

- Universal interface element for systems using both serial and parallel data formats
- Serial communication and peripheral interface
- Microprogram control store output register
- Serial-parallel/Parallel-serial pipeline conversion
- State machine feedback path isolation/diagnostics
- Serial readback register

Description

The SN54/74S818 is an 8-bit serializing/deserializing pipeline register. It can also be used as a serial readback register as well as a diagnostic register. All of these configurations are expandable in multiples of eight bits.

The 54/74S818 internally consists of a universal shift register and an 8-bit register. Its wide application results from a combination of powerful interconnection modes and independent clocking and pathing controls. It is ideally suited as a universal interface element involving both serial and parallel data formats.

Function Table

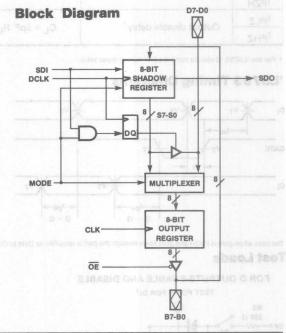
	INPUTS				OUTPUTS	JTS OPERATION			
MODE	SDI	CLK	DCLK	B7-B0	S7-S0	SDO	OPERATION THE PROPERTY OF THE	FIG.	
F0	X	1	*	Bn ← Dn	HOLD	S7	Load output register from input bus	1	
L	X	*	t	HOLD	Sn← Sn-1 S0← SDI	S7	Shift shadow register data	2	
L	X	1	t	Bn← Dn	Sn ← Sn-1 S0 ← SDI	S7	Load output register from input bus while shifting shadow register data		
Н	X	1	*	Bn ← Sn	HOLD	SDI	Load output register from shadow register	2,3,4	
H	L.	*	1	HOLD	Sn ← Bn	SDI	Load shadow register from output bus	3	
His	der Lot s	d bitrort	a Tons	Bn ← Sn	Sn ← Bn	SDI	Swap shadow register and output register		
Н	Н	*	1000	HOLD	HOLD	SDI	Enable D7-D0 as outputs for RAM write-back	4	

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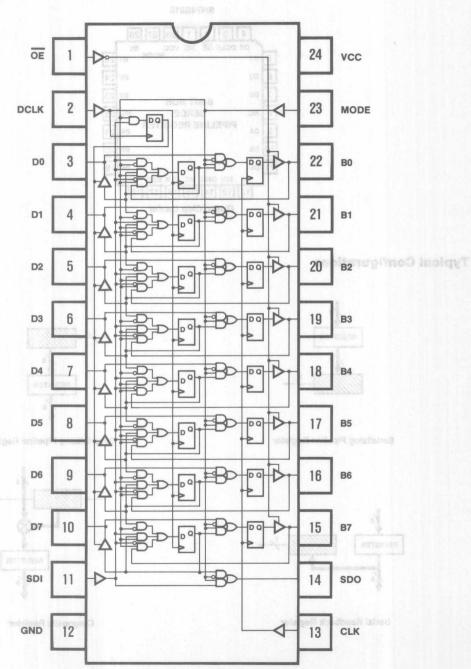
Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
SN74S818	NS, JS, NL (28)	Com
SN54S818	JS, W, L (28)	Mil





Logic Diagram

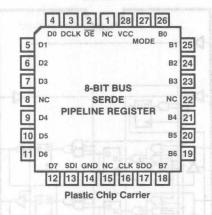


13

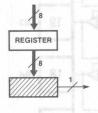
Pln Configuration

Pin Configuration

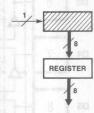
SN74S818



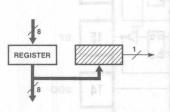
Typical Configurations



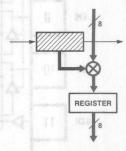
Serializing Pipeline Register



Deserializing Pipeline Register



Serial Readback Register



Diagnostic Register

Absolute Maximum Ratings

Supply voltage V _{CC}	0.5 V to 7 V
Input voltage	1.5 V to 7 V
Off-state output voltage	
Storage temperature	-65°C to +150°C

Operating Conditions

OVERDOL		PARAMETER	Vi- 5.5.V		1	VILITAF	RY	CC	MMERC	CIAL	UNIT
SYMBOL		PARAMETER	W.V = 37	XAN	MIN	TYP	MAX	MIN	TYP	MAX	Oldii
VCC	Supply voltage		Act 92 = 1.01		4.5	5	5.5	4.75	5	5.25	V
TA	Operating free air	temperature	An to sal	L MIN	-55	06	125	0		75	°C
V 30	Width of CLK	High	Am 8 = sol	XA	15		10	12	ek rogitik		ns
t _w	Width of CLK Low		Am A. c. upl	1	15	00	-VG	13			ns
twd	Width of DCLK High			Link	25	1752	730	20			ns
	Width of DCLK	Low 25 20	ne'-dpil	4	ns						
tsuc	Setup time from M	Setup time from MODE to CLK			20 f	90	-70	17 1	Sy Heighton		ns
thc	Hold time from CL	K to MODE	V 6.0 = 0V	16.e.h	01			01	ers alt(ns
tsud	Setup time from da	ata to CLK	V4.5 = 0V	y.	21 1			141	io Lingitus		ns
thd	Hold time from CL	K to data		20,636	01	*Ins	mus floo	01	iz ti infut		ns
t _{sudc}	Setup time from SI	DI, MODE to DCL	-K	XAN	31 1			20 t	o vlogui		ns
thdc	Hold time from DCLK to SDI, MODE		anti-to	01	District of	ter periode	01	is the colonial state.	an regel or	ns	
tsudq	Setup time from ou	utput to DCLK		1	25 †			181			ns
thdq	Hold time from DL	CK to output			01			0 1			ns

^{1.4} The arrow indicates the transition of the clock/gate input used for reference: 1 for the low-to-high transitions. 4 for the high-to-low transitions.

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAME	TER	TEST CONDITIONS		MILITARY MIN TYP MAX	COMMERCIAL MIN TYP MAX	UNIT	
V _{IL} of O	Low-level input v	oltage	1.175771753.4.0		0.8	autheq0.8	V	
VIH	High-level input	voltage			2	2	V	
VIC	Input clamp volta	age	V _{CC} = MIN I _I = -18 mA		-1.2	-1.2	V	
I _{IL}	Low-level input of	current	V _{CC} = MAX	V _I = 0.5 V	-0.25	-0.25	mA	
JH	High-level input	current	V _{CC} = MAX	V _I = 2.7 V	50	50	μΑ	
Y15611	Maximum input	DorB	M I	V _I = 5.5 V	gg-yawa da o	1	DRAWS	
η ×A	current	others	V _{CC} = MAX	V ₁ = 7 V	parameter 1	i	mA	
A GZT	4.17	0.6	6.0	I _{OL} = 32 mA	- 50	0.5	30k	
00 01	Low-level	B7-B0	V _{CC} = MIN V _{IL} = MAX	V _{IL} = MAX	I _{OL} = 24 mA	0.5	il Eurinisalo	AT
VOL	output voltage	SDO			V _{IL} = MAX V _{IH} = 2 V	I _{OL} = 8 mA	mp:H	10 10 HISTO 0.5
En		D7-D0	AIH - 5 A	I _{OL} = 4 mA	0.5			
80	High-level	B7-B0	V _{CC} = MIN	I _{OH} = 6.5 mA		OG to ritblild	tavu ²	
VOH	output voltage	SDO D7-D0	V _{IL} = MAX V _{IH} = 2 V	I _{OH} = -2 mA	2.4 W0 3	2.4	V	
OZL	Off-state		V _{CC} = MAX	V _O = 0.5 V	300Mat -250	ni amii bioH -250	μΑ	
lozh	output current		V _{IL} = MAX V _{IH} = 2 V	V _O = 2.4 V	NJO of etail 50 o	remit quies 50	μΑ	
los	Output short-circ	cuit current*	V _{CC} = MAX		-40 -100	-40 -100	mA	
Icc	Supply current		V _{CC} = MAX.	Outputs open	115 155	115 145	mA	

^{*} Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

Switching Characteristics $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$

SYMBOL	PARAMETER	PARAMETER TEST CONDITIONS (See Test Load/Waveforms)			MAX	UNIT	
fMAX	Maximum output clock frequency	ng) sol-a	C _L = 50 pF R _L = 280Ω OE = L	40		MHz	
	Maximum diagnostic alcak fraguanay	Cascaded	$C_1 = 50 \text{ pF R}_1 = 2 \text{ K}\Omega$	20		MHz	
fMAXD	Maximum diagnostic clock frequency	Uncascaded	CL - 50 PF HL - 2 KII	25		IVITIZ	
tCLK	CLK to output delay	-38	C _L = 50 pF R _L = 280Ω OE = L		14	ns	
tss	SDI to SDO delay (MODE = HIGH)		-v-1 200W		12	ns	
tMS	MODE to SDO delay		$C_L = 50 \text{ pF R}_L = 2 \text{ K}\Omega$		17	ns	
t _{DS}	DCLK to SDO delay (MODE = LOW)	- Fu	hox ¹		28	ns	
^t DEZL			4A 00-00		25	ns	
^t DEZH	DCLK to D7-D0 enable delay		$C_L = 50 \text{ pF R}_L = 2 \text{ K}\Omega$		20	ns	
†DDLZ	DOLK to D7 D0 disable dalor		C - 5 - 5 D - 0 KO		36	ns	
^t DDHZ	DCLK to D7-D0 disable delay		$C_L = 5 pF R_L = 2 K\Omega$		60	ns	
^t DC	DCLK to CLK separation		C _L = 50 pF R _L = 280Ω OE = L	22		ns	
tCD	CLK to DCLK separation		CL = 50 pr RL = 28011 OE = L	35		ns	
t _{PZL}	Output enable delay	tor typical regist	$C_{L} = 50 \text{ pF R}_{L} = 280\Omega$		19	ns	
^t PZH	Output enable delay		OL - 30 PF HL = 28011		13	ns	
t _{PLZ}	Output disable delay		C. = 5 pE D. = 2800		12	ns	
t _{PHZ}	Output disable delay		$C_L = 5 pF R_L = 280\Omega$		22	ns	

Switching Characteristics Over Operating Range

SYMBOL	PARAMETER Maximum output clock frequency		TEST CONDITIONS (See Interface Test Load/Waveforms)	MILI	TARY MAX	COMM	ERCIAL MAX	UNIT
fMAX			C _L = 50 pF R _L = 280Ω OE = L	33		40		MHz
4.	Maximum diagnostic	Cascaded	0 - 50 - F D - 0 KO	16		20		NACC-
^f MAXD	clock frequency	Uncascaded	$C_L = 50 \text{ pF R}_L = 2 \text{ K}\Omega$	20		25		MHz
tCLK	CLK to output delay	T. John Staff	C _L = 50 pF R _L = 280Ω OE = L	, J	18		14	ns
tss	SDI to SDO delay (MC	DE = HIGH)			18	104	15	ns
^t MS	MODE to SDO delay		$C_L = 50 pF R_L = 2 K\Omega$		27		18	ns
t _{DS}	DCLK to SDO delay (N	MODE = LOW)			38	30		ns
^t DEZL			0 50 5 5 0 000		35		25	ns
^t DEZH	DCLK to D7-D0 enable	e delay	$C_L = 50 \text{ pF R}_L = 2 \text{ K}\Omega$		30	LE SE	25	ns
†DDLZ	DCLK to D7-D0 disabl	o dolay	C - 5 p B - 2 KO		45	V	45	ns
^t DDHZ	BOEK to BY-Bo disabi	e delay	$C_L = 5 pF R_L = 2 K\Omega$		90	Marine San	80	ns
t _{DC}	DCLK to CLK separati	on	C = 50 = F D = 0000 OF = 1	30		30		ns
tCD	CLK to DCLK separati	on	$C_L = 50 \text{ pF } R_L = 280\Omega \text{ OE} = L$	45		40		ns
t _{PZL}	Output anable dalay		C _L = 50 pF R _L = 280Ω	e 2. Se	25		20	ns
^t PZH	Output enable delay		CL = 50 pr HL = 28011		20		15	ns
t _{PLZ}	Output disable delay		C - 5 - F D - 0000		20		15	ns
t _{PHZ}	Cutput disable delay		$C_L = 5 pF R_L = 280\Omega$	137	30		25	ns

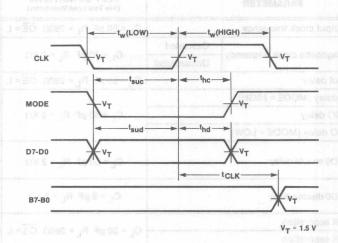


Figure 1. Switching waveforms for typical register applications (OE = L)

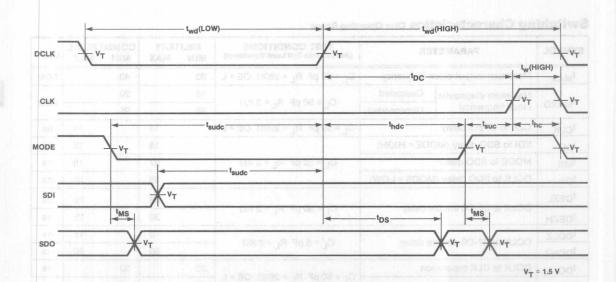


Figure 2. Switching waveforms for shift-in followed by diagnostic load

Timing Waveforms

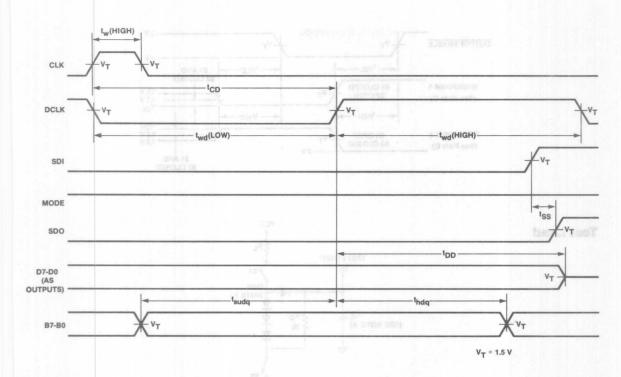
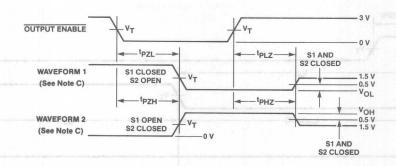
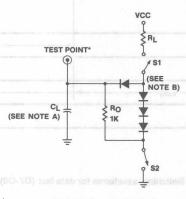


Figure 3. Switching waveforms for data bus (D7-D0) disabling

Enable/Disable Delay



Test Load



- * The "TEST POINT" is drived by the output under test, and observed by instrumentation.
- NOTES: A. CL includes probe and jig capacitance.
 - B. All diodes are 1N916 or 1N3064.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
 Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - D. In the examples above the phase relationships between inputs and outputs have been chosen arbitrarily.
 - E. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz Z_{Out} = 50Ω and for series 54/74S t_{R} = 2.5 ns $t_{F} \leq 2.5$ ns.
 - F. When measuring propagation delay times of 3-state outputs, switches S1 and S2 are closed.

	B7-B0	D7-D0, SDO
RO	1 ΚΩ	5 ΚΩ

Basics of Diagnostics

The basic theory of diagnostics is to insert test data to the inputs of a typical system and sample the test results from certain nodes of the circuits. For a combinatorial circuit, testing is very easy since the circuit has no memory of the previous states. But for a sequential circuit, the data to be sampled at a node depends not only on the inputs, but also on the current state it is in. If the previous state contains some error, it will possibly perform an illegal jump. In that case, depending on which state the system is currently in, the next state may be different. After several illegal jumps, it will be quite impossible to keep track of the jumps which it performs.

A way to solve the problem is by converting a sequential circuit to a combinatorial one. A sequential circuit can often be viewed as a network with a clock and a number of inputs and outputs, with some outputs being routed back to the inputs (see Figure 5a). If the loop is broken and inputs which are fed back from the outputs are instead fed in from some external sources (see Figure 5b), the system can be viewed as combinatorial and system testing will be easier. The "shadow register" concept involves shifting in serial data to the hidden register (the shadow register) and then loading test data to the output register. Together with other system inputs, the test results will appear on the output end of the network and can be sampled and analyzed.

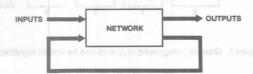


Figure 5a. A typical digital system

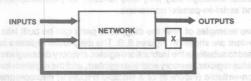


Figure 5b. The feedback of figure 5a is broken to convert the system to a non-sequential one

Diagnostic On-Chip™ (DOC™) Using Shadow Register

The diagnostic register is an 8-bit register with two levels of registers—a shadow register and an output register. A shadow register is basically a buried register with shift capability. There is also an output register whose outputs appear to the rest of the system. There is an output flipflop to each shadow flipflop. An output flipflop drives a three-state output buffer before going to the output pin. If the output is disabled, the output pin may be converted to an input pin. This feature is very important if the output is driving a bus and sampling of data on the bus is desired.

The input to a bit of the shadow register is a multiplexer which can select from one of the following nodes:

- a) Output of the preceding bit of the shadow register (or SDI for the least significant bit).
- b) Output of the same bit of the shadow register.
- c) Data on the output pin of the same bit. This data may be the output of the corresponding bit of the output register if there is no output enable pin and the output is enabled, or the input to that pin if there is an output enable pin and output is disabled. Refer to Figure 6 for some general information on a typical diagnostic functional part with output enable (OE).

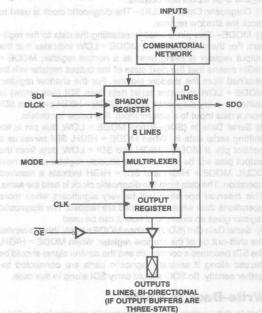


Figure 6. A typical functional block diagram for a diagnostic part

The input to any bit of the output register is also selected from one of the following nodes:

- a) Corresponding input bit.
- b) Corresponding output bit of the shadow register.

The reasons why a shadow register is preferred, as compared to shifting in diagnostic data directly to the output register, are:

- a) The output register contains control signals for the system. Certain bits of this register may control different ports which are driving the same bus. As diagnostic data is shifted in, these bits become random and the ports they are controlling may drive a bus simultaneously. Invalid data may appear and worst of all, with a low-impedance path between the power supply, severe damage may be done to these ports.
- b) As a diagnostic word is shifted in, the system is performing different tasks from what it is supposed to do. For example, when an ALU is performing an addition, diagnostic data is shifted in. The ALU then performs some other functions. The status of the system keeps changing. In some cases, illegal states may appear which produces unpredictable test results; for example, a flag may appear unpredictably.
- c) The shadow register enables diagnostic data to be shifted in as background data without holding up the processor operation.

The diagnostic register is one part in a series of diagnostic products which follows a new standard for diagnostics. The basic standard is described in Figure 6 and the table on page one. This standard implies that all diagnostic parts in this series are cascadable.

Diagnostic Pins a stdere tugito as a sverts to rio texts

There are several pins in the diagnostic register in addition to the regular 8-bit inputs and outputs:

1) Diagnostic Clock (DCLK)—The diagnostic clock is used to clock the shadow register.

2) MODE—This pin is used in selecting the data to the registers. For the output register, MODE = LOW indicates that the output register is being used as a normal register; MODE = HIGH means that the next state of the output register will be obtained from the shadow register. For the shadow register, MODE = LOW indicates serial data from SDI (see below) is shifted in every diagnostic clock; MODE = HIGH switches SDI from a data input to a control input. See below for details.

3) Serial Data In (SDI)—When MODE = LOW, this pin is for shifting serial data in. When MODE = HIGH, SDI serves as a control pin. If MODE = HIGH and SDI = LOW, data from the output pins will be loaded to the shadow register on the next DCLK. MODE = HIGH and SDI = HIGH indicate a reserved operation. The data from the diagnostic clock is held the same. This reserved operation will be very significant when more operations than what is described are needed. The diagnostic register gives an example of how it can be used.

4) Serial Data Out (SDO)—When MODE = LOW, this pin carries the shift-out bit of the shadow register. When MODE = HIGH, the SDI becomes a control pin and the control signal should be passed along if several diagnostic parts are connected together serially. So SDO should carry SDI along in this case.

Write-Back to RAMs

Due to the applications of a diagnostic register in a writable microprogram control store, this part also includes an additional feature to initialize the control RAMs; when necessary, the input data pins to the register can be operated as output pins. In short, a diagnostic register is an 'asymmetric register transceiver' with shift capability. The term 'asymmetric register transceiver' means that there are two bidirectional registered ports on a chip, and these ports are enabled with different methodologies and have different timings. One port is still primarily for inputs (D7-D0), while the other is primarily for outputs (B7-B0).

When MODE and SDI are both HIGHs, the D7-D0 will be converted to an output port on the rising edge of the next DCLK by enabling the three-state buffers driving the D7-D0. The input for the three-state buffers is from the outputs of the shadow register (S7-S0).

Applications

This part can be used as a: microprogram control store register, data register, status register, address register, instruction register, interrupt mask register, interrupt vector, program counter, stack pointer, and for other general purposes.

If the diagnostic registers are used in a system using microprogram control words, status registers, and instruction registers, etc., one way to connect them together is shown in Figure 7. There is only one data input and one data output to the diagnostic parts. When serial data is shifted in or shifted out, data has to be passed from one diagnostic chip to another. Since SDI must be passed from chip-to-chip if it is used for control, it is necessary for logic designers to make sure the fall-through time of SDI to the last chip and the setup time from SDI to DCLK are satisfied.

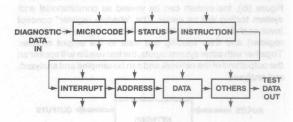


Figure 7. One way diagnostic registers can be linked together

The diagnostic registers are basically used for diagnostic purposes, although they may also function as parallel-to-serial and serial-to-parallel converters.

Two examples of how the diagnostic parts can be built into a system are shown in Figures 8, 9. The diagnostic registers are used to substitute the instruction register, memory data registers, status register, memory address registers, and the registers for an on-writable (Figure 8) or a writable (Figure 9) microprogram control store. The only additional block to a typical system without diagnostic features is the diagnostics controller. The diagnostics controller should be able to supply the system with signals like MODE, SDI, DCLK, and the register clock (CLK). In order words, the diagnostics controller in itself is a supercontroller of the processing unit. It should also be noted that all sequential paths, except for the register files, should be converted to combinatorial paths if all the diagnostic parts are to break the sequential loops.

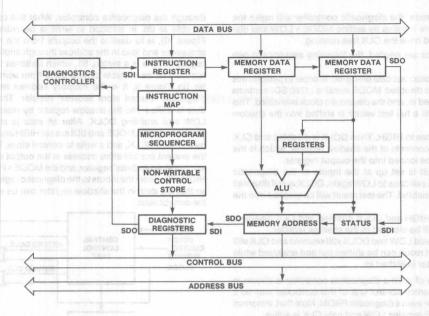


Figure 8. An application example of using diagnostic registers in a CPU using non-writable control store

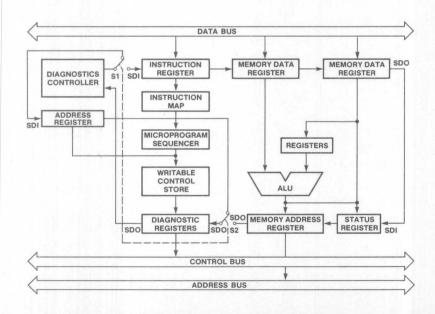


Figure 9. An application example of using diagnostic registers in a CPU using writable control store

In normal operation, the diagnostic controller will make the diagnostic feature inactive by setting MODE = LOW and disabling DCLK and have the CLK free running.

When diagnostics are needed, the following sequence is performed:

- 1) Shift in diagnostic test data bit-by-bit. In order to perform this operation, CLK is disabled; MODE remains LOW; SDI contains the bit to be shifted in, and the diagnostic clock is enabled. This will continue until a full test vector is shifted into the shadow register.
- 2) MODE switches to HIGH. Then DCLK is disabled and CLK is enabled. The contents of the shadow register, which is the test vector, will be loaded into the output register.
- 3) The test result is set up at the inputs of the diagnostic registers. MODE switches to LOW again. DCLK is still disabled and CLK is still enabled. The test result will be clocked into the output register.
- 4) With MODE HIGH and DCLK enabled and CLK disabled, the test result will be clocked to the shadow register.
- 5) With MODE held LOW and DCLK still enabled and CLK still disabled, the test result can be shifted out and analyzed while another test vector is shifted in.

A block diagram of such a diagnostics controller is shown in Figure 10. The central control unit of this controller may be a disk-based unit or even a diagnostic PROM. Note that, in normal operation, MODE remains LOW and only CLK is active.

Figure 9 is an example with writable programmable control store where initialization of the control RAMs is necessary. This can be done by loading in a sequence of data and address

through the diagnostics controller. What this controller must be able to do, in addition to what is described above (see Figure 10), is to disable the outputs from the microprogram sequencer and feed in the address through another diagnostic register. There is a switch, S1, which switches the SDI to the registers of the writable control store from some other register (in Figure 9, it is the memory address register) to the diagnostic 'control store address' register. The initialization data is shifted into the shadow register by resetting MODE to LOW and enabling DCLK. After all data is shifted into the shadow register, MODE and SDI are set HIGH and then followed by a CLK, a DCLK, and a write to control store. The CLK loads the present control store address in the output registers of the 'control store address' register, and the MODE = HIGH and SDI = HIGH will enable the inputs to the diagnostic register as outputs, so that the data in the shadow register can be written back to the control store.

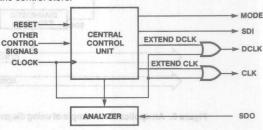
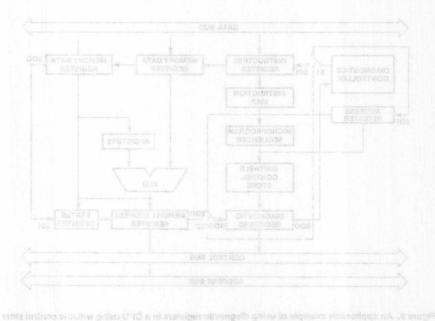


Figure 10. A diagnostic controller unit



8-Bit Bus Latch Transceivers-**Advanced CMOS-TTL Compatible**

74ACT547 74ACT567

Features/Benefits

- Bidirectional transceivers utilizing latches
- . Independent latches for A bus and B bus
- Data can be swapped between internal latches
- · 8-bit data paths match byte boundaries
- '547/'567 devices can replace two '373 devices
- . Independent gate enables for rank A and rank B
- Low quiescent supply current of < 10 μA (typical)
- Active supply current at about 20% LS equivalent
- Wide commercial operating supply and temperature ranges 4.5 V to 5.5 V; -40°C to +85°C
- 24-pin SKINNYDIP® saves space.

Description

These transceivers have a pair of 8-bit latches connected backto-back, i.e. the bus pins are used for input or output. The latches are followed by either non-inverting ('ACT547) or inverting ('ACT567) three-state buffers.

Both devices have independent gate enable inputs for ranks A and B (GA1, GA2, GB1, GB2), and independent output enables for ranks A and B (OEAB, OEBA).

The direction of operation is controlled by OEAB and OEBA. When OEAB is Low and OEBA is High, the devices operate in the A-to-B direction. When OEAB is High and OEBA is Low, the devices operate in the B-to-A direction. When OEAB and OEBA are both High, the A and B buses are configured as inputs. When OEAB and OEBA are both Low, the A and B buses are configured as outputs. See the Bus Operation Tables for the detailed operation.

Data is passed through the latch whenever either of the gate enables for the respective rank (GA1 or GA2, GB1 or GB2) are

All of the 8-bit devices are packaged in the popular 24-pin SKINNYDIP® package.

Ordering Information

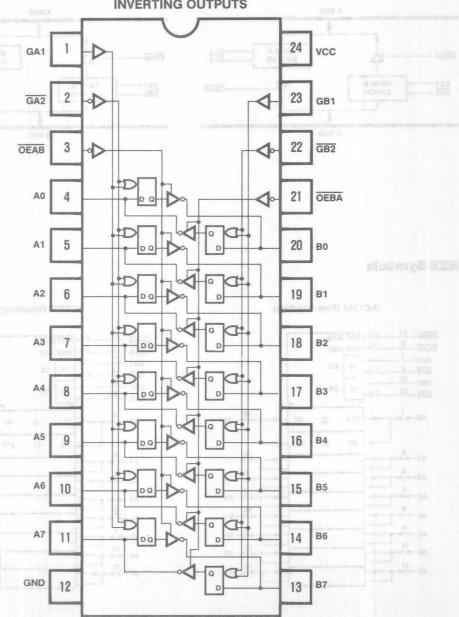
PART NUMBER	PACKAGE	TEMPERATURE	POLARITY	TYPE	TECH
74ACT547	NS, JS	Commercial	Noninvert	Lateb	2040
74ACT567	NS, JS	Commercial	Invert	Latch	CMOS

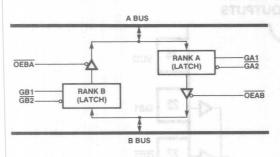
Logic Symbol

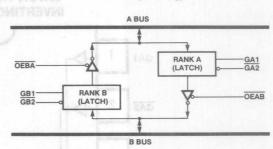
LATCH TRANSCEIVER **NON-INVERTING OUTPUTS** GA1 VCC GA2 OEAB GB2 OEBA 21 A0 20 A1 B0 19 A2 B1 18 A3 B2 17 A4 **B3** 16 A5 **B**4 10 15 **B5** A6 11 14 **B6** GND 12 13 **B7**

Logic Symbol

74ACT567 LATCH TRANCEIVER INVERTING OUTPUTS





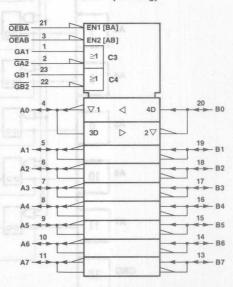


IEEE Symbols

'ACT547 (Non-inverting)

OEBA 21 EN1 [BA] OEAB -EN2 [AB] GA1-≥1 GA2 _ 2 GB1 ____23 C4 ≥1 GB2 22 20 ★ ➤ B0 A0 --- $\nabla 1$ 4D 1 3D 2 7 A1 5 19 **← ►** B1 18 ★ ► B2 A2 -> 17 ★ ► B3 A3-4-1 16 ★ ► B4 15 ★ B5 A5 -14 ► B6 13 **★** B7

'ACT567 (Inverting)



Function Table Nomenclature Description

7: Eight ing	put/output pins on the A side.
	put/output pins on the B side.
HorLst	ate irrelevant ("Don't Care" conditions)
Gate ena	ables for rank A of 'ACT547/'ACT567.
B2: Gate ena	ables for rank B of 'ACT547/'ACT567.
OB: Previous	data of the internal rank A/B.
GB2: Gate ena	ables for rank B of 'ACT547/'ACT56

GA1	GA2	RANK A GB1		GB2	RANK B
X d Z L X		(Flush)		A L X	Enabled (Flush)
X	D Lis	Enabled (Flush)	or L	Н	Disabled (Freeze)
Brite Prince	H	Disabled (Freeze) X L			Enabled (Flush)
LBo	9 H	Disabled (Freeze)	neFL	Н	Disabled (Freeze)
Hud	X	Enabled (Flush)	Х	K - H	Enabled (Flush)
H eud	X	Enabled (Flush)	The second secon		Disabled (Freeze)
Hild	×	Enabled (Flush)	ns/H	××	Enabled (Flush)

OEAB:	To enable the A-to-B operation.
OEBA:	To enable the B-to-A operation.

OEAB	OEBA	OPERATION DIRECTION
A L	L	A, B buses both are outputs (Transfer stored data to bus stored)
L	Н	A-to-B
Н	L	B-to-A
Н	Н	A, B buses both are inputs (storage)

Bus Operation for 'ACT547

OPERATION		CTION	DAT	A I/O	BLOCK DIAGRAM		ATE LE (A)	RANK A		LE (B)	RANK B				
OPERATION	OEAB	OEBA	A0-A7	B0-B7	BLOCK DIAGRAM	GA1	GA2	C Jughupi	GB1	GB2	HANK D				
		117			deronal.	1011 6120	Н	QoA	tel Lin	Н	QoB				
						L	Н	QoA	Н	X	B bus				
					A BUS	A TO LTO	AH S	QoA	X	BOL	B bus				
	1				BUS RANK B	A TOHO	X	A bus	deLes	Н	QoB				
Storage	Н	Н	Input	Input	RANK	SAH	X	A bus	Н	X	B bus				
					A	Н	X	A bus	X	L	B bus				
					BU	X	L	A bus	L	Н	QoB				
							L	A bus	H	X	B bus				
						X	L	A bus	X	L	B bus				
					19290	L	Н	QoA	L	Н	QoB				
	.noltme	go Gret-	A acts elek	ns oT	SASO belds	1	Н	QoA	Н	X	B bus				
	.notine	go A-ot-	Barti eldi	To en			Н	QoA	X	L	B bus				
		and the same of	Output	Andreas are a series	BUS RANK	H	X	Rank B	IS LO	H	QoB				
B-to-A Operation	Н	L	of	Input	8450	Н	X	Rank B	Н	X	B bus				
du)120 ens		Rank B	1	RANK A	Н	X	Rank B	X	LX	B bus				
	data to	të dje s	tento(T)		BU	X	L	Rank B	id Li	Н	QoB				
			A-to-l3	H		X	L	Rank B	Н	X	B bus				
	Annual Section		A-IN-8		Delor	X	L	Rank B	X	LX	B bus				
	A STATE OF THE	100000							and the second s	L	Н	QoA	L	Н	QoB
		4 7				L	Н	QoA	Н	X	Rank A				
					A BUS	L	Н	QoA	X	L	Rank A				
		L H		Output	RANK B	Н	X	A bus	L	Н	QoB				
A-to-B Operation	L		Input		RANK	Н	X	A bus	Н	X	Rank A				
				Rank A	AB	Н	X	A bus	X	L	Rank A				
					ви	X	L	A bus	L	Н	QoB				
						X	L	A bus	Н	X	Rank A				
		3 %				X	L	A bus	X	L	Rank A				
		THE				L	Н	QoA	L	Н	QoB				
						L	Н	QoA	Н	X	Rank A				
					A BUS	L	Н	QoA	X	L	Rank A				
Transfer			Output	Output	RANK	Н	Х	Rank B	L	Н	QoB				
Stored	L	L	of	of	RANK	H*	Х	Rank B	Н	Х	Rank A				
Data		1111	Hank B	Rank A	B BU	H*	Х	Rank B	Х	L	Rank A				
						X	L	Rank B	L	Н	QoB				
						X*	L	Rank B	Н	Х	Rank A				
			3.3			X*	L	Rank B	X	L	Rank A				

^{*} Note: These controls for OEAB, OEBA, GA1, GA2, GB1 and GB2 can cause race conditions.

Absolute Maximized Addings

13

Bus Operation for 'ACT567

OPERATION		TROL	DAT	A I/O	BLOCK DIAGRAM		ATE BLE (A)	RANK A		ATE (B)	RANK B
OPERATION	OEAB	EAB OEBA A0-A7 B0-B7 GA1	GA2	Lice or	GB1	GB2	DANK E				
						L	Н	QoA	Est.	Н	QoB
						L	H	QoA	. н.	X	B bus
					A	L	Н	QoA	X	L	B bus
		F 18			BUS RANK B	Н.,	Χ	A bus	L	Н	QoB
Storage	Н	Н	Input	Input	RANK	Н	X	A bus	"H	X	B bus
					A B	Н	X	A bus	Х	L	B bus
					BUS	X	L	A bus	L	Н	QoB
		MERCI	EDD			X	L	A bus	Н	X	B bus
	4	SYT		¥100		X	L	A bus	X	L	B bus
v 8.8		3		4,5		L	Н	QoA	flot/k	Ĥ	QoB
				172		L	Н	QoA	Н	X	B bus
				12	A BUS	L	Н	QoA	X	L	B bus
			Output	12	RANK	Н	X	Rank B	L	Н	QoB
B-to-A	Н	L	of	Input	B B	Н	X	Rank B	Н	X	B bus
Operation			Rank B	18	RANK A	Н	X	Rank B	X	L	B bus
				18	BUS TAIL GET	X	L	Rank B	L	Н	QoB
				18	\$80 JAD	X	L	Rank B	Н	X	B bus
		Landa Inda		14	GA., GRI	X	L	Rank B	X	L	B bus
80	.x			18	9887 (988	L	Н	QoA	L	Н	QoB
				16	TEO TAO	L	Н	QoA	Н	X	Rank A
					A BUS	L	Н	QoA	X	L	Rank A
				Output	RANK	Н	X	A bus	L	Н	QoB
A-to-B Operation	L	Н	Input	of	RANK	Н	X	A bus	Н	X	Rank A
LEUDINE THE	of 1013 St	HDM-44	or I smit	Rank A	A B	Н	X	A bus	X	L	Rank A
					BUS	X	L	A bus	L	Н	QoB
				-		X	L	A bus	Н	X	Rank A
						X	L	A bus	X	L	Rank A
						L	Н	QoA	L	Н	QoB
						L	Н	QoA	Н	X	Rank A
					A BUS	L	Н	QoA	X	L	Rank A
Transfer			Output	Output	RANK	Н	X	Rank B	L	Н	QoB
Stored	L	L	of	of	В	H*	X	Rank B	Н	X	Rank A
Data			Rank B	Rank A	RANK	H*	X	Rank B	X	L	Rank A
					B	X	L	Rank B	L	Н	QoB
						X*	L	Rank B	Н	X	Rank A
		1				X*	L	Rank B	X	L	Rank A

^{*} Note: These controls for OEAB, OEBA, GA1, GA2, GB1, and GB2 can cause race conditions.

Absolute Maximum Ratings

Supply voltage, V _{CC}	5 V to 7.0 V
DC input voltage, V ₁	CC + 0.5 V
DC output voltage, V _O	CC + 05 V
DC output source/sink current per output pin, IO	±35 mA
DC V _{CC} or ground current, I _{CC} or I _{GND}	. ±200 mA
Input diode current, I _{IK} : V _I <0	
V ₁ <0	20 mA
≥V _C C×HA3QH.	+20 mA
Output diode current, IOK: NO<0	
V _O <0	20 mA
V _O >V _{CC}	+20 mA
Storage temperature -65°	to +150°C

Operating Conditions 3 X

SYMBOL	PAI A Dus X L	RAMETER	MIN		IMERCIAL TYP	MAX	UNIT	
Vcc	Supply voltage		4.5		5	5.5	V	
TA	Operating free air temperatu	re		-40			85	°C
tw	Width of gate	l l	High	12	1			
Boo I	Width of gate	HILL	_ow	12				ns
aud 8	X Rank B H X	14.07547	GA1, GB1	81	0		H L	A-BI-
	Cat and Binds X	'ACT547	GA2, GB2	81	SH RAL			Breda
t _{su}	Setup time	aua -	GA1, GB1	81				ns
acid S	X H Banka 1	'ACT567	GA2, GB2	81				
and a	L Rank B X L	VA 07547	GA1, GB1	81				
th Son		'ACT547	GA2, GB2	81				
τh	Hold time	IA OTEOT	GA1, GB1	81				ns
		'ACT567	GA2, GB2	1			3731016	
tr	Input rise time at V _I = 4.5 V		MAN SUB	0			500	ns
tf	Input fall time at V _I = 4.5 V			0			500	ns

1 The arrows indicate the transition of the gate control input used as reference: 1 for the LOW-to-HIGH transitions, 1 for the HIGH-to-LOW transitions.



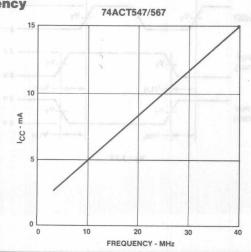
Electrical Characteristics Over Operating Conditions

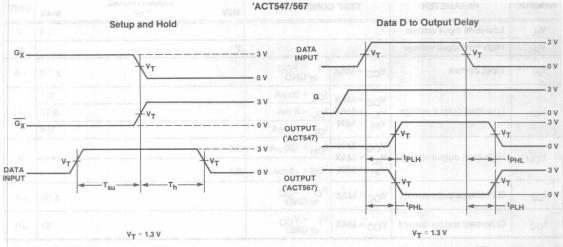
SYMBOL	PARAMETER	TEST (CONDITIONS	MIN	COMMERCIAL TYP	MAX	UNIT	
VIL	Low-level input voltage	10/52			LINET DIES COPES	0.8	V	
VIH	High-level input voltage		ATAG VOL	2			V	
IIN	Input current	V _{CC} = MAX	V _I = V _{CC} or GND		19/	± 1.0	μΑ	
V	V _{OL} Low-level output voltage	Voc = MAX	I _{OL} = 20 μA			0.1	V	
VOL		V _{IL} = MAX V _{IH} = MIN	I _{OL} = 6 mA		144	0.37		
			I _{OL} = 12 mA		AND THE RESIDENCE OF THE PARTY	0.4		
Va	High lovel output voltage	V _{CC} = MIN	I _{OH} = -20 μA	3.4		~	V	
VOH	High-level output voltage	V _{IL} = MAX V _{IH} = MIN	IOH = -6 mA	2.4		N.	ATA	
loz	Off-state output current	V _{CC} = MAX	V _O = V _{CC} or GND		Ste ¹	± 30	μΑ	
lcc	Quiescent supply current	V _{CC} = MAX	V _I = V _{CC} or GND		Nation and	80	μΑ	

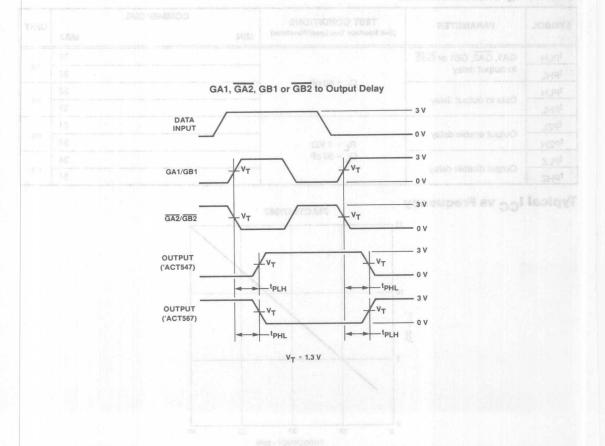
Switching Characteristics

SYMBOL	PARAMETER	TEST CONDITIONS (See Interface Test Load/Waveform)	COMMERCIAL	MAX	UNIT	
t _{PLH}	GA1, GA2, GB1 or GB2			32		
tPHL	to output delay	0 - 50 - 5		32	ns	
t _{PLH}	2	C _L = 50 pF	GAS CAS	32		
t _{PHL}	Data to output delay		and the state of t	32	ns	
t _{PZL}	Output analyte datas		1098	34		
t _{PZH}	Output enable delay	R _L = 1 KΩ		34	ns	
t _{PLZ}	Outout disable delevi	C _L = 50 pF		34		
t _{PHZ}	Output disable delay		ISOTAD	34	ns	

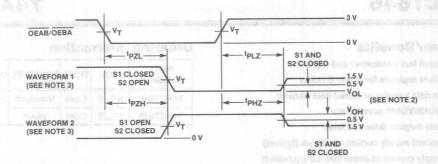
Typical I_{CC} vs Frequency



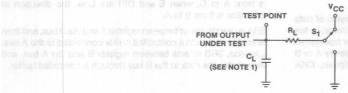




Enable/Disable Waveforms



Test Load



Notes: 1. C_L includes probe and jig capacitance.

- When measuring tpzL, S₁1 is tied to V_{CC}. When measuring tpHz and tpzH, S₁ is tied to ground.
 - When measuring propagation delay times of three-state outputs, $\rm S_1$ is open, i.e. not connected to $\rm V_{CC}$ or ground.
- Waveform 1 is for an output with internal conditions such that the output is Low except when disabled by the output control.
 - Waveform 1 is for an output with internal conditions such that the output is High except when disabled by the output control
- 4. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
- 5. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $t_{r} \leq$ 6 ns, $t_{f} \leq$ 6 ns, Z_{out} = 50 Ω .

8-Bit Bus Front-Loading Latch Transceivers — Advanced CMOS-TTL Compatible 74ACT646 74ACT648

Features/Benefits

- · Bidirectional bus transceiver and register
- Independent registers for A and B buses
- · Real-time data transfer or stored data transfer
- 24-pin SKINNYDIP® saves space
- . Three-state outputs drive bus lines
- Low quiescent supply current of <10 μA (typical)
- · Active supply current at about 20% LS equivalent
- Wide commercial operating supply and temperature ranges 4.5 V to 5.5 V; -40°C to +85°C

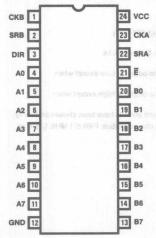
Description

This 8-bit bus transceiver with three-state outputs has sixteen D-type flip-flops and multiplexers. The bus-oriented pinout of the part is shown in the Pin Configuration. The internal gate-level hardware configurations for the 'ACT646/648 are given in the Logic Diagram. The basic repeated element, consisting of an edge-triggered flip-flop paralleled with a bypassing path, or "feed-through", into a two-way multiplexer is sometimes called a "front-loading latch."

A pair of multiplexers are used to distribute two bytes of data through the part. The data-routing combinations offered by the multiplexers provide flexibility in directing data to or from either bus, and/or either register. Data is loaded into registers A or B upon the rising edge of the appropriate clock signals. CKA

Pin Configurations

'ACT646/648 8-Bit Bus Front-Loading Latch Transceiver



Ordering Information

PART NUMBER	PKG	TEMP	POLARITY	OUTPUT	TECH
74ACT646	NS,JS	Com	Noninvert	Three-	CMOC
74ACT648	NS,JS	Com	Invert	state	CMOS

clocks register A, which receives data from the B bus directly at its inputs. Similarly, CKB clocks register B, which has the A bus available directly at its inputs. Control of the multiplexers is provided by two select lines (one per register), SRA and SRB. Command of the outputs is performed by enable line $\overline{\mathbb{E}}$, and direction line DIR.

When \overline{E} is High, data from the buses can be stored into register A and B. When \overline{E} is Low and DIR is High, the direction of operation is from A to B, when \overline{E} and DIR are Low, the direction of operation is from B to A.

SRA is used to select between register A and the B bus, and then to route the data to a controlled buffer connected to the A bus. Likewise, SRB selects between register B and the A bus, and then routes the data to the B bus through a controlled buffer.

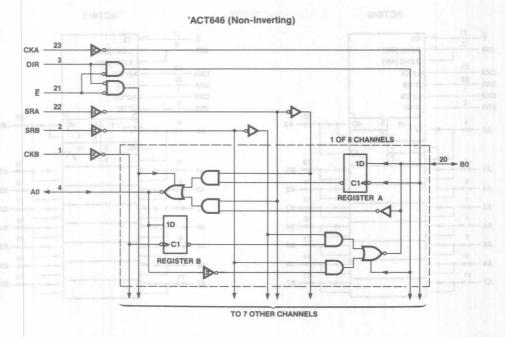
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TWX: 910-338-2376

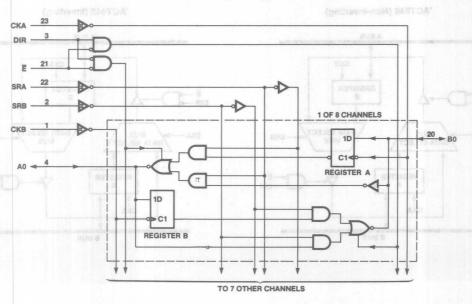
2175 Mission College Bivd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2374

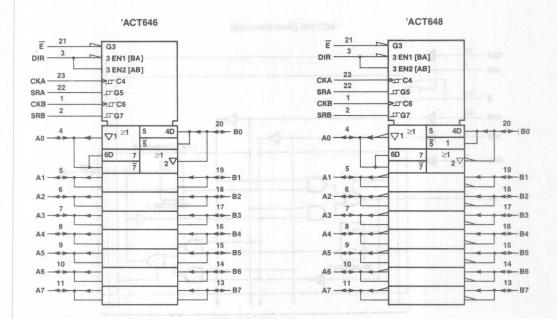


Logic Diagrams

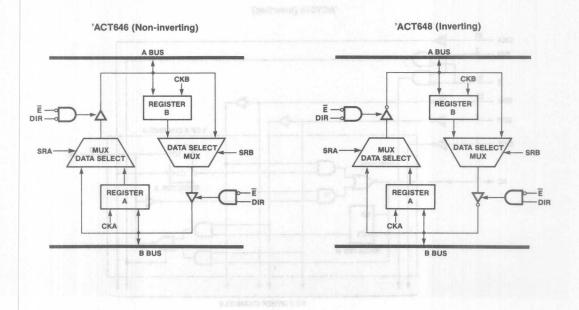


'ACT648 (Inverting)





Block Diagrams



	n Table											DAT	où n		
Nomen	clature Desc		ion		To er	nable A	-to-B or	B-to-	A operation	on.		JON			EPERATION
		DIF	:10						operation						
			Ē	DU	DIR	aras.	OPER	ATION	DIREC	TION					
			1	1	L		PRINT!	B-1	to-A	tugat					
		Issa A	L		Н		- 100	A-1	to-B						
		Lagran	u		X	A	and B	buses	both are	inputs					
		學時间	H	Out	^			(Sto	rage)						
			A/SRI	⊖U 8•	To se	lect the	e outnu	t data	coming f	rom the	A/R				
		Real	ou		regist		RA/SRE	is a H	High leve						
		A0-	A7:		Eight	input/c	output p	ins on	the A sid	e.					
			B7:		Eight	input/o	output p	ins on	the B sid	e.					
		CK	A/CK	B:	Clock	Clock for Register A/B.									
		X:			Horl	_ state i	irreleva	nt ("Do	n't Care"	conditio	on).				
						ive edge e is ass		ck cau	ses clock	ing, if c	lock				
		UC	ou.		Horl	or ca	ase (noi	nclock	ed operat	ion).					
	R Adela A Dus	RG	TR:		Regis	ter.									
					STATE OF THE PARTY	er Di									
								8701							
					1										

Bus Operation for 'ACT646

OPERATION	CONTROL				DATA I/O		BLOCK DIAGRAM	FALA	BLE	'ACT646
	E	DIR	SRA	SRB	A0-A7	B0-B7	o select the direction of	CKA	СКВ	10
				-	an alare a sin			UC	UC	No operation
					HOP		BUS RGTR A	UC	til	Real time A bus data → RGTR E
Storage	Н	X	X	X	Input	Input	RGTR B B	1	UC	Real time B bus data → RGTR A
					NA SERVI	8-6	CKB CKA	1	t ¹	Real time A bus data → RGTR E Real time B bus data → RGTR A
						age)	018)	UC	UC	Real time B bus data → A bus
Real time				8	l, ant ma	it enimo	BUS RGTR	UC	†	Real time B bus data → A bus Real time B bus data → RGTR B
B-to-A	L	L	L	X	Output	Input	RGTR B	1	UC	Real time B bus data → A bus Real time B bus data → RGTR A
Operation						he A sid he B sid	CKB CKA	1	-A7: -81:	Real time B bus data → A bus Real time B bus data → RGTR A Real time B bus data → RGTR B
					is it has eve	Torse Control	or Latete implement ("Do	UC	UC	RGTR A data → A bus
Stored data					ola ti "gril	2.27	Α	UC	t	RGTR A data → A bus RGTR A data → RGTR B
B-to-A	L	L	Н	Х	Output	Input	RGTR B BUS	†	UC	Real time B bus data → RGTR A RGTR A data → A bus
Operation							скв ска	1	1	Real time B bus data → RGTR A RGTR A data → A bus RGTR A data → RGTR B
								UC	UC	Real time A bus data → B bus
Real time							A BUS RGTR A	UC	t	Real time A bus data → B bus Real time A bus data → RGTR B
A-to-B	L	Н	X	L	Input	Output	BBB	t	UC	Real time A bus data → B bus Real time A bus data → RGTR A
Operation							скв ска	1	†	Real time A bus data → B bus Real time A bus data → RGTR A Real time A bus data → RGTR B
								UC	UC	RGTR B data → B bus
Stored data							A BUS RGTR	UC	t	Real time A bus data → RGTR B RGTR B data → B bus
A-to-B	L	Н	X	н	Input	Output		t	UC	RGTR B data → B bus RGTR B data → RGTR A
Operation							CKB CKA	t	t	Real time A bus data → RGTR B RGTR B data → B bus RGTR B data → RGTR A

Bus Operation for 'ACT648

OPERATION		CON	TROL		DATA I/O		BLOCK DIAGRAM		BLE	'ACT648
VED SEV G	E	DIR	SRA	SRB	A0-A7	B0-B7		CKA	СКВ	
Am 068 ±		1		0.77	1911 1911	- 11-14	A	UC	UC	No operation
Am 05-							BUS RGTR	UC	1	Real time A bus data → RGTR B
Storage	Н	X	X	X	Input	Input	RGTR B	1	UC	Real time B bus data → RGTR A
Am 00+							CKB CKA	1 .	1	Real time A bus data → RGTR B Real time B bus data → RGTR A
D 9087 + 67 554						111111		UC	UC	Real time B bus data → A bus
Real time					_		BUS RGTR	UC	. 1	Real time $\overline{\underline{B}}$ bus data \rightarrow A bus Real time $\overline{\underline{B}}$ bus data \rightarrow RGTR B
B-to-A	L	L	L	х	Output	Input	RGTR B	1	UC	Real time \overline{B} bus data \rightarrow A bus Real time B bus data \rightarrow RGTR A
Operation		Dia 60	8386	cos			CKB CKA	1	1	Real time B bus data → A bus Real time B bus data → RGTR A Real time B bus data → RGTR B
XAN			VIAL		RI			UC	UC	RGTR Ā data → A bus
Stored data			8		6. (%		A BUS RGTR	UC	noon	RGTR A data → A bus RGTR A data → RGTR B
B-to-A	L	L	н	Х	Output	Input	RGTR B BUS	1	UC	Real time B bus data → RGTR A RGTR Ā data → A bus
Operation							скв ска	t	t	Real time B bus data → RGTR A RGTR A data → A bus RGTR A data → RGTR B
86 008						9		UC	UC	Real time A bus data → B bus
Real time							A BUS RGTR	UC	/ j k	Real time A bus data → B bus Real time A bus data → RGTR B
A-to-B	L	Н	X	L	Input	Output	RGTR B	1	UC	Real time $\overline{\underline{A}}$ bus data \rightarrow B bus Real time $\overline{\underline{A}}$ bus data \rightarrow RGTR A
Operation							CKB CKA	oola aet †	t t	Real time A bus data → B bus Real time A bus data → RGTR A Real time A bus data → RGTR B
								UC	UC	RGTR B data → B bus
Stored data							A BUS RGTR	UC	t	Real time A bus data → RGTR B RGTR B data → B bus
A-to-B	L	н	x	н	Input	Output	RGTR B	1	uc	RGTR B data → B bus RGTR B data → RGTR A
Operation							CKB CKA	1	1	Real time A bus data → RGTR B RGTR B data → B bus RGTR B data → RGTR A

Supply voltage, V _{CC}	-0.5 V to 7.0 V
DC input voltage, V ₁	-0.5 V to Voc +0.5 V
DC output voltage, VO	-0.5 V to Voo+0.5 V
DC output source/sink current per output pin, I _O	±35 mA
DC V _{CC} or ground current, I _{CC} or I _{GND}	± 100 mA
Input diode current, I _{IK} :	
Input diode current, I _{IK} : V _I <0	20 mA
V _I >V _{CC}	+20 mA
Output diode current, IOK:	
V _O <0	20 mA
A V _O >V _{CC} and a and lead	+20 mA
Storage temperature	65 to +150° C

Operating Conditions

SYMBOL	PARA	METER	MIN	COMMERCIAL	MAX	UNIT	
Vcc	Supply voltage		4.5	5	5.5	V	
TA	Operating free-air temperatur	re	-40		85	°C	
A STOR	Width of clock	High	20	X H L		ns	
tw	Width of clock	Low	20		l la	115	
t _{su}	Set up time		251			ns	
th	Hold time		Of			ns	
t _r and B	Input rise time at V _I = 4.5 V	U. T. T. T.	0		500	ns	
t _f sug 3	Input fall time at V _I = 4.5 V	0	0		500	ns	
ЮН	High-level output current	- A ROS			-6	mA	
OL	Low-level output current		quubi luqni		12	mA	

[†] The arrow indicates the Low-to-High transition of the clock input used as reference.

Electrical Characteristics Over Operating Conditions

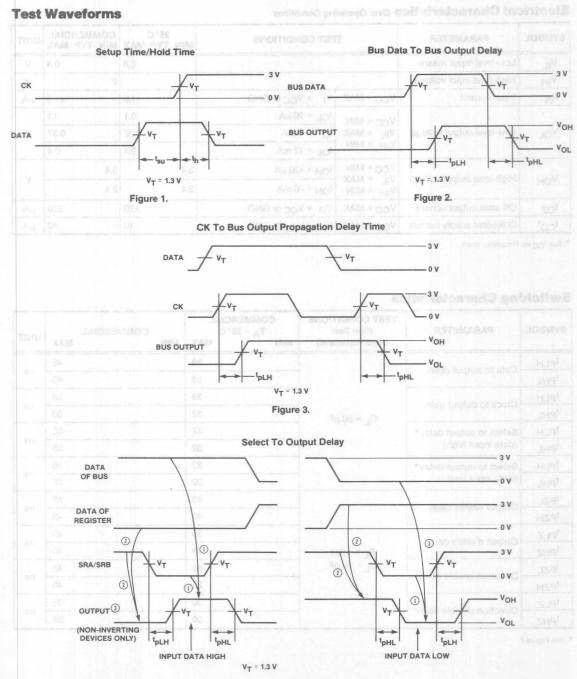
SYMBOL	PARAMETER	T MG on S	EST CONDITIONS	MIN	25°C TYP MAX	COMMERCIAL MIN TYP MAX	UNIT
V _{IL}	Low-level input voltage				0.8	0.8	٧
VIH	High-level input voltage		C210204	2		2	V
IIN	Input current	VCC = MAX	VI = VCC or GND	-	±1.0	±1.0	μΑ
	Low-level output voltage	VCC = MIN	I _{OL} = 20 μA		0.1	0.1	
VOL		V _{IL} = MAX V _{IH} = MIN	IO = 6 mA		0.32	0.37	V
gV			IOL = 12 mA		0.4	0.4	
and.	High land a task attach	VCC = MIN	IOH = -20 μA	3.4	146	3.4	.,
VOH	High-level output voltage	VIL = MAX	IOH = -6 mA	2.4	on and	2.4	V
loz	Off-state output current	V _{CC} = MAX	VO = VCC or GND		±10	±30	μΑ
lcc*	Quiescent supply current	VCC = MAX	VI = VCC or GND		10	40	μΑ

^{*} See ICC vs. Frequency chart.

Switching Characteristics

SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load/Waveform)	COMMERCIAL T _A = 25°C MIN MAX	COMMERCIAL MAX	UNIT		
^t PLH	Data to autout dallay		38	45			
tPHL	Data to output delay	A Company	38	45	ns		
t _{PLH}	Clock to output delay		32	38			
^t PHL	Clock to output delay	C _I = 50 pF	32	38	ns		
t _{PLH}	Select to output delay*		32	35			
tPHL	(data input high)		32	35	ns		
t _{PLH}	Select to output delay*		32	arrag 35			
tPHL	(data input low)		32	35	ns		
tPZL			40	45	H		
^t PZH	Output enable delay	e delay	40	40 A CAND 28 45	ns		
tPLZ	0 4- 4 4114- 4-1-		35	40			
t _{PHZ}	Output disable delay	$R_{L} = 1K\Omega$	35	40	ns		
t _{PZL}		C _L = 50 pF		45			
^t PZH	Direction enable delay		35	10 40	ns		
t _{PLZ}	10°		30	35			
t _{PHZ}	Direction disable delay		30	35	ns		

^{*} See Figure 4.



NOTES: 1. When SRA/SRB is low, the input data will transfer to output bus.

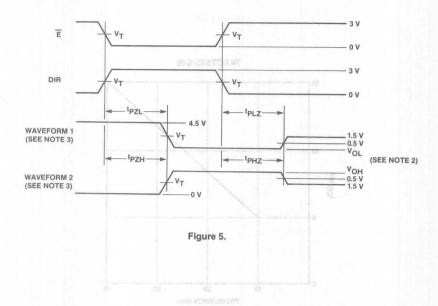
Figure 4.

^{2.} When SRA/SRB is high, the data of register will transfer to output bus.

^{3.} For the inverting devices, the timing is similar, but the output is opposite to that for the non-inverting devices.

Typical ICC vs. Frequency

Enable/Disable/Direction-Change Delay



Test Load

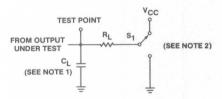


Figure 6.

NOTES 1. C_L includes probe and jig capacitance.

2. When measuring t_{PLZ} and $t_{PZL},\,S_1$ is tied to $v_{CC}.$ When measuring t_{PHZ} and $t_{PZH},\,S_1$ is tied to ground.

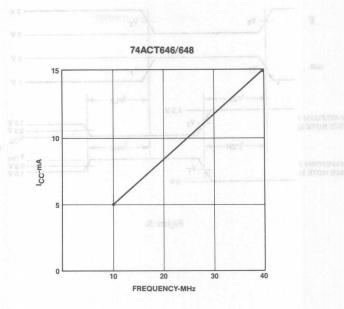
When measuring propagation delay times of three-state outputs, \mathbf{S}_1 is open, i.e., not connected to \mathbf{V}_{CC} or ground.

Waveform 1 is for an output with internal conditions such that the output is Low except when disabled by the output control.

Waveform 2 is for an output with internal conditions such that the output is High except when disabled by the output control.

- 4. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
- 5. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, t_f \leq 6 ns, t_f \leq 6 ns, Z_{OUt} = 50 $\Omega.$

Typical ICC vs. Frequency



8-Bit Bus Front-Loading Latch Transceivers — **Advanced CMOS-TTL Compatible** 74ACT651 74ACT652

Features/Benefits

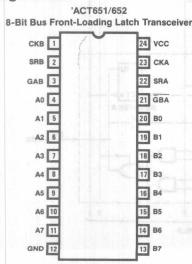
- · Bidirectional bus transceiver and register
- · Independent registers for A and B buses
- · Real-time data transfer or stored data transfer
- · Simultaneous outputs on both buses
- 24-pin SKINNYDIP® saves space
- . Three-state outputs drive bus lines
- Low quiescent supply current of <10 μA (typical)
- . Active supply current at about 20% LS equivalent
- · Wide commercial operating supply and temperature ranges 4.5 V to 5.5 V; -40° C to +85° C

Description

This 8-bit bus transceiver with three-state outputs has sixteen D-type flip-flops and multiplexers. The bus-oriented pinout of the part is shown in the Pin Configuration. The internal gatelevel hardware configurations for the 'ACT651/652 are given in the Logic Diagrams. The basic repeated element, consisting of an edge-triggered flip-flop paralleled with a bypassing path, or "feed-through", into a two-way multiplexer is sometimes called a "front-loading latch."

A pair of multiplexers are used to distribute two bytes of data through the part. The data-routing combinations offered by the multiplexers provide flexibility in directing data to or from either bus, and/or either register. Data is loaded into registers A or B

Pin Configurations



Ordering Information

PART NUMBER	PKG	TEMP	POLARITY	ОИТРИТ	TECH	
74ACT651	NS,JS	Com	Noninvert	Three-	CMOS	
74ACT652	NS,JS	Com	Invert	state	CIVIOS	

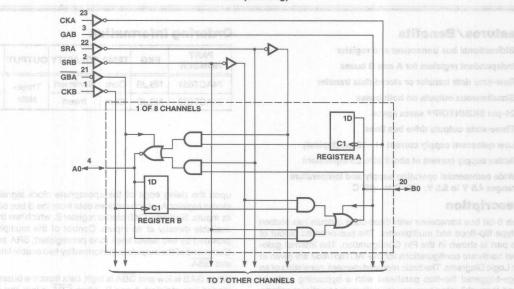
upon the rising edge of the appropriate clock signals. CKA clocks register A, which receives data from the B bus directly at its inputs. Similarly, CKB clocks register B, which has the A bus available directly at its inputs. Control of the multiplexers is provided by two select lines (one per register), SRA and SRB. Command of the outputs is performed by two enable lines, GAB and GBA.

When GAB is low and GBA is high, data from the buses can be loaded into registers A and B. When GBA is low, the A bus is configured for output. When GAB is high, the B bus is configured for output. The A and B buses can be enabled at the same time. to operate as outputs simultaneously.

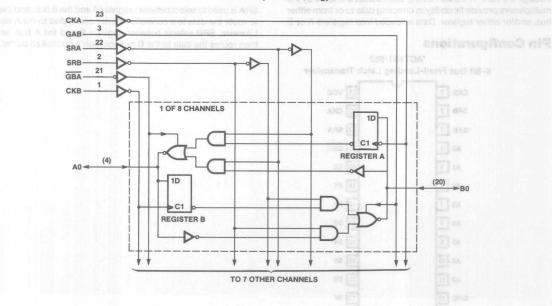
SRA is used to select between register A and the B bus, and then to route the data to a controlled buffer connected to the A bus. Likewise, SRB selects between register B and the A bus, and then routes the data to the B bus through a controlled buffer.

Logic Diagrams

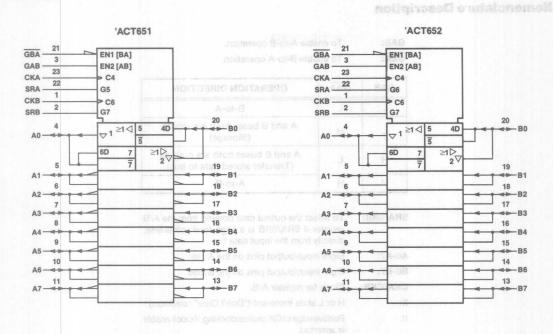
'ACT651 (Inverting)



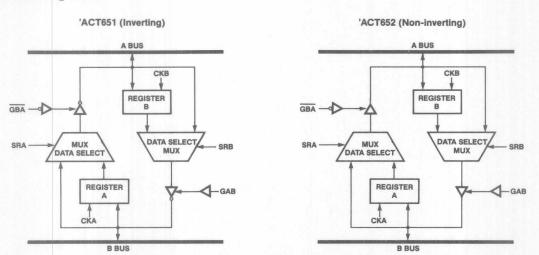
'ACT652 (Non-Inverting)



IEEE Symbols



Block Diagrams



13

Function Table

Function Table Nomenclature Description

GAB: To enable A-to-B operation.

GBA: To enable B-to-A operation.

GAB	GBA	OPERATION DIRECTION
L	ıL .	B-to-A
L	Н	A and B buses both are inputs (Storage)
Н	_s L	A and B buses both are outputs (Transfer stored data to bus)
Н	Н	A-to-B

SRA/SRB: To select the output data coming from the A/B

register if SRA/SRB is a High level; otherwise,

directly from the input data bus.

A0-A7: Eight input/output pins on the A side.

B0-B7: Eight input/output pins on the B side.

CKA/CKB: Clock for register A/B.

X: H or L state irrelevant ("Don't Care" condition).

Positive edge of CK causes clocking, if clock enable

is asserted.

UC: H or L or ↓ case (nonclocked operation).

RGTR: Register.

1:

Bus Operation for 'ACT651

OPERATION	BET 1	CON	TROL		DAT	A I/O	BLOCK DIAGRAM	1 1 30 30 30 30	BLE	'ACT651 GITARBA
	GAB	GBA	SRA	SRB	A0-A7	B0-B7	78-08	СКА	СКВ	GAB GBA SHA GF
		aciti	Te do	014 0	0 00		A	UC	UC	No operation
	Bb s	BAB	nei la	aR -	E pu		BUS RGTR	UC	1	Real time A bus data → RGTR E
Storage	L	Н	X	X	Input	Input	RGTR B B	T Tall	UC	Real time B bus data → RGTR A
	eh a au d	d As		617 60		AND	CKB CKA	t	1	Real time A bus data → RGTR B Real time B bus data → RGTR A
Maura - a	lab a	od Ba	egas le	B C	U-100			UC	UC	Real time B bus data → A bus
Real time	rest es	d 3 e	mi) le	66 68	00		A BUS RGTR	UC	1	Real time $\overline{\underline{B}}$ bus data \rightarrow A bus Real time $\overline{\underline{B}}$ bus data \rightarrow RGTR $\overline{\underline{B}}$
B-to-A	L	L	L	X	Output	Input	RGTR B	fitgi	UC	Real time B bus data → A bus Real time B bus data → RGTR A
Operation			201	He He He		200	CKB CKA	t	t	Real time B bus data → A bus Real time B bus data → RGTR A Real time B bus data → RGTR B
Est in him	rai-	airb	NATI	pri :	u ou			UC	UC	RGTR Ā data → A bus
Stored data	A -	niah stab	東京 第5万):H):H	pu	-	BUS	UC	t	RGTR Ā data → A bus RGTR Ā data → RGTR B
B-to-A	L	L	Н	X	Output	3'1	RGTR B B BUS	lites	UC	Real time B bus data → RGTR A
Operation	8b 16 A - 1内 -	ateb	A HT	98 98 98		ASSO	скв ска	t	1	Real time B bus data → RGTR / RGTR Ā data → A bus RGTR Ā data → RGTR B
eud 8 e	BO P	nd A	emit le	BHI (10 1013			UC	UC	Real time A bus data → B bus
Real time	a dall	od A.s	enti is enti is	oFi oFi	1 30		A BUS RGTR A	UC	1	Real time \overline{A} bus data \rightarrow B bus Real time A bus data \rightarrow RGTR I
A-to-B	Н	Н	Х	L	Input	Output	RGTR B	tuc	UC	Real time \overline{A} bus data \rightarrow B bus Real time \overline{A} bus data \rightarrow RGTR
Operation	ust t ust t	da ISA IO∤	eni is Spirie Smil L	Rd 原用 上で		2500 A350	CKB CKA	t	t	Real time \overline{A} bus data \rightarrow B bus Real time \overline{A} bus data \rightarrow RGTR \overline{A} Real time A bus data \rightarrow RGTR \overline{A}
90	8	- Atah	ant	bs.	W DU			UC	UC	RGTR B data → B bus
Stored data	into a	od A :	ent i	68) 148)	r 60		A BUS RGTR A	UC	t	Real time A bus data → RGTR I RGTR B data → B bus
A-to-B	Н	Н	X	Н	Input	Output	RGTR	tus	UC	RGTR B data → B bus RGTR B data → RGTR A
Operation	dab - da - loar -	ad / State 675.1	9 FT B	09 09		8010 8010	CKB BUS	t	t	Real time A bus data → RGTR I RGTR B data → B bus RGTR B data → RGTR A
/B bus	4-1	lan d	YA FIT	DP I	U DO			UC	UC	RGTR Ā/Ē data → A/B bus
Transfer	8 - 8 8	B dol	ART		Figu	Ш	A BUS RGTR A	UC	1	RGTR Ā/B data → A/B bus RGTR Ā data → RGTR B
Stored	Н	L	Н	Н	Output	Output	RGTR B	719	UC	RGTR Ā/Ē data → A/B bus RGTR Ē data → RGTR A
Data	18-	att. h	ABI	08 08 08		ANG	CKB & CKA	t	1	RGTR Ā/B data → A/B bus RGTR Ā data → RGTR B RGTR B data → RGTR A

Bus Operation for 'ACT652

OPERATION	earo.	CON	TROL	100	DAT	A I/O	BLOCK DIAGRAM		BLE	ACT652
	GAB	GBA	SRA	SRB	A0-A7	B0-B7	78-00	CKA	СКВ	ORB GRA SRA SR
		neits	lecto i	41 3	u lau		A	UC	UC	No operation
	lab at	d A p	mit te	R	ou		BUS RGTR	UC	1	Real time A bus data → RGTR
Storage	all as	Н	X	X	Input	Input	RGTR B	119	UC	Real time B bus data → RGTR
	sb au	d A e	only in	IR IR		880 l	CKB CKA	1	1	Real time A bus data → RGTR Real time B bus data → RGTR
aus A — s	sp se	d d s	failt vs	184 3	ย่อแ			UC	UC	Real time B bus data → A bus
Real time	ab a.	d S e	mil le mil le	9.	ou		A BUS RGTR A	UC	t	Real time B bus data → A bus Real time B bus data → RGTR
B-to-A	L		L	Х	Output	Input	RGTR	ntqii	UC	Real time B bus data → A bus Real time B bus data → RGTR
Operation		d E s d E s	end e ond s ond s	6A 6A 6A		Bare Ceci	CKB CKA	t	1	Real time B bus data → A bus Real time B bus data → RGTR Real time B bus data → RGTR
811	s A-	siab	A BY	MR C	บ วบ			UC	UC	RGTR A data → A bus
Stored data	e A F	elso sieti	A ST	IR IR	50	1	BUS RGTR	UC	t	RGTR A data → A bus RGTR A data → RGTR B
B-to-A	L	8 8 8	Н	X	Output	Input	RGTR B B	htgt	UC	Real time B bus data → RGTR RGTR A data → A bus
Operation	isbai - At	id S s ereb steb	oid is A sta A sta	9위 9위 9위	T T	AUS AUS	CKB CKA	1	1	Real time B bus data → RGTR RGTR A data → A bus RGTR A data → RGTR B
god 8 s	lab a	dĀe	etit la	9F 3	u au			UC	UC	Real time A bus data → B bus
Real time	teb ei		erriz lis erriz lis		pu	ar	A BUS RGTR A	UC	1	Real time A bus data → B bus Real time A bus data → RGTR
A-to-B	Н	Н	X	L	Input	Output	RGTR	tug	UC	Real time A bus data → B bus Real time A bus data → RGTR
Operation		d A s	end la end le end la			670	CKB CKA	1	1	Real time A bus data — B bus Real time A bus data — RGTR Real time A bus data — RGTR
	da-	atab	i an	OF S	u bu			UC	UC	RGTR B data → B bus
Stored data	tab si d Q -	d Ace	ere 16 B 20	sR on	: 04	1 -	A BUS RGTR	UC	1	Real time A bus data → RGTR RGTR B data → B bus
A-to-B	Н	Н	X	Н	Input	Output	RGTR B B BUS	1.mg	uc	RGTR B data → B bus RGTR B data → RGTR A
Operation	15 0 a) 4 5 b - 80	d A s sisb sisb		18 18 18		KHS	скв ска	1	1	Real time A bus data → RGTR RGTR B data → B bus RGTR B data → RGTR A
aud 65	4 - a	so B	E et	bal :	u bu			UC	UC	RGTR A/B data → A/B bus
Transfer	0.9	ati B	AT A ST)R (8)	SU		BUS RGTR	uc	t	RGTR A/B data → A/B bus RGTR A data → RGTR B
Stored	Н	L	Н	Н	Output	Output		itgi	UC	RGTR A/B data — A/B bus RGTR B data — RGTR A
Data	N - 4 DR - BR -	50 T 8750 8760		IS IS		170	CKB CKA	1	1	RGTR A/B data — A/B bus RGTR A data — RGTR B RGTR B data — RGTR A

Supply voltage, V _{CC} DC input voltage, V _I DC output voltage, V _O				0.5	V to 7.0 V
DC input voltage, V ₁		AMOITHOUGH TAR	f	0.5 V to Vc	C +0.5 V
DC output voltage, VO				0.5 V to V	CC+0.5 V
DC output source/sink current per of	output pin, Io .				±35 mA
Input diode current, I _{IK} :	GND · · · · · ·			- Alghrava voor sveridgie	± 100 mA
V _I <0			. Mag r. Mar.	ters van hegel	-20 mA
Output diode current, lov:					
V _O <0				il. overlavet output valtege	-20 mA
Storage temperature		ADEST = JOI		65 to	o +150°C
			VCC = MIN		
Operating Conditions			MIN = MA		

SYMBOL	01±	PARAMETER GMO TO GOV =	MIN	COMMERCIAL MAX	UNIT	
Vcc	Supply voltage			4.5	5 here (aneceps) 5.5	V
TA	Operating free-air tem	perature		-40	85	°C
	Middle of alcole	High	High			ns
tw	Width of clock	Low		20		
t _{su}	Set up time	S COMMERCIAL	иотпако	251	997 30 A A A A A A A A A A A A A A A A A A	ns
t _h	Hold time	L KAM MIN	(/avetoms)	Ot		ns
tr	Input rise time at V _I =	4.5 V		0	500	ns
t _f	Input fall time at V _I = 4.5 V				500 Data to output delay	ns
ГОН	High-level output current				-6	mA
loL	Low-level output curre	ent			yaleb fugitio ci blociO 12	mA

1 The a	rrow indicates the Low-to	-High transition of the clock input used as reference	э.	Select to output delay*	
	00 SE				
				CBA to A bus	
				valab sidseth fuque	
				GAB to 8 bus	
				output disable datay	

SYMBOL	PARAMETER		TEST CONDITIONS	25°C MIN TYP MAX	COMMERCIAL MIN TYP MAX	UNIT	
VIL	Low-level input voltage	Company Company	olah	0.8	8.0 Maie/source 0.8	V	
VIH	High-level input voltage	**********		2	2 manus abo	V	
IIN	Input current	VCC = MAX	VI = VCC or GND	±1.0	±1.0	μΑ	
#157	Low-level output voltage		VCC = MIN	I _{OL} = 20 μA	0.1	0.1	turatura
VOL		VIL = MAX	IO = 6 mA	0.32	0.37	V	
	* 1 * 1 * 1 * 1 * 1 * 1 * 1 * 1 * 1 * 1	VIH = MIN	I _{OL} = 12 mA	0.4	0.4	onsok	
	I link Investment	VCC = MIN	IOH = -20 μA	3.4	3.4		
V _{OH} Hi	High-level output voltage	V _{IL} = MAX V _{IH} = MIN	IOH = -6 mA	2.4	2.4	V	
loz	Off-state output current	VCC = MAX	VO = VCC or GND	±10	±30	μΑ	
lcc*	Quiescent supply current	VCC = MAX	V _I = V _{CC} or GND	10	40	μА	

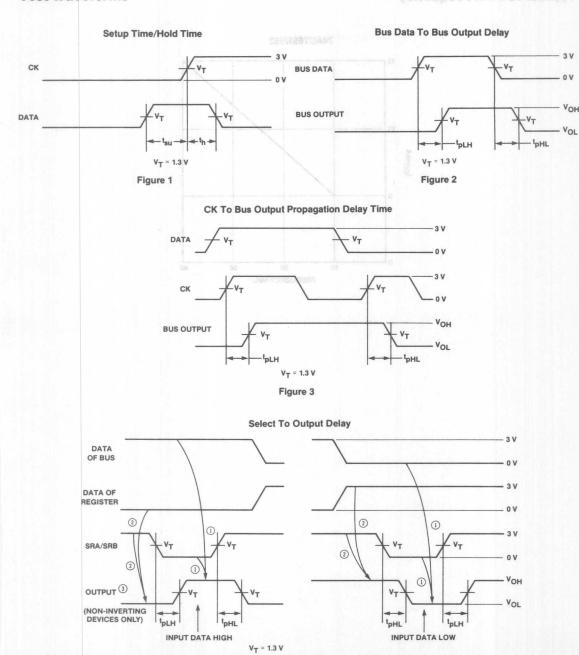
^{*} See ICC vs. Frequency chart.

Switching Characteristics

SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load/Waveform)	COMMERCIAL T _A = 25°C MIN MAX	COMMERCIAL MAX	UNIT
tPLH	Data ta a da dala	9	39	48	N.
tPHL	Data to output delay	0	35	42	ns
tPLH	Clock to cutout dolou		35	termo lucino levernosti 44	HOT
t _{PHL}	Clock to output delay	C ₁ = 50 pF	35	40	ns
^t PLH	Select to output delay*	o_ oop.	preter as block highli south a 32	nuclears nells-or and all research 40	tis eri7
^t PHL	(data input high)		32	40	ns
^t PLH	Select to output delay*		35	44	200
^t PHL	(data input low)	32	36	ns	
^t PZL	GBA to A bus		28	32	
^t PZH	output enable delay		28	32	ns
t _{PLZ}	GBA to A bus		28	32	ns
^t PHZ	output disable delay	$R_L = 1K\Omega$	35	38	ns
t _{PZL}	GAB to B bus	C _L = 50 pF	30	33	
^t PZH	output enable delay		28	32	ns
t _{PLZ}	GAB to B bus		28	32	-
tPHZ	output disable delay		35	38	ns

^{*} See Figure 4.

Test Waveforms

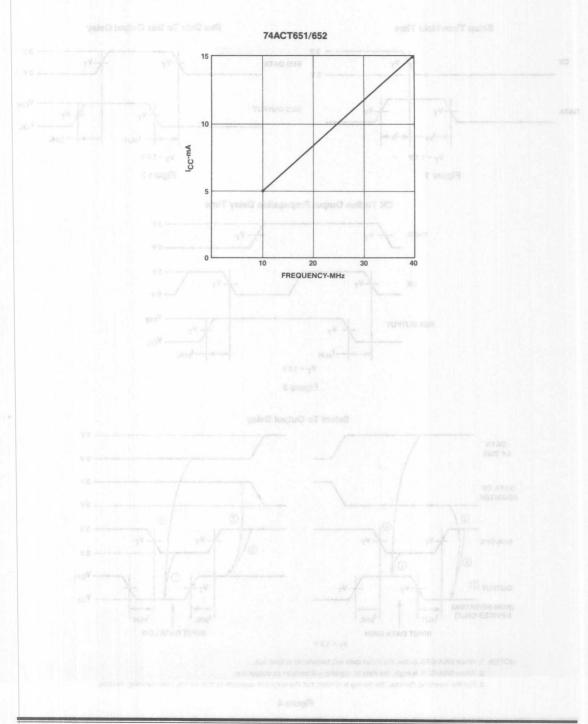


- NOTES: 1. When SRA/SRB is low, the input data will transfer to output bus.
 - 2. When SRA/SRB is high, the data of register will transfer to output bus.
 - 3. For the inverting devices, the timing is similar, but the output is opposite to that for the non-inverting devices.

Figure 4

VOH

Typical ICC vs. Frequency



Enable/Disable/Direction-Change Delay

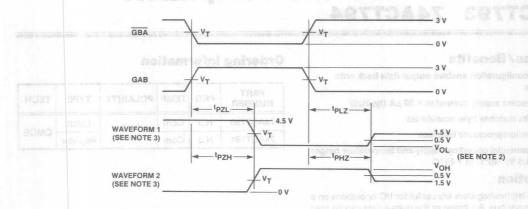
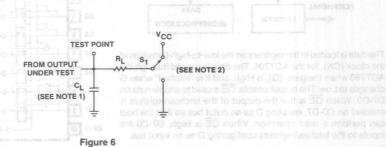


Figure 5

Standard Test Load



72

- NOTES 1. CL includes probe and jig capacitance.
 - 2. When measuring tpLz and tpzL, S1 is tied to VCC. When measuring tpHz and tpzH, S1 is tied to ground.
 - When measuring propagation delay times of three-state outputs, S_1 is open, i.e., not connected to V_{CC} or ground.
 - Waveform 1 is for an output with internal conditions such that the output is Low except when disabled by the output control.
 - Waveform 2 is for an output with internal conditions such that the output is High except when disabled by the output control.
 - 4. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
 - 5. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $t_r \leq$ 6 ns, $t_f \leq$ 6 ns, $z_{out} =$ 50 Ω .

13

ACTT93 Function Table

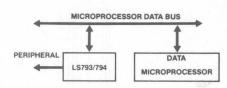
8-Bit Latches/Registers with Readback-Advanced CMOS-TTL Compatible 74ACT793 74ACT794

Features/Benefits

- I/O port configuration enables output data back onto input bus
- Low quiescent supply current of < 10 μA (typical)
- · Eighth bits matches byte boundaries
- Ideal for microprocessor interface
- Wide commercial operating supply and temperature ranges 4.5 V to 5.5 V; -40°C to + 85°C

Description

These 8-bit latches/registers are useful for I/O operations on a microprocessor bus. An image of the output data can be read back by the CPU. This operation is important in control algorithms which make decisions based on the previous status of output controls. Rather than storing a redundant copy of the output data in memory, simply reading the register as an I/O port allows the data to be retrieved from where it has been stored in an ACT793/4, for verification and/or updating.



The data is loaded in the registers on the low-to-high transition of the clock (CK), for the ACT794. The data is passed through the ACT793 when the gate, (G), is High, and it is "latched" when G changes to Low. The output enable, \overline{OE} is used to enable data on D7-D0. When \overline{OE} is low the output of the latches/registers is enabled on D0-D7, enabling D as an outut bus so that the host can perform a read operation. When \overline{OE} is High, D7-D0 are inputs to the latches/registers configuring D as an input bus.

The output drive of these commercial parts for any output pin is $I_{\rm OL}$ = 12 mA.

ACT793 Function Table

G	ŌE	Q	D
L	L	Q ₀ **	Output, Q
L	Н	Q ₀ **	Input
H [†]	L	D*	Output, Q*
Н	Н	D	Input

^{*} In this case the output of the latch feeds the input, and a "race" condition results.

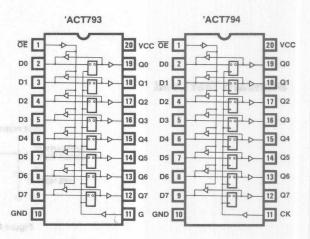
** Q₀ represents the previous "latched" state.

† This transition is not a normal mode of operation and may produce hazards

Ordering Information

PART NUMBER	PKG	TEMP	POLARITY	TYPE	TECH
74ACT793	N,J	Com	Non-	Latch	01100
74ACT794	N,J	Com	invert	Register	CMOS

Logic Symbols



'ACT794 Function Table

CK	ŌE	Q	D
LorHor	L	Q ₀	Output, Q
LorHor	Н	Q ₀	Input
1 Servery	and Lorente	Q ₀	Output, Q*
ustra bi cara 1.4	had the Heat rest	D D	Input

^{*} In this case the output of the register is clocked to the inputs and the overall O output is unchanged at Q₀.

TWX: 910-338-2376 2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2374 Monolithic MM Memories

Supply voltage, VCC	0.5 V to 7.0 V
DC input voltage, V _I	0.5 V to V _{CC} +0.5 V
DC output voltage, VO	-0.5 V to VCC +0.5 V
DC output source/sink current per output pin, IO	±35 mA
DC VCC or ground current, ICC or IGND	±100 mA
Input diode current, I _{IK} :	
V ₁ <0	20 mA
V >VCC	+20 mA
Output diode current, IOK:	
V _O <0	–20 mA
VO >VCC	+20 mA
Storage temperature	65° C to +150° C

Operating Conditions

SYMBOL	PARAMETER MIN Supply voltage 4.5		MIN	COMMERCIAL TYP	MAX	UNIT	
V _{CC}			4.5 5		V		
TA	Operating free-air temperature	mperature		Contract of the same of the same of	85	°C	
t _W Width of Clock/Gate		High	15	FETEMARAR	1.40	UPIAS	
t _W Width of Clock/Gate	Width of Clock/Gate	Low	15		adjese	ns	
t Setup time		'ACT793	81	Clock to output detay	-	E STATE	
t _{su}	Setup time	'ACT794	251			IH9 ³	
an -		'ACT793	81	Outgut enable delay		ns	
t _h 00	Hold time	'ACT794	Ot			129	
tr	Input rise time at V _I = 4.5 V		0	yelsb eldsab signiiO	500	ns	
tf	Input fall time at V _I = 4.5 V		0		500	ns	
IOH	High-level output current				-6	mA	
loL	Low-level output current				12	mA	

¹ The arrows indicates the transition of the clock/gate input used for reference. 1 for the low-to-high transitions, 1 for the high-to-low transitions.

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		MIN TYP	MAX	UNIT
VIL	Low-level input voltage	4	ALCOHOL STATE		0.8	V
VIH	High-level input voltage	(0)	-v-X	2		V
IN	Input current	V _{CC} = MAX	V _I = V _{CC} or GND		±1.0	μΑ
	Low-level output voltage	VIH = MIN	Ι _{ΟL} = 20 μΑ	0-0	0.1	V
VOL			I _{OL} = 6 mA	of the self-figure of event and the late	0.37	
			I _{OL} = 12 mA		0.4	
	Liber terretor de la lace	VCC = MIN	IOH = -20 μA	3.4		
VOH	High-level output voltage	V _{IL} = MAX V _{IH} = MIN	I _{OH} = -6 mA	2.4		V
loz	Off-state output current	V _{CC} = MAX	VO = VCC or GND		±30	μΑ
Icc	Quiescent supply current	V _{CC} = MAX	V _I = V _{CC} or GND		80	μΑ

Switching Characteristics for 'ACT793

SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load/Waveform)	MIN COMMERCIAL MAX	UNIT
t _{PLH}		(4.4	Ol niq fuqtuo req the rusu ilnimatruo 40	giuo O
tPHL	Data to output delay	0 - 50 - 5	40	ns
tPLH	Cata to quitout dalay	C _L = 50 pF	40	v ns
t _{PHL}	Gate to output delay		40	Tugtu
t _{PZL}	Output enable delay†		30	ns
t _{PZH}	Output enable delay	R _L = 1 K Ω	30	BOSTO
t _{PLZ}	Output disable delay†	C _L = 50 pF	33	ns
t _{PHZ}	Output disable delay		33	115

[†] For the 'ACT793, G should remain LOW during these tests.

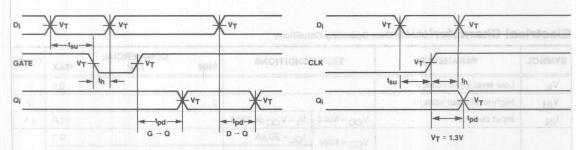
Switching Characteristics for 'ACT794

		DE-1						
SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load/Waveform)	MIN COMMERCIAL MAX	UNIT				
tPLH Clock to output delay		0 - 50 - 5	40					
t _{PHL}	Clock to output delay	C _L = 50 pF	emit gutse 40	ns				
t _{PZL}	Output enable delay	ACT783 RI	30	ns				
^t PZH	Output enable delay	R _L = 1 K Ω	emit blott 30	113				
t _{PLZ}	Output disable delay	C _L = 50 pF	30	ns				
t _{PHZ}	Output disable delay		30	115				

'ACT793 Timing Diagrams

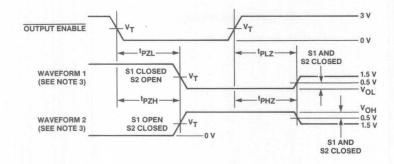
'ACT794 Timing Diagrams

Absolute Maximum Ratings

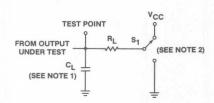


The case when gate is HIGH and data flows through the part is specified as Data to Output delay in the Switching Characteristics table. (V_T = 1.3V).

Enable/Disable Waveforms



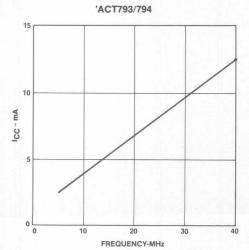
Standard Test Load



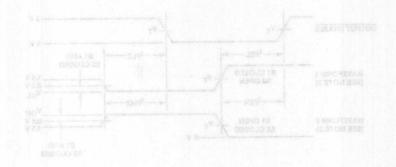
Notes 1. C_L includes probbe and jig capacitance.

- 2. When measuring tp_Z and tpZL, S1 is tied to VCC. When measuring tpHZ and tpZH, S1 is tied to ground.
 - When measuring propagation delay times of three-state outputs, $\rm S_1$ is open, i.e., not connected to $\rm V_{CC}$ or ground.
- Waveform 1 is for an output with internal conditions such that the output is Low except when disabled by the output control.
 - Waveform 2 is for an output with internal conditions such that the output is High except when disabled by the output control.
- 4. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
- 5. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $t_{f} \leq$ 5 ns, $t_{f} \leq$ 6 ns, Z_{OUt} = 50 Ω .

Typical I_{CC} vs Frequency







Standard Test Load

Notice 1 '0; inchicas probbs and liq ourselfance

2 Is lies to pround.

The Household Grandship mana

Autoritation 1 is for the crubing equiverse coughtous may see that the principle is 1 in

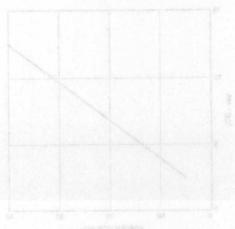
Waveform 2 is for an oblique with homeun conditions such that one conjust is your except use

A. In the manufact above, the cites a stationarials and public and cultural take poet.

\$ All about palear are standard by genomers tending the full owing already restrict PRR = 1 and 1 and 2 and 3 are 6 and 2 and 2 and 3 and

Typical top vs Prequency

PRINCELLOY





Introduction Military Products Division **PROM** PLE™ Devices **PAL®** Devices HAL®/ZHAL™ Devices System Building Blocks/HMSI™ **FIFO Memory Support** Arithmetic Elements and Logic 10 Multipliers 8-Bit Interface **Double-Density PLUS™ Interface** ECL10KH 14 Logic Cell Array **General Information Advance Information Package Drawings** Representatives/Distributors

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MC10H106	Triple 4-3-3 Input NOR Gate	14-15		with Enable	14-50
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	OR-AND-INVERT Gate	14-25	MC10H174	Dual 4-to-1 Multiplexer	14-66
MC10H118	Dual 2-Wide 3-Input OR-AND Gate .	14-27	MC10H175	Quint Latch	14-68
MC10H119	4-Wide 4-3-3-3 Input OR-AND		MC10H176	Hex D Master-Slave Flip-Flop	14-70
	Gate	14-29	MC10H179	Look-Ahead Carry Block	14-72
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Maria Contract	Gate	14-31	MC10H210	3-Input, 3-Output OR/NOR Gates	14-77
			MC10H211	3-Input, 3-Output OR/NOR Gates	14-77

ECL10KH Selection Guide

DEVICE	FUNCTION	PACKAGE	PINS
	NOR Gate	and the same of	WHEN SEED A
MC10H102	Quad 2-Input	SPARSON & TT.	· 第 5 日本代本 「
MC10H211	Dual 3-Input, 3-Output		Account to the second of the second
	OR Gate		and the second
MC10H103	Quad 2-Input		Fedition/Con
MC10H210	Dual 3-Input, 3-Output		denoupait galtinood 1
1800	AND Gates		* Power distribution 5
MC10H104	Quad AND	N. V.	Fioles margin 150 c
	Complex Gates	21	Voltego ecorpersati
MC10H101	Quad OR/NOR		ECL 10K-compails
MC10H105	Triple 2-3-2 Input OR/NOR		mailtoireasso
MC10H107	Triple Exclusive OR/NOR	n or with each tokens, it	of a standardated
MC10H109	Dual 4-5 Input OR/NOR	anie pain i ratou	yushid no Asidaba
MC10H117	Dual 2-Wide OR-AND/OR-AND Invert	OL 10KH Ismily, to	
MC10H118	Dual 2-Wide 3-Input OR/AND	n, rounting, and	denavace lo redumin
MC10H121	4-Wide OR-AND/OR-AND Invert		Leg Multiple Strategie
	Translators		
MC10H124	Quad TTL/ECL	400	anughted als
MC10H125	Quad ECL/TTL		
L. O. ct W faller an	Receivers	STUHOTON	
MC10H115	Quad Line Receiver	-bli Sinary Counter-	
MC10H116	Triple Line Receiver		I pox
	Flip-FLop Latches	J, N	16
MC10H130	Dual latch		
MC10H131	Dual D Master Slave Flip-FLop		100
MC10H175	Quint Latch		37
MC10H176	Hex D-Flip-Flop		738
	Parity Checker		1 100
MC10H160	12-Bit Parity Generator-Checker		
	Encoders/Decodes		
MC10H161	Binary to 1-8 (Low)		lav de la
MC10H162	Binary to 1-8 (High)	Engrandamental conf	
	Data Selector Multiplexer		
MC10H158	Quad 2-Input Multiplexers (Non-inverting)	MCSSSOIG	
MC10H159	Quad 2-Input Multiplexers (Inverting)	CHARLES TO E	
MC10H164	8-Line Multiplexer	SE STRUCK ON STRUCK IN	
MC10H173	Quad 2-Input Multiplexer Latch		
MC10H174	Dual 4-1 multiplexer		refinition to the second
	Counters	71G-A	lateral prompt
MC10H016	Binary Counter	FRAME RETRICO	
MC10H136	Universal Hexadecimal		
	Arithmetic Functions		E[3]
MC10H179	Lookahead Carry Block	SH PR DM SSV OF	
CHRONIC DOLLEG - BIN O	Special Functions	TO BUILD WITH	
MC10H141	Universal Shift Register		
MC10H166	5-Bit Magnitude Comparator	1	

ECL 1010H High-Speed

ECL 10KH High-Speed Emitter-Coupled Logic Family MC10H016 **4-Bit Binary Counter**

Features/Benefits

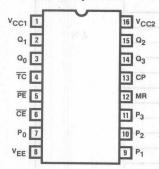
- Counting frequency, 200 MHz min.
- Power dissipation 570 mW typical
- Noise margin 150 mV
- Voltage compensated
- ECL 10K-compatible

Description

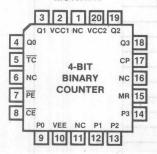
The MC10H016 is a high-speed synchronous, presettable, cascadable 4-bit Binary Counter. This device is a member of Monolithic Memories' new ECL 10KH family. It is useful for a large number of conversion, counting, and digital integration applications.

Pin Configuration

MC10H016 4-bit Binary Counter



MC10H016



Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
MC10H016	J, N, NL	Com

Function Select Table

CE	PE	MR	CP	FUNCTION
L	L	L 85	Z	Load parallel (P _n to Q _n)
Н	L	elen	Z	Load parallel (Pn to Qn)
L	Н	L	Z	Count
Н	Н	L	Z	Hold
X	X	L	ZZ	Masters respond; slaves hold
X	X	ηН	X	Reset (Q _n = LOW, T _C = HIGH)

Z = Clock Pulse (Low to High)

ZZ = Clock Pulse (High to Low).

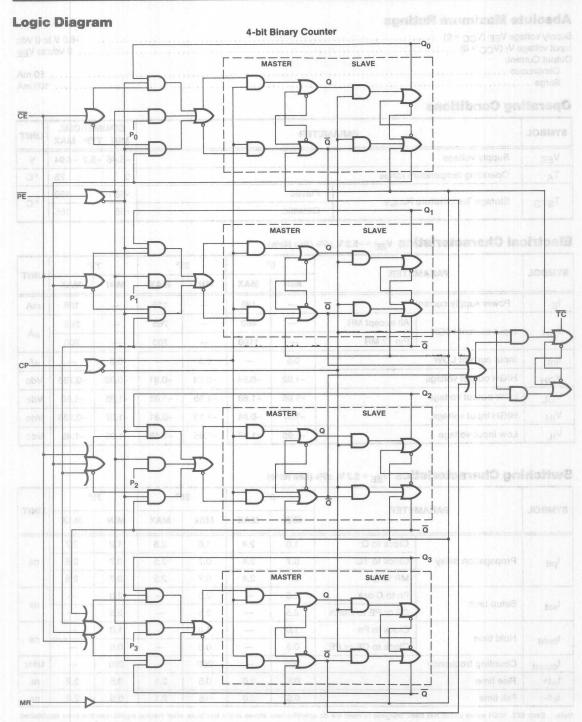
Features include assertion inputs and outputs on each of the four master/slave counting flip-flops. Terminal count is generated internally in a manner that allows synchronous loading at nearly the speed of the basic counter.

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Note: This diagram is provided for understanding of logic operation only. It should not be used for evaluation of propagation delays as many gate functions are achieved internally without incurring a full gate delay.

	0)		
Input voltage V _I (V _{CC} = 0)		 	0 Vdc to VEE
Output Current:			
			50 mA
Surge		 	100 mA

Operating Conditions

SYMBOL	PARAMETER			COMM MIN TY	ERCIAL P MAX	UNIT
VEE	Supply voltage	The state of the s		-5.46 -5	5.2 -4.94	V
TA	Operating temperature range			0	75	°C
т.	Ctorage Tomporeture Dance	Plastic		-55	150	°C
STG	Storage Temperature Range	Ceramic		-55	165	

Electrical Characteristics V_{EE} = -5.2 V ±5% (See Note)

CVMDOI	DADA		C)0	2	5°	7	5°	mA μA
SYMBOL	PARA	METER	MIN	MAX	MIN	MAX	MIN	MAX	UNI
I _E	Power supply current		استوام	126	184	115	114	126	mA
1	I + + I II O I I	All except MR	No12-7	450	-	265	11-	265	
linH	Input current HIGH	Pin 12 MR		1190	_	700		700	
linL	Input current LOW		0.5	- 4-	0.5	- 10	0.3	$\gamma = 1$	μΑ
VOH	HIGH output voltage		-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
VOL	LOW output voltage		-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
V _{IH}	HIGH input voltage	SEVAR.	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
VIL	Low input voltage		-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

Switching Characteristics V_{EE} = 5.2 V, $\pm 5\%$ (See Note)

			()°	2	5°	7	5°	ns ns
SYMBOL	PARA	METER	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
		Clock to Q	1.0	2.4	1.0	2.5	1.0	2.7	
t _{pd}	Propagation delay	Clock to TC	0.7	2.4	0.7	2.5	0.7	2.6	ns
		MR to Q	0.7	2.4	0.7	2.5	0.7	2.6	
		Pn to Clock	2.0	-(3-7	2.0		2.0	-	ne
^T set	Setup time	CE or PE to Clock	2.5	- 1	2.5	-	2.5	(-1	ns
	11-14-1	Clock to Pn	1.0	-	1.0		1.0	1	1
^t hold	Hold time	Clock to CE or PE	0.5	-	0.5	-	0.5	15-	ns
fcount	Counting frequency		200	-(200		200	_	MHz
t _r ,t+	Rise time		0.5	2.0	0.5	2.1	0.5	2.2	ns
t _f ,t-	Fall time		0.5	2.0	0.5	2.1	0.5	2.2	ns

Note: Each ECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50 \(\Omega resistor to -2.0 \(V \).

ECL 10KH High Speed Emitter Coupled Logic Family MC10H100 Quad 2-Input NOR Gate with Strobe

Features/Benefits **Ordering Information** · Propagation delay, 1 ns typical PART NUMBER PACKAGE TEMPERATURE · 25 mW typical/gate (no load) MC10H100 J. N. NL Com Noise margin 150 mV Voltage compensated ECL 10K-compatible Description **Logic Diagram** The M10H100 is a member of Monolithic Memories' ECL 10KH family. This ECL device is a Quad 2-Input NOR Gate with Strobe. MC10H100 This device is a functional/pinout duplication of the standard ECL 10K family part, with 100% improvement in propagation Aout delay and no increase in power supply current. AIN DIN EIN EIN **Pin Configuration** 2 = 4 + 5 + 9 | 1 | 100 | 100 | 100 | VCC1 = PIN 1 VCC2 = PIN 16 VEE = PIN 8 MC10H100 Quad 2-Input NOR Gate with Strobe MC10H100 16 V_{CC2} 3 2 1 20 19 V_{CC1} 1 15 E_{OUT} A_{OUT} 2 4 BOUT DOUT 18 14 POUT BOUT 3 ECL10KH 5 AIN EIN 17 QUAD 13 E_{IN} AIN 4 6 2-INPUT NC NC 16 NOR GATE 12 E_{IN} AIN 5 AIN WITH STROBE DIN 15 11 DIN B_{IN} 6 8 BIN 10 D_{IN} BIN VEE NC C DIN B_{IN} 7 9 10 11 12 13 9 C VEE 8

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Absolute illeviment Patings

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MMI

Supply voltage VEE (VCC = 0) Input voltage VI (VCC = 0)	-8.0 V to 0 V _{dc}
Output current:	
Continuous	50 mA
Surge	100 mA

Operating Conditions

SYMBOL	DOTAL PA	COMM MIN TY	UNIT			
VEE	Supply voltage			-5.46 -5.20 -4.94		
TA	Operating temperature range		0	75	°C	
_	nusvaenik	Plastic	-55	150	0.0	
TSTG	Storage temperature range	Ceramic HMOT 1033 kernomaka olimboros	-55	-55 165	°C	

Electrical Characteristics V_{EE} = -5.2 V ±5% (See Note)

OVMDOL	TUDO I DADAME		0	0	2	5°	7	5°	
SYMBOL	PARAME	TER TERM	MIN	MAX	MIN	MAX	MIN	MAX	UNI
IE Power supply current		12 100		29		26	-	29	mA
	In a standard I II CI I	Pin 9	-	900	_	560	Lance Andrews	560	^
linH	Input current HIGH	All other pins	_	500	-	310	_	310	μΑ
linL	Input current LOW	Input current LOW		-	0.5	_	0.3	-	μΑ
Vон	HIGH output voltage		-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdd
VOL	LOW output voltage		-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdd
VIH	HIGH input voltage		-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdd
VIL	LOW input voltage		-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdd

Switching Characteristics V_{EE} = -5.2 V ±5% (See Note)

CVIADOI	THE STANDARD	257 (8)	0	0	2	5°	7:	5°	
SYMBOL	PARAM	ETER	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
t _{pd}	December dela	Pin 9	0.65	1.6	0.7	1.7	0.7	1.8	
	Propagation delay	All other pins	0.4	1.3	0.45	1.35	0.5	1.5	ns
tr	Rise time (20%-80%)		0.5	2.0	0.5	2.1	0.5	2.2	ns
tf	Fall time (80%-20%)		0.5	2.0	0.5	2.1	0.5	2.2	ns

Note: Each ECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-Ω resistor to -2.0 V.

ECL10KH High-Speed Emitter-Coupled Logic Family MC10H101 Quad OR/NOR Gate

Features/Benefits

- Propagation delay, 1 ns typical
- Power dissipation 25 mW/gate
- Noise margin 150 mV
- Voltage compensated
- ECL 10K-compatible.

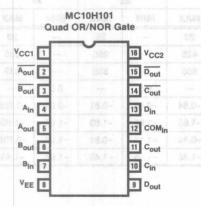
Ordering Information

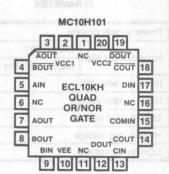
PART NUMBER	PACKAGE	TEMPERATURE
MC10H101	J,N,NL(20)	Com

Description

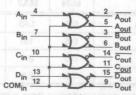
The MC10H101 is a member of Monolithic Memories' ECL family. This ECL 10KH part is a functional/pinout duplication of the standard ECL 10K family part, with 100% improvement in propagation delay, and no increase in power-supply current.

Pin Configurations





MC10H101 Quad OR/NOR Gate



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Monolithic Memorles



· Propagation delay, 1 na typical

Operating Conditions

SYMBOL		PARAMETER	COMME MIN TY		UNIT
VEE	Supply voltage		-5.46 -5	2 -4.94	٧
TA	Operating temperature range		0	75	°C
_	Characa hamanahan anan	Plastic	-55	150	00
TSTG	Storage temperature range	Ceramic Cerami	-55	165	°C

Electrical Characteristics V_{EE} = -5.2 V ± 5% (See Note)

SYMBOL	DAL	RAMETER	0	0	2	5°	7	5°	UNIT
STMBUL	PAI	NAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNI
I _E	Power supply curre	ent		29		26	all and the later of	29	mA
	In and allowed blake	MC10H101	-	425	200 ¹⁰ [1]	265	-0	265	
linH	nH Input current high	MC10H101 (Pin 12 only)	-	850	100 E [11]	535	-[3]	535	μΑ
linL	Input current LOW	nput current LOW		_	0.5	-	0.3	500 B	μΑ
VOH	HIGH output volta	ge on a	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
VOL	LOW output voltage	ge Tuox T	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
VIH	HIGH input voltag	e ruce(8)	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
VIL	LOW input voltage	HEV MIE	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

Switching Characteristics V_{FF} = -5.2 V, ±5% (See Note)

OVMOOL	21211	stati	300 307 7 0°suc		25°		75°		
SYMBOL	PARAMETER		MIN	MAX	MIN	MAX	MIN	MAX	UNIT
^t pd	Propagation delay	All others	0.5	1.45	0.5	1.5	0.5	1.6	ns
		12 Pin	0.5	1.6	0.5	1.6	0.5	1.7	
t _r , t+	Rise time	7.00	0.5	2.1	0.5	2.2	0.5	2.3	ns
t _f , t-	Fall time	1412 14 140 0 0	0.5	2.1	0.5	2.2	0.5	2.3	ns

Note: Each ECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50 Ω resistor to -2.0 V.

ECL 10KH High-Speed Emitter-Coupled Logic Family MC10H103 **Quad 2-Input OR Gate**

Features/Benefits

- · Propagation delay, 1.0 ns typical
- Power dissipation 25 mW/gate
- Noise margin 150 mV
- Voltage compensated
- ECL 10K compatible

Ordering Information

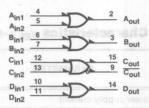
PART NUMBER	PACKAGE	TEMPERATURE
MC10H103	J,N,NL(20)	Com

Logic Diagram

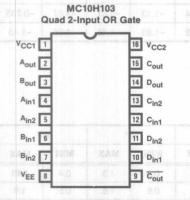
Description

The MC10H103 is a member of Monolithic Memories' ECL family. This ECL 10KH part is a functional/pinout duplication of the standard ECL 10K family part with 100% improvement in propagation delay, and no increase in power-supply current.

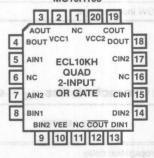
MC10H103 Quad 2-Input OR Gate



Pin Configurations



MC10H103



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14-11

Supply voltage V_{EE} (V_{CC} = 0) -8.0 V to 0 V_{dC} Input voltage V_I (V_{CC} = 0) ... 0 V_{dC} to V_{EE}

Output Current:

Continuous ... 50 mA

Operating Conditions

SYMBOL		PARAMETER	COMMERCIAL MIN TYP MAX	UNIT	
VEE	Supply voltage		-5.46 -5.2 -4.94	V	
TA	Operating temperature range		0 75	°C	
_	Ctarage tamparatura range	Plastic	-55 150		
STG	TSTG Storage temperature range Ceramic	Ceramic	-55 165	- °C	

Electrical Characteristics V_{EE} = -5.2 V ±5% (See Note)

SYMBOL	PARAMETER	0°		25°		75°		
	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNI
I _E	Power supply current	_	29	-	26	-	29	mA
linH	Input current HIGH		425	_	265	-	265	μΑ
linL	Input current LOW	0.5	_	0.5	_	0.3	_	μΑ
Vон	HIGH output voltage	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
VOL	LOW output voltage	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
V _{IH}	HIGH input voltage	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
VIL	LOW input voltage	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

Switching Characteristics V_{EE} = -5.2 V, ±5% (See Note)

SYMBOL	Parison on the Co.	0°		25°		75°		
	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
^t pd	Propagation delay	0.4	1.3	0.4	1.3	0.4	1.45	ns
t _r , t+	Rise time (20%-80%)	0.5	1.7	0.5	1.8	0.5	1.9	ns
t _f , t-	Fall time (80%-20%)	0.5	1.7	0.5	1.8	0.5	1.9	ns

Note: Each ECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50 Ω resistor to -2.0 V.

ECL 10KH High-Speed Emitter-Coupled Logic Family

MC10H102/Quad 2-Input NOR Gate MC10H105/Triple 2-3-2 Input OR/NOR Gate

Features/Benefits

- · Propagation delay, 1 ns typical
- Power dissipation 25 mW/gate
- Noise margin 150 mV
- Voltage compensated
- . ECL 10K compatible.

Description

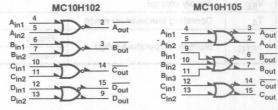
The MC10H102 and MC10H105 are members of Monolithic Memories new ECL family. These ECL 10KH parts are functional/pinout duplications of the standard ECL 10K family parts, with 100% improvement in propagation delay, and no increase in power-supply current.

Pin Configurations

Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
MC10H102	J,N,NL(20)	Home Conditions
MC10H105	J,IN,INL(20)	Com

Logic Diagrams



MC10H102

ECL10KH QUAD

2-INPUT NOR GATE

BIN2 VEE NC

4 BOUT VCC1

AIN1

NC

Quad 2-Input NOR Gate

5

6

8 BIN1

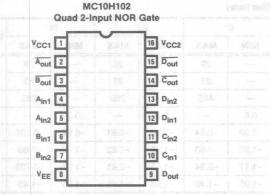
Triple 2-3-2 input OR/NOR Gate

18

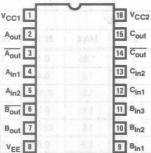
17

NC 16

DOUT CIN2

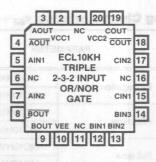


MC10H105 Triple 2-3-2 Input OR/NOR Gate



MC10H105

9 10 11 12 13



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14-13

mitter-Coupled Logic Family

Absolute Maximum Ratings

Supply vo	oltage V _{EE} (V _{CC} = 0)	-8.0 V to 0 V _{do}
Input volt	tage V _I (V _{CC} = 0)	0 Vac to VEE
Output C	Current:	
	nuous	
		100 mA

Operating Conditions

SYMBOL	0.000.000	PARAMETER			
VEE 201	Supply voltage	row.	-5.46 -5.2 -4.94	V	
TA	Operating temperature range	Part - A park	0 75	°C	
117	Oterana temperatura	Plastic planting of an ending the angular state and an ending the state of the stat	-55 bas \$150	°C	
314	Storage temperature range	Ceramic danoparuless area FACE ACE as	-55 165	anome	

Electrical Characteristics V_{EE} = -5.2V ± 5% (See Note)

SYMBOL	DADAMET	0°		0	25°			5°	UNIT
STMBUL	PARAMETER		MIN	MAX	MIN	MAX	MIN	MAX	UNIT
	A TOOK SOOK TOOK	MC10H102	_	29	Sund Light	26	- 1	29	
lE	Power supply current MC10H105	_	23	Fige 75 (2)	21	-0	23	mA	
linH	Input current HIGH	OM 0	_	425	South (FE)	265	-[7]	265	μΑ
linL	Input current LOW	aua[F]	0.5	-	0.5	-	0.3	- Ama	μΑ
VOH	HIGH output voltage	ния а	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
VOL	LOW output voltage	99	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
VIH	HIGH input voltage		-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
VIL	LOW input voltage		-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

Switching Characteristics V_{EE} = -5.2 V, ±5% (See Note)

CVMDOI	PARAMETER		0°		25°		75°		
SYMBOL			MIN	MAX	MIN	MAX	MIN	MAX	UNI
	seamant no list	MC10H102	0.4	1.25	0.4	1.25	0.4	1.4	
^t pd	Propagation delay	MC10H105	0.4	1.2	0.4	1.2	0.4	1.3	ns
t _r , t+ Rise time	Tallage III	MC10H102	0.5	1.5	0.5	1.6	0.55	1.7	
	Hise time	MC10H105	0.5	1.5	0.5	1.6	0.5	1.7	ns
t _f , t-	Fall time	MC10H102	0.5	1.5	0.5	1.6	0.55	1.7	ns
		MC10H105	0.5	1.5	0.5	1.6	0.5	1.7	

Note: Each ECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50 Ω resistor to -2.0 V.

ECL 10KH High Speed Emitter Coupled Logic Family MC10H106 Triple 4-3-3 Input NOR Gate

Features/Benefits

- · Propagation delay, 1 ns typical
- 36 mW typical/gate (no load)
- Noise margin 150 mV
- Voltage compensated
- ECL 10K-compatible

Ordering Information

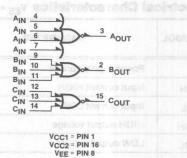
PART NUMBER	PACKAGE	TEMPERATURE		
MC10H106	J, N, NL	Com		

Description

The M10H106 is a member of Monolithic Memories' ECL 10KH family. This ECL device is a Triple 4-3-3 Input NOR Gate. This device is a functional/pinout duplication of the standard ECL 10K family part, with 100% improvement in propagation delay and no increase in power supply current.

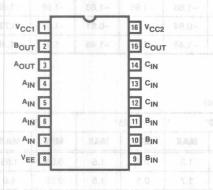
Logic Diagram

MC10H106

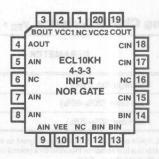


Pin Configuration

MC10H106 Triple 4-3-3 Input NOR Gate



MC10H106



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Monolithic MM Memories

Supply voltage V _{EE} (V _{CC} = 0) -8.0 V to 0 Input voltage V _I (V _{CC} = 0) 0 Vdc to Output current:	
Continuous 50) mA
Surge) mA

Operating Conditions

SYMBOL	D J JN N L 80	PARAMETER	COMMERC MIN TYP	MAX	UNIT
VEE	Supply voltage		-5.46 -5.20	-4.94	V
TA	Operating temperature range		0	75	°C
_	01	Plastic	-55	150	0.0
TSTG Storage temperature range	TSTG	Ceramic	-55	165	°C

Electrical Characteristics V_{EE} = -5.2 V ±5% (See Note)

Ordering Information

OVMBOL	e line a ma	0°		2	25° 75°			on bo
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
IE .	Power supply current		23	-	21		23	mA
linH	Input current HIGH		500	_	310	9 67% TV WP A	310	μΑ
linL	Input current LOW	0.5	_	0.5	_	0.3	_	μΑ
Vон	HIGH output voltage	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
VOL	LOW output voltage	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
VIH	HIGH input voltage	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
VIL	LOW input voltage	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

Switching Characteristics V_{EE} = -5.2 V ±5% (See Note)

SYMBOL	ar lea Tuon a	()°	2	5°	7	5°	
STMBOL	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
tpd	Propagation delay	0.5	1.3	0.5	1.5	0.55	1.55	ns
tr	Rise time (20%-80%)	0.5	1.7	0.5	1.8	0.55	1.9	ns
tf	Fall time(80%-20%)	0.5	1.7	0.5	1.8	0.55	1.9	ns

Note: Each ECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-Ω resistor to -2.0 V.

ECL 10KH High-Speed A DOLMGESM **Emitter-Coupled Logic Family** MC10H104/MC10H107 Quad 2-Input AND Gate/Triple 2-Input **Exclusive OR/NOR Gate**

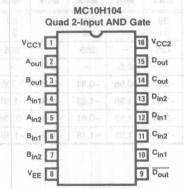
Features/Benefits

- · Propagation delay, 1 ns typical
- · Power dissipation 35 mW/gate typical
- Noise margin 150 mV
- Voltage compensated
- ECL 10K-compatible

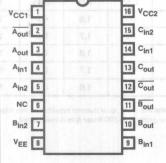
Description

The MC10H104 and MC10H107 are members of Monolithic Memories' new ECL family. These ECL 10KH parts are functional/pinout duplications of the standard ECL 10K family parts with 100% improvement in propagation delay, and no increase in power-supply current.

Pin Configurations



MC10H107 Triple 2-Input **Exclusive OR/NOR Gate**



Ordering Information

1	PART NUMBER	PACKAGE	TEMPERATURE
	MC10H104	LALAU (OO)	3301010
1	MC10H107	J,N,NL(20)	Com Pay

Logic Diagrams MC10H104

Ain1

Ain2

B_{in1}

B_{in2}

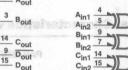
C_{in1}

C_{in2}

D_{in1} 13 Din2

12

4	-	-	-
5	J)	2 A _{out}	
6	-	2	
7		B	

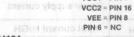


MC10H107

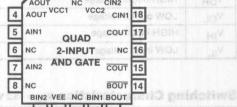
11 Bout

10 12 Cout

VCC1 = PIN	ı	1
VCC2 = PIN	į	16
VFF = PIN	ı	8

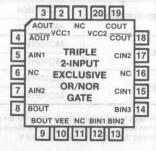


MC10H104 3 2 1 20 19



9 10 11 12 13

MC10H107



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TWX: 910-338-2376

14-17

MC10H104 MC10H107

Absolute Maximum Ratings

Input voltage V _I (V _{CC} = 0)		8.0 V to 0 Vdc
Output current:		
Continuous	 	50 mA
Surge	 Continues and the second of the second	100 mA

Operating Conditions

SYMBOL PARAMET		TED	CC	OMMERCI	AL	UNIT
		IER	MIN	TYP	MAX	UNIT
VEE	Supply Voltage		-5.46	-5.2	-4.94	V
TA	Operating temperature range		0	eldise	75	°C
TSTG Storage temperature range	Storage temperature range	Plastic	-55		150	°C
	Parage temperature range	Ceramic	-55		165	

Electrical Characteristics V_{EE} = -5.2 V ± 5% (See Note)

SYMBOL	PARAMETER		()°	2	5°	7	5°	UNIT
STMBOL			MIN	MAX	MIN	MAX	MIN	MAX	ONT
IE at well	Power supply current	MC10H104 MC10H107	-	39 31	GE SV	35 28	say6	39 31	mA
linH M	Input current HIGH	8100 - 39%	-	425	-	265		265	μΑ
linL	Input current LOW	1771	0.5	-	0.5	-	0.3	-	μΑ
VOH	HIGH output voltage	FOR THE STATE OF T	-1.02	-0.84	-0.98	-0.81	-0.92	0.735	Vdc
VOL	LOW output voltage	1004 9	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
VIH	HIGH input voltage	ENA. 21	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
VIL	LOW input voltage	OIL 0	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

Switching Characteristics $V_{EE} = -5.2 \text{ V}, \pm 5\%$ (See Note)

OVIADOL	PARAMETER		0)°	2	5°	7	5°	
SYMBOL			MIN	MAX	MIN	MAX	MIN	MAX	UNI
	Propagation delay	MC10H104	0.4	1.6	0.45	1.75	0.45	1.9	
^t pd Tropagation delay	1 Topagation dolay	MC10H107	0.4	1.5	0.4	1.6	0.4	1.7	ns
	Disables	MC10H104	0.5	1.6	0.5	1.7	0.5	1.8	
t _r , t+	Rise time	MC10H107	0.5	1.5	0.5	1.6	0.5	1.7	ns
t _f , t- Fall time	MC10H104	0.5	1.6	0.5	1.7	0.5	1.8	-	
	rail time	MC10H107	0.5	1.5	0.5	1.6	0.5	1.7	ns

Note: Each ECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow grater than 500 linear fpm is maintained.

Outputs are terminated through a 50 Ω resistor to -2.0 V.

ECL 10KH High-Speed **Emitter-Coupled Logic Family** MC10H109

Dual 4-5 Input OR/NOR Gate

Features/Benefits

- · Propagation delay, 1 ns typical
- · Power dissipation 35 mW/gate typical
- Noise margin 150 mV
- Voltage compensated
- ECL 10K-compatible

Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
MC10H109	J,N,NL(20)	Com

Electrical Cheractoristics vas -- 32 v - 55 (see h

Description

The MC10H109 is a member of Monolithic Memories' new ECL family. These ECL 10KH parts are functional/pinout duplications of the standard ECL 10K family parts with 100% improvement in propagation delay, and no increase in power-supply current.

Logic Diagram

Pin Configuration MC10H109 MC10H109 Dual 4-5 Input OR/NOR Gate AIN1 4 V_{CC1} 1 3 AOUT AIN2 5 VCC1 = PIN 1 AIN3 6 15 BOUT 2 AOUT AOUT 2 AIN4 7 V_{CC2} = PIN 16 14 BOUT A_{OUT} 3 BIN1 9 B_{IN2} 10 VEE - PIN 8 14 BOUT 13 B_{IN5} AIN1 4 BIN3 11 15 BOUT B_{IN4} 12 AIN2 5 12 B_{IN4} **BIN5 13** 11 B_{IN3} A_{IN3} 6 10 B_{IN2} AIN4 7 Switching Characteristics versus as v. as v. con versus 9 B_{IN1} VEE 8

> MC10H109 3 2 1 20 19 VCC2 BOUT VCC1 AOUT 18 5 DUAL 6 4-5 INPUT NC 16 NC OR/NOR 7 15 **B**4 GATE 8 A3 **B**3 14 A4 VEE NC B1 9 10 11 12 13

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TWX: 910-338-2376 2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2374

Power supply V _{EE} (V _{CC} = 0)	8.0 V to 0 Vdc
Output current:	
Continuous	50 mA
Surge	100 mA

Operating Conditions

OVERDOL		COMMERCIAL				
SYMBOL	PARAMETER		MIN	TYP	MAX	רואט
VEE	Supply Voltage		-5.46	-5.2	-4.94	V
TA	Operating temperature range		0	9860	75	°C
TSTG	Storage temperature range	Plastic	-55		150	°C
	Storage temperature range Ceramic		-55		165	

Electrical Characteristics V_{EE} = -5.2 V ± 5% (See Note)

SYMBOL	PARAMETER		0°		25°		75°		UNIT
SYMBOL			MIN	MAX	MIN	MAX	MIN	MAX	UNIT
I _E	Power supply current	MC10H109	-	15	n and	14	1.34. 6.1	15	mA
linH	Input current HIGH		_	425	germon	265	perior q	265	μΑ
l _{inL}	Input current LOW		0.5	-830	0.5	-	0.3	ao¥=	μΑ
VOH	HIGH output voltage		-1.02	-0.84	-0.98	-0.81	-0.92	0.735	Vdc
VOL	LOW output voltage	0 - 25 d _E	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
VIH	HIGH input voltage		-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
VIL	LOW input voltage		-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

Switching Characteristics V_{EE} = -5.2 V, ±5% (See Note)

SYMBOL	DADAMETER	(0°		25°		75°	
	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
^t pd	Propagation delay	0.4	1.3	0.4	1.3	0.45	1.45	ns
t _r , t+	Rise time	0.5	2.0	0.5	2.1	0.5	2.2	ns
t _f , t-	Fall time	0.5	2.0	0.5	2.1	0.5	2.2	ns

Note: Each ECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50 Ω resistor to -2.0 V.

ECL 10KH High-Speed Emitter-Coupled Logic Family MC10H115 Quad Line Receiver

Features/Benefits

- · Propagation delay 1.0 ns typical
- · Power dissipation, 175 mW typical
- Noise margin 150 mV
- Voltage compensated
- ECL 10K-compatible

Description

The MC10H115 is a Quad Differential Amplifier designed for use in sensing double-ended signals over long lines. This ECL 10KH part is a functional/pinout duplication of the standard ECL 10K family part, with 100% improvement in counting frequency and no increase in power-supply current.

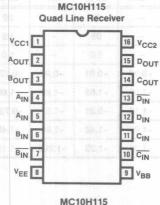
Ordering Information

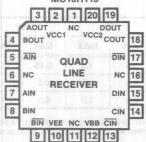
PART NUMBER	PACKAGE	TEMPERATURE
MC10H115	J,N,NL(20)	Com

Application Information

The base bias supply (VBB) is made available at pin 9 to make the device useful as a Schmitt trigger, or in other applications where a stable reference voltage is necesary. Active current sources provide the MC10H115 with excellent common mode rejection. If any amplifier in a package is not used, one input of that amplifier must be connected to VBB (pin 9) to prevent upsetting the current source bias network.

Pin Configuration





Logic Diagram

AIN 4 2 AOU

MC10H115

C_{IN} 10 14 C_{OU}

V_{CC1} = PIN 1 V_{CC2} = PIN 16 V_{EE} = PIN 8

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TWX: 910-338-2376

Monolithic Memories

PMMI

Supply voltage V _E (V _{CC} = 0) Input voltage V _I (V _{CC} = 0)	0 Vdc to VEE
Output Current: Continuous Surge	50 mA

Operating Conditions

SYMBOL	PARAMETER COMMERCI					
VEE	Supply voltage	-5.46 -5.2	-4.94	V		
TA	Operating temperature range	Operating temperature range		75	°C	
T0	A Charles Anna Anna Anna Anna Anna Anna Anna Ann	Plastic	-55	150	°C	
TSTG	Storage temperature range Ceramic Cera		-55 deluca	165	ni es	

Electrical Characteristics V_{EE} = -5.2 V ±5% (See Note)

	ogio Diegram	0°		25°		75°		UNIT
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNI
I _E	Power supply current	-	29	- 3	26	il bad	29	mA
linH	Input current HIGH	-	150		95	-171	95	μΑ
ІСВО	Input leakage current	_	1.5	V 0 Tel.	1.0	- 63	1.0	μΑ
VOH	HIGH output voltage	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
VOL	LOW output voltage	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
VIH	HIGH input voltage	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
VIL	LOW input voltage	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc
V _{BB}	Reference voltage	-1.42	-1.28	-1.35	-1.23	-1.295	1.15	Vdc

Switching Characteristics V_{EE} = -5.2 V, ±5% (See Note)

0.4410.01	DADAMETER	0°		2	25°		75°	
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
tpd	Propagation delay	0.4	1.3	0.4	1.3	0.45	1.45	ns
t _r , t+	Rise time	0.5	1.4	0.5	1.5	0.5	1.6	ns
t _f , t-	Fall time	0.5	1.4	0.5	1.5	0.5	1.6	ns

Note: Each ECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50 fresistor to -2.0 V.

ECL 10KH High-Speed Emitter-Coupled Logic Family MC10H116 Triple Line Receiver

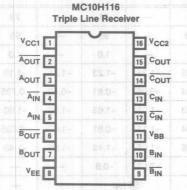
Features/Benefits

- Propagation delay 1 ns typical
- · Power dissipation, 85 mW typ/pkg
- Noise margin 150 mV
- Voltage compensated
- ECL 10K-compatible

Description

The MC10H116 is a Triple Line Receiver. This device is a member of Monolithic Memories' new ECL family. It is a functional/pinout duplication of the standard ECL 10K family part with 100% improvement in propagation delay and no increase in power-supply current.

Pin Configuration



Application Information

Ordering Information

PART NUMBER

MC10H116

The MC10H116 is designed to be used in sensing differential signals over long lines. The bias supply (VBB) is made available to make the device useful as a Schmitt trigger, or in other applications where a stable reference voltage is necessary.

PACKAGE

J,N,NL(20)

TEMPERATURE

Com

Active current sources provide these receivers with excellent common-mode noise rejection. If any amplifier in a package is not used, one input of that amplifier must be connected to VBB to prevent unbalancing the current-source bias network.

The MC10H116 does not have internal-input pull-down resistors. This provides high impedance to the amplifier input and facilitates differential connections.

Typical applications:

- Low level receiver
- Schmitt trigger
- Voltage level interface

Logic Diagram

MC10H116

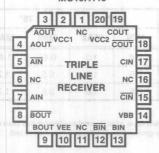
4 2 AOUT 5 3 AOUT

B_{IN} 9 6 B_{OUT} B_{OUT}

C_{IN} 12 14 C_{OUT} 13 15 C_{OUT} V_{BB}

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MC10H116



TWX: 910-338-2376

Monolithic Memories

MM

upply voltage V _{EE} (V _{CC} = 0) -8.0 V to 0 nput voltage V _I (V _{CC} = 0) 0 Vdc to V	VEE
Dutput Current:	
Continuous 50	
Surge	mA

Operating Conditions

SYMBOL) (QL) (e)/(E Brit-	COMMI MIN TY	P MAX	UNIT	
VEE	Supply voltage		-5.46 -5	5.2 -4.94	V
TA	Operating temperature range		0	75	°C
TSTG	Plastic	Plastic	-55	150	00
	Storage temperature range	Ceramic	-55	165	°C

Electrical Characteristics V_{EE} = -5.2 V ±5% (See Note)

OVMO	Lunso, one to out of that are offer must be obened	0	10	2	5°	75°		UNIT
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
ME MONT	Power supply current	0E +	23	- 141	21	elulti"	23	mA
linH	Input current HIGH	961	150	may Inf	95	771	95	μΑ
Ісво	Input leakage current		1.5	mus 0 177	1.0	- 121	1.0	μΑ
V _{BB}	Reference voltage	-1.37	-1.25	-1.35	-1.23	-1.31	-1.19	Vdc
VOH	HIGH output voltage	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
VOL	LOW output voltage	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
VIH	HIGH input voltage (1)	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
VIL	LOW input voltage (1)	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc
VCMR	Common mode range (3)	_	-	-2.85	-0.8	-	10 Yes	Vdc
VPP	Input sensitivity (4)	_	_	150	typ	and a second	_	mVPF

Switching Characteristics V_{EE} = -5.2 V, ±5% (See Note)

CVMDOI	TUD9 - 11 - 12 - 12 - 12 - 12 - 12 - 12 - 1	0°		25°		7	LINUT	
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
^t pd	Propagation delay	0.4	1.3	0.4	1.3	0.45	1.45	ns
t _r , t+	Rise time	0.5	1.5	0.5	1.6	0.5	1.7	ns
t _f , t-	Fall time	0.5	1.5	0.5	1.6	0.5	1.7	ns

Notes: 1. When $V_{\mbox{\footnotesize{BB}}}$ is used as the reference voltage.

- Each ECL 10KH series circuit has been designed to meet the specifications shown in the test table, after thermal equilibrium has been established.
 The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained.
 Outputs are terminated through a 50-Ω resistor to -2.0 V.
- 3. Differential input not to exceed 1.0 Vdc.
- 4. Differential input required to obtain full logic swing on output.

ECL 10KH High-Speed Emitter-Coupled Logic Family MC10H117 Dual 2-Wide 2-3 Input OR-AND/OR-AND-INVERT Gate

Features/Benefits

- · Propagation delay 1 ns typical
- · Power dissipation, 100 mW/gate typical
- Noise margin 150 mV
- Voltage compensated
- ECL 10K-compatible

Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE		
MC10H117	J,N,NL(20)	Com		

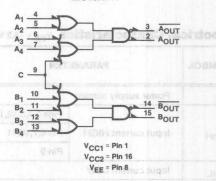
Description

The MC10H117 is a member of Monolithic Memories' ECL 10KH family. This ECL device is a Dual 2 wide 2-3 input OR-AND/OR-AND-INVERT gate designed for use in data distribution and as a data controller for digital multiplexers.

This general purpose logic element is a functional pinout duplication of the standard ECL 10K part, with 100% improvement in propagation delay, and no increase in power-supply current.

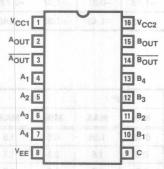
Logic Diagram

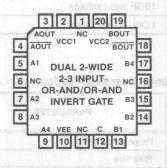
MC10H117



Pin Configurations

MC10H117
Dual 2-Wide 2-3 Input
OR-AND/OR-AND-Invert Gate





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Monolithic Memories

MMI

	, -,	 	 	 	 	 		-0.U V 1	o u vac
Input voltage (VCC = 0)									
Output Current:				10.04			37 人儿		-345
Continuous		 	 	 	 	 			50 mA
Surge		 	 	 	 	 			100 mA

Operating Conditions

SYMBOL	F	PARAMETER	COMMERCIAL MIN TYP MAX	UNIT
VEE	Supply voltage	-5.46 -5.2 -4.94	V	
TA	Operating temperature range		0 75	°C
_	Cttt	Plastic	-55 150	0.0
TSTG	Storage temperature range	Ceramic	-55 165	°C

Electrical Characteristics V_{EE} = -5.2 V ±5% (See Note)

OVMOOL	DADAM		0	0	2	5° // (1/4)	OT JOB 7	5° mate entr	mA μA ν _{dc}
SYMBOL	PARAM	ETER	MIN	MAX	MIN	MAX	MIN	29 275 320 415	UNIT
I _E	Power supply current	- 01 pc	-	29	-	26	_	29	mA
FILE	TUCE # 2	Pins 3,4,5,12,13,14	5 – 1	465	-	275	-	275	
l _{inH}	Input current HIGH	Pin 6,7,10,11	-	545	_	320	-	320	μΑ
	V _{CC} : = Pin 18	Pin 9	_	710	_	415		415	Ci sol
linL	Input current LOW		0.5	-	0.5	_	0.3	-	μΑ
VOH	HIGH output voltage		-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	V _{dc}
VOL	LOW output voltage		-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	V _{dc}
VIH	HIGH input voltage		-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	V _{dc}
VIL	LOW input voltage	liel,	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	V _{dc}

Switching Characteristics V_{EE} = -5.2 V, ±5% (See Note)

SYMBOL	17 As exvent care gara	()°	2	5°	7	5°	UNIT
	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	Propagation delay	0.45	1.35	0.45	1.35	0.5	1.5	ns
t _r , t+	Rise time	0.5	1.50	0.5	1.6	0.5	1.7	ns
t _f , t-	Fall time	0.5	1.50	0.5	1.6	0.5	1.7	ns

Note: Each ECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established.

The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50 Ω resistor to -2.0 V.

ECL 10KH High-Speed Emitter Coupled Logic Family MC10H118 **Dual 2-Wide 3-Input OR-AND Gate**

Features/Benefits

- · Propagation delay 1 ns typical
- · Power dissipation, 100 mW/Gate typical
- Noise margin 150 mV
- Voltage compensated
- ECL 10K-compatible

Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
MC10H118	J,N,NL(20)	Com

Description

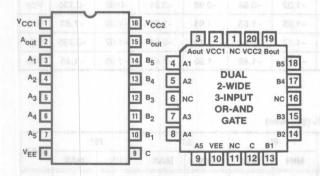
The MC10H118 is a member of Monolithic Memories' ECL 10KH family. This ECL device is a Dual 2-Wide 3-Input OR-AND Gate. It is a functional pinout duplication of the standard ECL 10K part with 100% improvement in propagation delay and no increase in power supply current.

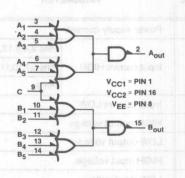
Logic Diagram

MC10H118 **Dual 2-Wide** 3-Input OR-AND Gate

Pin Configurations

MC10H118 **Dual 2-Wide 3-Input OR-AND Gate**





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14-27

Input voltage V _I (V _C C = 0)	- 0)8.0 V to 0 Vd
Continuous	

Operating Conditions

SYMBOL	F	COMMERCIAL MIN TYP MAX	UNIT	
VEE	Supply voltage	-5.46 -5.2 -4.94	V	
TA	Operating temperature range		0 75	°C
_	2	Plastic	-55 150	
TSTG	Storage temperature range	Ceramic	-55 165	°C

Electrical Characteristics V_{EE} = -5.2 V ±5% (See Note)

			-	0° 25°			7	5°	
SYMBOL	PARAM	ETER	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
I _E	Power supply current	A A A	- 29 - 26 - 465 - 275 - 545 - 320 - 710 - 415	Inother	29	mA			
	100 A A C T	Pins 3,4,5,12,13,14	_	465	-	275	_	275	
The second of th	Input current HIGH	Pins 6,7,10,11	_	545	_	320	- 180	320	μΑ
	: Ma - 100A	Pin 9	-	710	RED CHA	415	E ODIVE-S	415	
linL	Input current LOW	Ta Di ja	0.5	-	0.5	_	0.3	—	μΑ
VOH	HIGH output voltage	74-1-10	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
VOL	LOW output voltage	81 19	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
VIH	HIGH input voltage	70	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
VIL	LOW input voltage		-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc
			43554	JAI	103	Benedy	0.00	-	prof .

Switching Characteristics V_{EE} = -5.2 V, ±5% (See Note)

SYMBOL	PARAMETER	(o an	2	5°	7	5°	unit
	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNII
tpd	Propagation delay	0.5	1.6	0.5	1.7	0.55	1.85	ns
t _r , t+	Rise time	0.5	1.5	0.5	1.6	0.5	1.7	ns
t _f , t-	Fall time	0.5	1.5	0.5	1.6	0.5	1.7	ns

Note: Each ECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-Ω resistor to -2.0 V.

ECL 10KH High-Speed Emitter Coupled Logic Family MC10H119 4-Wide 4-3-3-3 Input OR-AND Gate

Features/Benefits

- · Propagation delay 1 ns typical
- Power dissipation, 100 mW/Gate typical
- Noise margin 150 mV
- Voltage compensated
- ECL 10K-compatible

Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
MC10H119	J,N,NL(20)	Com

Description

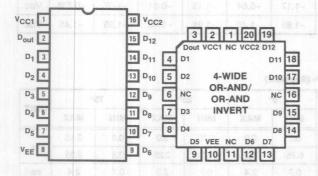
The MC10H119 is a member of Monolithic Memories' ECL 10KH family. This ECL device is a 4-Wide 4-3-3-3 Input OR-AND Gate. It is a functional pinout duplication of the standard ECL 10K part with 100% improvement in propagation delay and no increase in power supply current.

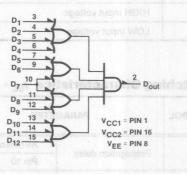
Pin Configurations

MC10H119 4-Wide 4-3-3-3 Input OR-AND Gate

Logic Diagram

MC10H119 4-Wide 4-3-3-3 Input OR-AND Gate





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TWX: 910-338-2376
TWX: 910-338-2374
Memories

MM

14-29

Supply voltage VEE (VCC = 0) -8.0 V to 0 Vd Input voltage V _I (V _{CC} = 0) 0 Vdc to V _E	
Output Current:	
Continuous	4
Surge	4

Operating Conditions

SYMBOL	D (DS)JIAMS 681	COMMERCIAL MIN TYP MA	LIMIT	
VEE	Supply voltage		-5.46 -5.2 -4.9	4 V
TA	Operating temperature range		0 7	5 °C
	2	Plastic	-55 15	
	Storage temperature range	Ceramic	-55 16	°C

Electrical Characteristics V_{EE} = -5.2 V ±5% (See Note)

			0°		25°		75°		DOT YOU
SYMBOL.	PARAM	ETER	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
I _E	Power supply current			29		26	1-1	29	mA
linH		Pins 3,4,5,6,7,9,11, 12,13,14,15	<i>3</i> _	500	-	295	no <u>ll</u> are	295	μΑ
		Pin 10		610	-	360	_	360	
linL	Input current LOW		0.5		0.5	- 411 <u>22</u> 401:	0.3	-	μΑ
VOH	HIGH output voltage	te pri	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
VOL	LOW output voltage		-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
VIH	HIGH input voltage		-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
VIL	LOW input voltage	Au - A	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

Switching Characteristics V_{EE} = -5.2 V, ±5% (See Note)

SYMBOL			(0°		25°		75°	
	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	TINU	
^t pd	Propagation delay	All others	0.7	2.0	0.75	2.0	0.8	2.15	ns
		Pin 10	0.75	2.2	0.75	2.25	0.8	2.35	
t _r , t+	Rise time		0.7	2.4	0.7	2.3	0.7	2.4	ns
t _f , t-	Fall time		0.7	2.4	0.7	2.3	0.7	2.4	ns

Note: Each ECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50 Ω resistor to -2.0 V.

ECL 10KH High-Speed Emitter-Coupled Logic Family MC10H121 4-Wide OR-AND/OR-AND-INVERT Gate

Features/Benefits

- Propagation delay 1 ns typical
- · Power dissipation, 145 mW typical
- Noise margin 150 mV
- Voltage compensated
- ECL 10K-compatible

Pin Configuration

D₄ 7

VEE 8

Ordering Information

Logic Diagram

13

14

15

D₁₀

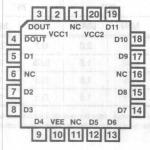
PART NUMBER	PACKAGE	TEMPERATURE
MC10H121	J, N, NL	Com

Description

The MC10H121 is a 4-Wide OR-AND/OR-AND-INVERT Gate.
This device is a member of Monolithic Memories' new ECL family. This ECL 10KH part is a functional/pinout duplication of the standard ECL 10K family part with 100% improvement in propagation delay, and no increase in power-supply current.

MC10H121 MC10H121 4-Wide OR-AND/OR-AND-INVERT Gate VCC1 1 16 V_{CC2} 15 D₁₁ POUT 2 POUT 3 14 D₁₀ D₁ 4 13 D₉ DOUT D₂ 5 12 D₈ 10 3 DOUT D6 -D₃ 6 11 D₇ 12

MC10H121



to Provingation delay All others

(a the Rich time to Fall time)

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TWX: 910-338-2376

Monolithic Memories

VCC1 = PIN 1

V_{CC2} = PIN 16

VEE - PIN 8



14.31

14

10 D₆

9 D₅

Supply voltage VEE (VCC = 0)	Input v
Continuous	Cor
Surge	Sur

Operating Conditions

SYMBOL	S GH.M.C PSTS	22111	MERCIAL TYP MAX	UNIT	
VEE	Supply voltage	-5.46	-5.2 -4.94	V	
TA	Operating temperature range	0	75	°C	
TSTG		Plastic	-55	+150	00
	Storage temperature range	Ceramic See TREVALCHA-RONG AA-RO	-55	+165	°C

Electrical Characteristics V_{EE} = -5.2 V ±5% (See Note)

	PARAMETER		0°		25°		75°		LIMIT
SYMBOL	PARAI	WEIER TENED	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
I _E	Power supply curren	nt	-	29	_	26	DAVI —	29	mA
linH	1	Pins 4 - 7, 9, 11 - 15	-	500	A FEBRUAR	295	NEUSALA-Y-II	295	
	Input current HIGH Pin 10	<u> </u>	610	151 <u>4</u> (8)	360	-0	360	μΑ	
linL	Input current LOW	- 1 - 1 - 1 - 1 - 1 - 1 - 1 - 1 - 1 - 1	0.5	-	0.5	_	0.3	rue <u>G</u>	μΑ
Vон	HIGH output voltage	Carrier of	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
VOL	LOW output voltage	Carley o	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
VIH	HIGH input voltage	Da-a	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
VIL	LOW input voltage	11 10	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

Switching Characteristics V_{EE} = -5.2 V, ±5% (See Note)

SYMBOL			(0°		25°		75°	
	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNIT	
^t pd	Propagation delay	All others	0.55	1.95	0.6	2.0	0.7	2.40	
		Pin 10	0.45	1.8	0.45	1.8	0.55	2.2	ns
t _r , t+	Rise time		0.5	1.7	0.5	1.8	0.5	1.9	ns
t _f , t-	Fall time		0.5	1.7	0.5	1.8	0.5	1.9	ns

Note: Each ECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50 Ω resistor to -2.0 V.

ECL 10KH High-Speed Emitter-Coupled Logic Family MC10H124 Quad TTL-to-ECL Translator

Features/Benefits

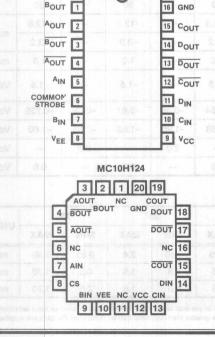
- Propagation delay 1.5 ns typical
- Power dissipation 520 mW typical
- Noise margin 150 mV
- Voltage compensated
- ECL 10K-compatible

Description

The MC10H124 is a Quad TTL-to-ECL translator. This device is a member of Monolithic Memories' new ECL family. This quad translator is used for interfacing data and control signals between a saturated logic section and the ECL section of digital systems. The 10KH part is a functional/pinout duplication of the standard ECL 10K family part, with 100% improvement in propagation delay, and no increase in power-supply current.

MC10H124
Quad TTL-to-ECL Translator

Pin Configuration



Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
MC10H124	J, N, NL	Com

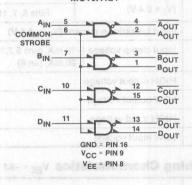
Application Information

The MC10H124 has TTL-compatible inputs and ECL complementary open-emitter outputs that allow use as an inverting/non-inverting translator or as a differential line driver. When the common strobe input is at the low logic level, it forces all true outputs to an ECL low logic state and all inverting outputs to an ECL high logic state.

An advantage of this device is that TTL-level information can be transmitted differentially, via balanced twisted-pair lines, to ECL equipment, where the signal can be received by the MC10H115 or MC10H116 differential line receivers. The power supply requirements are ground, +5.0 volts, and -5.2 volts.

Logic Diagram

MC10H124



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TWX: 910-338-2376 **Monolithic**

MMI

Supply voltage VEE (VCC = 5.0 V) Supply voltage, VCC (VEE = -5.2 V) Input Voltage, V _I (VCC = 5.0 V)	 	. 0 to +7.0 Vdc
Output Current: Continuous Surge		50 mA

Operating Conditions

SYMBOL	PAR.	COMMERCIAL MIN TYP MAX	UNIT	
VEE	Supply voltage		-5.46 -5.2 -4.94	V
TA	Operating temperature range		0 75	°C
ekumaa JO	Storage temperature range	Plastic	-55 +150	100
STG		Ceramic	-55 +165	°C

Electrical Characteristics V_{EE} = -5.2 V ±5% V_{CC} = 5.0 V ±5% (See Note)

SYMBOL	n sovenisge of th PARAMETER linform		0	0 10 10 10	2	5°	75°		UNIT
STIVIBUL			MIN	MAX	MIN	MAX	MIN	MAX	UNII
Ens rewi	Negative power supply d	Negative power supply drain current		72	-	66	_	72	mA
ICCH	Positive power supply dr		-	16	-	16	nottan	18	mA
ICCL	Positive power supply dr	Positive power supply drain current*		25	-	25	и —	25	mA
L	Input current HIGH	Pin 6	-	200	ro <u>ht</u> lans	200	LITT bsut	200	_
IH.	(V _I = 2.4 V)	Pins 5, 7, 10, 11	_	50	COME THE	50	1	50	μΑ
1	Input current LOW	Pin 6	1	-12.8	1300 100	-12.8	10	-12.8	A
IIL	(V ₁ = 0.4 V)	Pins 5, 7, 10, 11	-	-3.2	ugo mil	-3.2	41	-3.2	mA
ال	Input breakdown current	(V _{in} = 5.5 V)		1.0	uoo (1.0	+	1.0	mA
VIC	Input clamp voltage (-10	mA, pins 5,7,10,11) mA, pin 6)		-1.5	1005 <u>Fii</u>	-1.5	1	-1.5	Vdd
VOH	HIGH output voltage		-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdd
VOL	LOW output voltage		-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdd
V _{IH}	HIGH input voltage	EB0	2.0	_	2.0	deleter - Appendix	2.0		Vdd
VIL	LOW input voltage		_	0.8	_	0.8	Na -	0.8	Vdc

Switching Characteristics V_{EE} = -5.2 V, $\pm 5\%$ (See Note)

SYMBOL	DADAMETER	0°		25°		75°		LINUT
	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
^t pd	Propagation delay	0.55	2.25	0.55	2.4	0.85	2.95	ns
t _r , t+	Rise time	0.5	1.5	0.5	1.6	0.5	1.70	ns
t _f , t-	Fall time	0.5	1.5	0.5	1.6	0.5	1.70	ns

Note: Each ECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50 Ω resistor to -2.0 V.

^{*} ICCH — Current drain from V_{CC} power supply with all inputs at Logic HIGH level ICCL — Current drain from V_{CC} power supply with all inputs at Logic LOW level.

ECL 10KH High-Speed Emitter-Coupled Logic Family MC10H125 Quad ECL-to-TTL Translator

PRELIMINARY INFORMATION

This document contains specifications and information which are subject to change.

Features/Benefits

- Propagation delay, 2.5 ns typical
- Power Dissipation 520 mW typical
- Noise margin 150 mV
- Voltage compensated
- ECL 10K-compatible

Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
MC10H125	J,N,NL(20)	Com AT

Application Information

The MC10H125 incorporates differential inputs and Schottky TTL "totem pole" outputs. The differential inputs don't have input pull-down and allow for use as an inverting/non-inverting translator or as a differential line receiver. The V_{BB} reference voltage is available from Pin 1 for use in single-ended input biasing. The outputs of the MC10H125 go to a low logic level whenever the inputs are left floating.

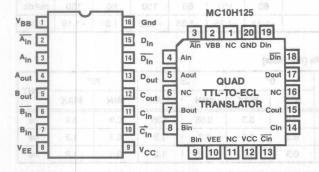
An advantage of this device is that ECL-level information can be received via balanced twisted pair lines in the TTL equipment. This isolates the ECL-logic from the noisy TTL environment. Power supply requirements are ground, +5.0 volts and -5.2 volts.

Description

The MC10H125 is a member of Monolithic Memories' ECL family. The MC10H125 is a quad translator for interfacing data and control signals between the ECL section and TTL compatible section of digital systems. The 10KH part is a functional/ pinout duplication of the standard ECL 10K family part, with 100% improvement in propagation delay, and no increase in power-supply current.

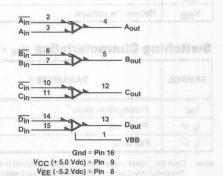
Pin Configuration

MC10H125
Quad ECL-to-TTL Translator



Logic Diagram

MC10H125 Quad ECL-to-TTL Translator



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Monolithic Memories

14-35

Power supply V _{FF} (V _{CC} ± 5.0 V)	8.0 V to 0 Vdc
Power Supply V _{CC} (V _{EE} = -5.2 V)	0 V to +7.0 Vdc
Input voltage V _I (V _{CC} = 5.0 V)	0 Vdc to V _{EE}

Operating Conditions

SYMBOL	not be par		MERCIAL TYP MAX	UNIT	
VEE	Supply Voltage	MITGAN	-5.46	-5.2 -4.94	V
TA	Operating temperature range	MC10	0	75	°C
TSTG	TSTG Storage temperature range	Plastic	-55	150	°C
1516 010	Storage temperature range	Ceramic		165	

Electrical Characteristics V_{EE} = -5.2 V ± 5%, V_{CC} = 5.0 V ± 5% (See Note)

OVMDOL	o patinger in a sea an indiger		0)°	2	5°	7	5°	UNIT
SYMBOL	PARAMETER		MIN	MAX	MIN	MAX	MIN	MAX	UNIT
IE SEST	Negative power supply drain current		Buprio V	44	s at her	40	Latter	44	mAdc
Іссн	THOUGHT SECURE OF THE SECURE O	Outputs = H	Whot is	63	ilm <u>ai</u> M	63	stander	63	usoilqu
ICCL	Positive power supply drain current	Outputs = L	-	40	-	40	-	40	mAdc
linH	Input current		-	225	-	145	-	145	μAdc
Ісво	Input leakage current		_	1.5	-	1.0	-	1.0	μAdc
VOH	HIGH output voltage	OH = -1 mA	2.5	-	2.5	_	2.5	_	Vdc
VOL	LOW output voltage	OL = +20 mA	_	0.5	_	0.5	(CEEBY	0.5	Vdc
VIH	HIGH input voltage		-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
VIL	LOW input voltage		-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc
los	Short circuit current			150	60	150	60	150	mAdc
V _{BB}	Reference voltage		-1.37	-1.25	-1.35	-1.23	-1.31	-1.19	Vdc

Switching Characteristics V_{EE} = -5.2 V, $\pm 5\%$ (See Note)

SYMBOL	PARAMETER	0°		25°		75°		LINUT
	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
tpd	Propagation delay*	0.8	3.3	0.85	3.35	0.9	3.4	ns
t _r , t+	Rise time	0.3	1.2	0.3	1.2	0.3	1.2	ns
t _f , t-	Fall time	0.3	1.2	0.3	1.2	0.3	1.2	ns

Note: Each ECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50 Ω resistor to -2.0 V.

^{*} Drives a 25-pF load.

ECL 10KH High-Speed Emitter-Coupled Logic Family Dual Latch MC10H130

Features/Benefits

- · Propagation delay, 1 ns typical
- Power dissipation, 155 mW typical
- Noise margin 150 mV
- · Voltage compensated
- ECL 10K-compatible

Description

The MC10H130 is a dual latch which has two different mechanisms to retain data through latch control signals. Each latch can be operated separately by holding the common latch control signal (C) LOW, then switching an individual latch control signal (CE1/CE2) from LOW to HIGH to cause retention of data in the relevant latch. If simultaneous operation of both latches is required, CE1 and CE2 are held LOW and the common latch control C is switched from LOW to HIGH.

For either latch, data present at the inputs (D1/D2) will be seen at the outputs (Q1/Q1 and Q2/Q2) when both latch control signals are LOW. This condition allows data to be setup within the latch, after which time causing a positive transition to the HIGH state on either or both latch control signals causes data retention. After either or both of these signals are HIGH, subsequent changes in data at an input are ignored by the latch, provided the hold time requirement is met.

An alternative means to load data in the latches is to use the direct set and reset (S1/S2 and R1/R2, respectively) lines. These inputs do not override the latch controls, or the D inputs. Instead, set or reset are only effective when either C. CE1/CE2 or both. are HIGH. Note that this relationship is different than the case for a similar part, the MC10H131, which is a Dual Master-Slave D-type Flip-Flop.

Function Table

D	C	CE1/CE2	R	S	Q _{n=1}
L	L	Commence of the state of the spirit	X	X	L
Н	L.	Will N	X	X	- Н
X	Н	X	L	L	Qn
X	Н	×	L	Н	Н
X	Н	X	Н	L	L
X	Н	×	Н	ОСН	N.D.
X	X	Н	DL	2 L	Qn
X	X	€ (H	L	аН	8.H
X	X	Н	Н	e.L	9 L
X	X	Н	Н	Н	N.D.

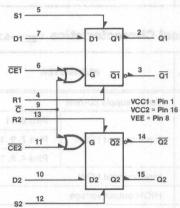
X = Don't Care N.D. = Not Defined

Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
MC10H130	J,N,NL(20)	Com

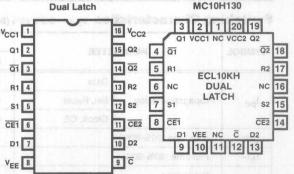
Logic Diagram

MC10H130 **Dual Latch**



Pin Configurations

MC10H130



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TWX: 910-338-2376



MC10H130

Absolute Maximum Ratings

Supply voltage V _{EE} (V _{CC} = 0) Input voltage V _I (V _{CC} = 0)	0V _{dc} to V _{EE}
Output Current: Continuous Surge	

Operating Conditions

SYMBOL	PARAMETER COMMERCIA MIN TYP M.					
VEE	Supply voltage		-5.46 -5.2 -4.94	V		
TA	Operating temperature range	bigod	0 75	°C		
_	MC10H13R	Plastic Material maneful own ser dear	-55 0 8 8 0 150	ine MC		
T _{stg}	Storage temperature range	-55 165	°C			

Electrical Characteristics V_{EE} = -5.2 V ±5% (See Note)

	PARAMETER		0	0	2	5° 01 W	I mont ty	5°	toutoc
SYMBOL			MIN	MAX	MIN	MAX	MIN	MAX	UNIT
I _E Power supply curre		0 18	- /6	38	id W o <u>w</u> es s	35	olla <u>n</u> onit	38	mA
	2 m ² = 33 V	Pins 6, 11	- 10	468	ti er al ino	275	moc -d oral	275	entis n
linH	Input current HIGH	Pins 7, 9, 10	- 100	545	richel and	320	Barta TO CO	320	μΑ
		Pins 4, 5, 12, 13	_	434	_	255	iem <u>ai</u> tre	255	anii bic
linL	Input current LOW	92	0.5	is to use the	0.5	Finistate (0.3	iam évilen Inserbust	μΑ
V _{OH}	HIGH output voltage	11	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
VOL	LOW output voltage		-1.95	-1.63	-1,95	-1.63	-1.95	-1.60	Vdc
VIH	HIGH input voltage	tin Configurat	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
VIL	LOW input voltage	MC10H130	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

Switching Characteristics VEE = -5.2 V ±5% (See Note)

SVMP OI	PARAMETER		177	0°		25°		75°		UNIT
SYMBOL			77.85	MIN	MAX	MIN	MAX	MIN	MAX	UNII
DIKH NG	The Later DU	Data	Fig.	0.40	1.60	0.40	1.70	0.40	1.80	Y
t _{pd}	Propagation delay	Set, Reset	12111	0.60	1.70	0.70	1.80	1.80	1.90	ns
	PEO 8 335 7	Clock, CE	1000	0.50	1.60	0.50	1.70	1.70	1.80	×
t _r ,t+	Rise time (20%-80%)		File	0.5	1.6	0.5	_ 1.7	0.5	1.8	ns
t _f ,t-	Fall time (80%-20%)		No.	0.5	1.6	0.5	1.7	0.5	1.8	ns
t _{set}	Setup time	Tours of the second	-	0.5	1.6	0.5	1.7	0.5	1.8	ns
thold	Hold time			0.5	1.6	0.7	H _	0.7	X	ns

Note: Each ECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50 Ω resistor to -2.0 V.

ECL 10KH High-Speed **Emitter-Coupled Logic Family** MC10H131 **Dual Master-Slave Type D Flip-Flop**

Features/Benefits

- · Propagation delay, 1 ns typical
- · Power dissipation, 235 mW typical
- Noise margin of 150 mV
- Voltage compensated
- ECL 10K-compatible

Description

The MC10H131 is a member of Monolithic Memories' ECL family. The MC10H131 is a dual master-slave D-type flip-flop. Asynchronous Set (S) and Reset (R) override Clock (CC) and Clock Enable (CE) inputs. Each flip-flop may be clocked separately by holding the common clock in the low state and using the enable inputs for the clocking fuction. If the common clock is to be used to clock the flip-flop, the Clock Enable inputs must be in the low state. In this case, the enable inputs perform the function of controlling the common clock.

The output states of the flip-flop change on the positive transition of the controlling input(s). A change in the information present at the data (D) input will not affect the data output at any other time due to master slave construction.

This ECL 10KH part is a functional/pinout duplication of the standard ECL 10K family part, with 100% improvement in clock speed and propagation delay and no increase in power supply

Function Tables

R-S TRUTH TABLE

R	S	Q _{n + 1}
L	L	Qn
L	Н	Н
Н	L	L
Н	Н	N.D.

N.D. = Not Defined.

CLOCKED TRUTH TABLE

A Property of the second		
С	D	Q _{n + 1}
L	X	Qn
н	L	L
н	Н	Н

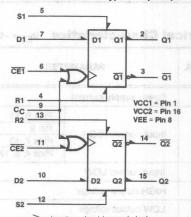
X = Don't Care. C = CE + CC

Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
MC10H131	J,N,NL(20)	Com

Logic Diagram

MC10H131 **Dual Master-Slave Type D Flip-Flop**

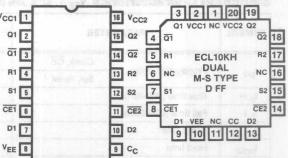


> : denotes edge triggered clock

Pin Configurations

MC10H131

Du	ual Master-	Slave Typ	e D Flip-Flop		MC1	ЮН	131
V	CC1 1	-	16 V _{CC2}	3	2	1	20
	01 2		15 00 1		VCC1	NC	vcc



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TWX: 910-338-2376

Supply voltage V _{EE} (V _{CC} = 0)	8.0 to 0 V _{dc}
Input voltage V _I (V _{CC} = 0)	0 V _{dc} to V _{EE}
Output Current:	
Continuous	50 mA
Surge	

Operating Conditions

SYMBOL	O [[(88), 194, 14, 1	PARAMETER	COMMERCIAL MIN TYP MAX	UNIT
VEE	Supply voltage		-5.46 -5.2 -4.94	V
TA	Operating temperature range		0 75	°C
_	Characa tamparatura ranga	Plastic	-55 150	°C
TSTG	Storage temperature range	Ceramic	-55 165	DIM en

Electrical Characteristics V_{EE} = -5.2 V ±5% (See Note)

	PARAMETER		- 0	0° ministra		5°qqll-qill e	ritologia 7	5° oau ed o	UNIT
SYMBOL	PARAMI	ETER® 155	MIN	MAX	MIN	MAX	MIN	MAX	UNI
I _E	Power supply current	- 18	(9)	62	tioon <u>e</u> ti n	56	ell-q ill arili	62	mA
	Y2CZ - Ph 16	Pins 6, 11	- 4	530	moloo ata	310	Too Tow to	310	the dr
	Input current HIGH	Pin 9	_	660	_	390	aga s vste	390	and the state of
linH		Pins 7, 10	_	485		285	_	285	μΑ
		Pins 4, 5, 12, 13	- 1	790	HENDERSONES	465	nat wer his tine villres	465	Maria Sur
linL	Input current LOW	Dr	0.5	(GLR <u>-1</u> 9)90	0.5	ni d <u>a J</u> oria	0.3	geq e. q bi	μΑ
VOH	HIGH output voltage		-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdd
VOL	LOW output voltage	52	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdd
VIH	HIGH input voltage		-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdd
VIL	LOW input voltage	in Configuration	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdd

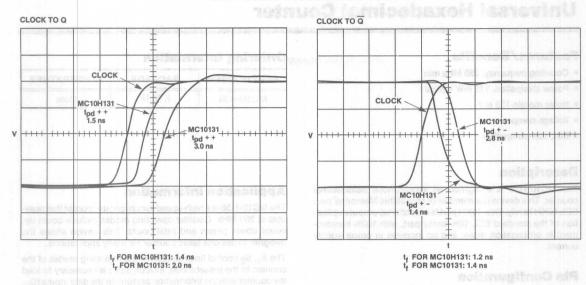
Switching Characteristics V_{EE} = -5.2 V, ±5% (See Note)

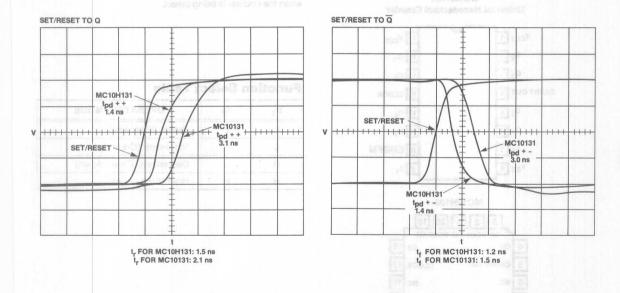
VCC L 02	PARAMETER			0°		25°		75°		LINUT
SYMBOL				MIN	MAX	MIN	MAX	MIN	MAX	UNIT
HXI	EQL IN EQL	Clock, CE	line.	0.80	1.6	0.8	1.7	0.8	1.8	
tpd	Propagation delay S	Set, Reset	Land.	0.6	1.6	0.7	1.7	0.7	1.8	ns
t _r , t+	Rise time (20%-80%)		1000	0.6	2.0	0.6	2.0	0.6	2.2	ns
t _f , t-	Fall time (80%-20%)			0.6	2.0	0.6	2.0	0.6	2.2	ns
t _{set}	Setup time			0.7		0.7		0.7		ns
thold	Hold time		[3]	0.8		0.8		0.8		ns
ttog	Toggle frequency	Parameter Control		250	-	250		250		MHz

Note: Each ECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established.

The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50 Ω resistor to -2.0 V.

Switching Time Comparison ECL 10KH versus ECL 10K





NOTE: $t_{\rm p}$ and $t_{\rm f}$ measured from the 20% to the 80% level of the output signal swing. $t_{\rm pd}$ is measured from the 50% level of the input to the 50% level of the output.

ECL 10KH High-Speed Emitter-Coupled Logic Family MC10H136 Universal Hexadecimal Counter

Features/Benefits

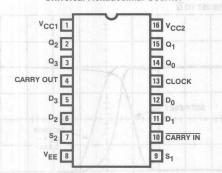
- · Counting frequency, 250 MHz min.
- Power dissipation, 715 mW typical
- Noise margin 150 mV
- Voltage compensated
- ECL 10K-compatible

Description

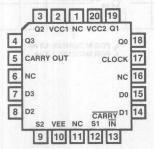
The MC10H136 is a high-speed synchronous hexadecimal counter. This device is a member of Monolithic Memories' new ECL 10KH family. This 10KH part is a functional/pinout duplication of the standard ECL 10K family part, with 100% improvement in propagation delay, and no increase in power-supply current.

Pin Configuration

MC10H136 Universal Hexadecimal Counter



MC10H136



Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
MC10H136	J, N, NL	Com

Application Information

The MC10H136 is a high-speed synchronous counter that operates at 250 MHz. Counter operating modes include count up, count down, preset and hold count. This device allows the designer to use one basic counter for many applications.

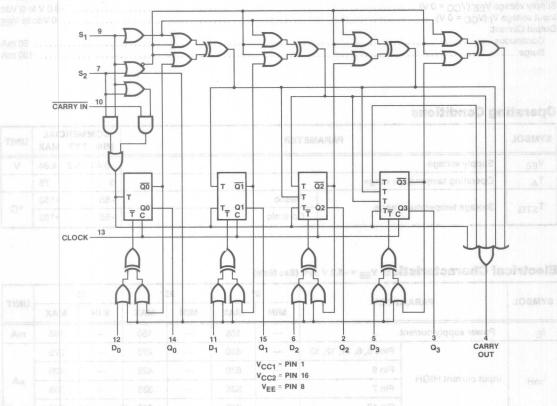
The S_1 , S_2 control lines determine the operating modes of the counter. In the preset mode, a clock pulse is necessary to load the counter with the information present on the data inputs (D_0 , D_1 , D_2 and D_3). Carry out goes low on the terminal counter or when the counter is being preset.

Function Select Table

S ₁	S ₂	OPERATING MODE
L	1819 Clar	Preset (Program)
L	H	Increment (Count up)
Н	L	Decrement (Count down)
Н	Н	Hold (Stop count)

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Logic Diagram



Sequential Truth Table*

INPUTS					C.U		OUTPUTS					UTS		
S ₁	S ₂	D ₀	D ₁	D ₂	D ₃	CARRY	CLOCK	Q ₀	Q ₁	Q ₂	Q ₃	CARRY	SELECT	
o.b.	88 4 0-	Liui	L	н.	e H	X	5	L	L	Н	eHalle	ov roda HE	Preset	
L	Н	X	X	X	X	BaLt -	5	Н	L	Н	Hai	ov n.Hmi vy	Increment	
L	Н	X	X	X	X	L	5	L	Н	Н	Н	Н	Increment	
L	de Hose	X	X	X	X	design i cht de	5	en Hudu	on Hone	a s (H bet	mo/Hot	eloes i <u>t</u> uf e ni	Increment	
L	Н	X	X	Х	X	Н		Н	Н	Н	Н	Н	Increment	
L	Н	Х	Х	Х	Х	Н	5	Н	Н	Н	Н	Н	Increment	
Н	Н	Х	Х	Х	X	X	5	Н	Н	Н	Н	Н	Hold	
L	L	Н	Н	L	L	X	5	Н	Н	L	L	L	Preset	
Н	L	Х	Х	X	Х	L	5	L	Н	L	L	Н	Decrement	
Н	L	X	X	X	X	L	5	Н	L	L	L	Н	Decrement	
Н	L	X	X	X	X	L	5	L	L	L	L	L	Decrement	
Н	L	X	Х	X	X	L	5	Н	Н	Н	Н	Н	Decremen	

x = Don't care

Truth table shows logic states assuming that the inputs vary in sequence from top to bottom, as shown.

The states of the Q0-Q3 outputs are shown assuming the occurance of a L-to-H edge transition (e.g. after clocking).

Input voltage V _I (V _{CC} = 0 V) -0.0 V to	
Output Current:	
Continuous	50 mA
Surge	00 mA

Operating Conditions

SYMBOL	PA	RAMETER		COMMI MIN TY		UNIT
VEE	Supply voltage			-5.46 -5	.2 -4.94	V
TA	Operating temperature range		- 50	0	75	
_	State to the state of the state	Plastic		-55	+150	00
TSTG	Storage temperature range	Ceramic		-55	+165	°C

Electrical Characteristics V_{EE} = -5.2 V ±5% (See Note)

CVMDOI	2424	PARAMETER		0	2	5°	7	5°	
SYMBOL	PARAI	WEIER	MIN	MAX	MIN	MAX	MIN	MAX	UNI
I _E	Power supply currer	nt	1 - 1	165		150	SF -	165	mA
	YNRAD 10	Pins 5, 6, 11, 12, 13	60 - 10	430	_ 00	275	961	275	
	lanut surrent IIICI	Pin 9	Ing Length	670	_	420	_	420	
linH	Input current HIGH	Pin 7	V _{ES} _ PUN	535	_	335	-	335	μΑ
		Pin 10	_	380	-	240	riturii	240	upa
linL	Input current LOW		0.5	-	0.5	nuc ul e	0.3	<u> </u>	μΑ
VOH	HIGH output voltage		-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdd
VOL	LOW output voltage	En In En	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdd
VIH	HIGH input voltage	H 3 3	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdd
VIL	LOW input voltage		-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

Note: Each ECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The Circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50 Ω resistor to -2.0 V.

Switching Characteristics V_{EE} = -5.2 V, ±5% (See Note)

nonmudes to change.	Tinc anomento		0	0	2	5°	7	5°	1218
SYMBOL	PARAI	METER	MIN	MAX	MIN	MAX	MIN	MAX	UNI
		Clock to Q	0.7	2.3	0.7	2.4	0.7	2.5	
^t pd	Propagation delay	Clock to carry out	1.0	4.8	1.0	4.9	1.0	5.0	ns
MODEL TAX	Heart anama	Carry in to carry out	0.7	2.5	0.7	2.6	0.7	2.7	A HINE
2.015.00		Data (D0 to C)	2.0	_	2.0	-tso <u>lu</u> yf V	2.0	hea <u>m</u> ea	12.09
(1)	et Setup time	Select (S to C)	3.5	_	3.5	_	3.5	r or State	ns
^t set		Carry in (Cin to C)	2.0	_	2.0	_	2.0		
		Carry in (C to Cin)	0	_	0	_	0	-	
		Data (C to D0)	0	_	0		0	12 12 13 13 A	0000
	Hold time	Select (C to S)	-0.5	ins a Tanta	-0.5	ating Walks	-0.5	10 704-11	inta argo
thold	Hold time	Carry in (C to Cin)	0	nd <u>92 c</u> ont	0 0	i gr <u>un</u> opte	0	the anoth	ns
	Voca , see [Carry in (Cin to C)	2.2	geo <u>Li</u> nivo	2.2	_	2.2	of and	S. Avenue
fcount	Counting frequency		250		250	- Constanting to the second	250	-	MHz
t _r ,t+	Rise time	ri - 181	0.5	2.3	0.5	2.4	0.5	2.5	ns
t _f ,t-	Fall time		0.5	2.3	0.5	2.4	0.5	2.5	ns

Note: Each ECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50 Ω resistor to -2.0 V.

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ECL 10KH High-Speed Emitter-Coupled Logic Family MC10H141 **Four-Bit Universal Shift Register**

PRELIMINARY INFORMATION

This document contains specifications and information which are subject to change.

Features/Benefits

- Shift frequency, 250 MHz min
- Power dissipation, 425 mW typical
- Noise margin 150 mV
- Voltage compensated
- **ECL 10K-compatible**

Description

The MC10H141 is a four-bit universal shift register which performs shift-left, or shift-right, serial/parallel in, and serial/parallel out operations with no external gating. Inputs S1 and S2 control

(See following page)

Function Table

SELECT		3.5	OUT	OPERATING			
S1	S2	Q0 _{n-1}	Q1 _{n-1}	Q2 _{n-1}	Q3 _{n-1}	MODE	
L	L	D0	D1	D2	D3	Parallel entry	
L	Н	Q1 _n	Q2 _n	Q3 _n	DR	Shift right*	
Н	L	DL	Q0 _n	Q1 _n	Q2 _n	Shift left*	
Н	L	Q0 _n	Q1 _n	Q2 _n	Q3 _n	Stop shift	

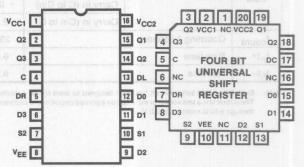
Outputs as exist after pulse appears at "C" input with input conditions as shown (Pulse Positive transition of clock input).

Ordering Information

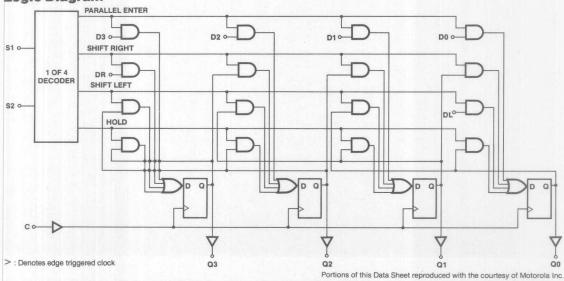
PART NUMBER	PACKAGE	TEMPERATURE
MC10H141	J,N,NL(20)	Com

MC10H141 Four-Bit Universal Shift Register





Logic Diagram



TWX: 910-338-2376

2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2374

Supply voltage, V _{FF} (V _{CC} = 0)		8.0 V to 0 V _{dc}
Input voltage, V ₁ (V _{CC} = 0)		0 Vdo to VEE
Output Current:	was was and and it	Market transf. C fieldin
Continuous		50 mA
Surge		100 mA

Operating Conditions

SYMBOL	ENTERTREESEE	PARAMETER	g Typical	MILITAR'		UNIT
VEE	Supply voltage	MONOLISE	V typical	-5.46 -5.2 -	4.94	V
TA	Operating free-air temperature	The second secon		0 Vm 081 m	75	°C
_	04	Plastic		-55	150	00
TSTG	Storage temperature range	Ceramic		-55	165	°C

Electrical Characteristics V_{EE} = -5.2 V ±5% (See Note)

SYMBOL		PARAMETER 7		oner Vicen°(signifur 2	5° ni-S ba	D 8 8 8 8 17	5°10 M on	willy
SYMBOL	PARA	AMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
I _E	Power supply curre	ent 100	21.7	112	is a lunch	102	pels, This	112	mA
	The state of the s	Pins 5, 6, 9, 11, 12, 13	- 4	405	sero n, on	255	noiteargo	255	Byong
linH =	Input current HIGH	Pins 7, 10	1	416	_	260	_	260	μΑ
196	T-C	Pins 4,	_	510	_6/8	320	Funct	320	110
linL	Input current LOW		0.5	ے ا	0.5	.6 _	0.3	_T0	μΑ
VOH	HIGH output voltage	ge	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
VOL	LOW output voltag	e 81 08.5	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
V _{IH}	HIGH input voltage)	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
VIL	LOW input voltage		-1.95	-1.48	-1.95	-1.48	-0.95	-1.45	Vdc

Switching Characteristics V_{EE} = -5.2 V, ±5% (See Note)

OVIMBOL	245	PARAMETER)°	2	5°	75	°	דומט
SYMBOL	PAH	AMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
^t pd	Propagation delay	OW	1.1	2.0	1.0	2.0	S 1.4 - 0	2.1	ns
thold	Hold time	[8][8]	1.0	_	1.0	_	1.0	ю —	ns
	SO DUV DIN	Data	1.5	-	1.5	_	1.5	o -	
t _{set}	Setup time	Select	3.0		3.0	_	3.0	261	ns
t _r , t+	Rise time		0.5	2.4	0.5	2.4	0.5	2.4	ns
t _f , t-	Fall time	HS H	0.5	2.4	0.5	2.4	0.5	2.4	ns
^f shift	Shift frequency		250	_	250	_	250	_	MHz

NOTE: Each ECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50Ω resistor to -2.0 V.

Description (Continued)

the four possible operations of the register without external gating of the clock. The flip-flops shift information on the positive edge of the clock. The four operations are stop shift, shift-left, shift-right, and parallel entry of data. The other six inputs are all data

type inputs; four for parallel entry data, and one for shifting in from the left (DL) and one for shifting in from the right (DR). This device is a functional/pinout duplication of the standard ECL 10K part, with 100% improvement in propagation delay and operation frequency and no increase in power supply current.

ECL 10KH High-Speed Emitter-Coupled Logic Family MC10H158 QUAD 2-Input Multiplexer

PRELIMINARY

This document contains specifications and information which are subject to change.

Features/Benefits

- · Propagation delay, 1.5 ns typical
- · Power dissipation, 197 mW typical
- Noise margin 150 mV
- Voltage compensated
- ECL 10K-Compatible

Description

The MC10H158 is a member of Monolithic Memories' ECL Family. The MC10H158 is a quad 2-input multiplexer. When the select line (SELECT) is LOW D_1 data appear at the outputs (Q3-Q0). Conversely, when the select input is HIGH, D_0 data appear at the outputs. This ECL part is a functional/pinout duplication of the standard ECL 10K family part, with 100% improvement in propagation delay and no increase in power-supply current.

MC10H158 Function Table

SELECT	D_0*	D_1* a.a	Q
sby L est.o-	X	18.0- L 88.0-	NLO-
56V 4 38.1	X	sa.r- H so.r-	.eH₁
oby H set o	V.L	18.0- X SET	aL.
H as a	Н	X	Н

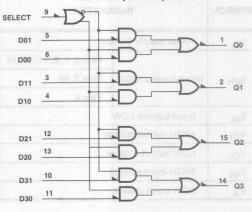
D_0/D_1 indicate each of four bit positions for the "zero" or "one" inputs, as controlled by the select line.

Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
MC10H158	J,N,NL(20)	Com

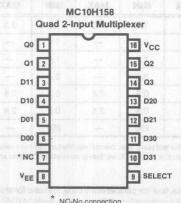
Logic Diagram

MC10H158 Quad 2-Input Multiplexer



V_{EE} Pin 8 V_{CC} Pin 16

Pin Configurations



3 2 1 20 19 Q0 NC VCC Q2 4 Q3 18 D11 5 D10 D20 17 ECL10KH 6 QUAD NC 16 NC 2-INPUT 7 MUX D01 D21 15 8 D30 NC VEE NC SEL D31 10 11 12

MC10H158

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TWX: 910-338-2376

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X = Don't care.

Supply voltage, V _E (V _{CC} = 0). Input voltage, V _I (V _{CC} = 0). Output Current:	
Output Current: Continuous	E0 == A
Surge	100 mA

Operating Conditions

SYMBOL		PARAMETER				
VEE	Supply Voltage	Logic Dis-	-5.46 -5.2 -4.94	٧		
TA	Operating temperature range		0 75	°C		
Toro	Storage temperature range	Plastic AGE Teacher Middle	-55 150	°C		
TSTG	all and a supplied an	Ceramic Paragraph profession	-55 105	- din		

Electrical Characteristics V_{EE} = -5.2 V ±5% (See Note)

CVMPOL	6.1		0°		25°		75°		UNIT
SYMBOL	PARAM	PARAMETER		MAX	MIN	MAX	MIN	MAX	UNI
I _E	Power supply current		_	9 53	LG + *s_	48	99.6 6	53	mA
l _{inH}	Input current HIGH	Pin 9	-	475	1 - >	295	1 -	295	μА
INH		Pins 3-6 and 10-13	_	515	8 4 X	320	3 —	320	
linL	Input current LOW		0.5	#	0.5	_	0.3		μΑ
VOH	HIGH output voltage	158	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
V _{OL}	LOW output voltage		-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
V _{IH}	HIGH input voltage		-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
VIL	LOW input voltage		-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

Switching Characteristics V_{EE} = -5.2 V, ±5% (See Note)

SYMBOL	PARAMETER		0°		25°		75°		
			MIN	MAX	MIN	MAX	MIN	MAX	UNIT
	Propagation delay	Data	0.5	1.9	0.5	1.9	0.5	2.0	ns
^t pd		Select	1.0	2.9	1.0	2.9	1.0	2.9	
t _r , t+	Rise time	Man 3	0.7	2.2	0.7	2.0	0.7	2.2	ns
t, t	Fall time		0.7	2.2	0.7	2.0	0.7	2.2	ns

NOTES: Each ECL 10 KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established.

The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 500 resistor to -2.0 V.

ECL 10KH High-Speed Emitter-Coupled Logic Family MC10H159

PRELIMINARY INFORMATION

This document contains specifications and information which are subject to change.

Quad 2-Input Inverting Multiplexer with Enable

Features/Benefits

- Propagation delay, 1.5 ns typical
- Power dissipation, 218 mW typical
- Noise margin 150 mV
- Voltage compensated
- ECL 10K-compatible

Description

The MC10H159 is a member of Monolithic Memories' ECL family. The MC10H159 is a quad 2-input inverting multiplexer with enable. A HIGH level on the enable input (ENABLE) overrides the select input (SELECT) and forces all of the outputs (Q3-Q0) to the LOW level. A LOW level on the enable input allows multiplexer action, which is controlled by the select input. When the select input is LOW, D_1 data appear at the outputs. Conversely, when the select input is HIGH, D_0 data appear at the outputs.

MC10H159 Function Table

ENABLE	SELECT	84	D_0*	D_1*	83 Q
A. L 803	- L	895	X	L	H
L 988	L	028	X	Н	BraL
Au L	8.8 H		L a	X	H
-0.736 J Vdc	Se H	18.0	H	X	8.0.L
H	X		X	X	L

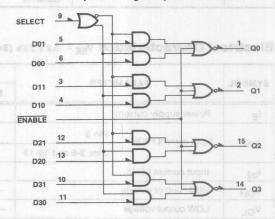
^{*} D_0/D_1 indicate each of 4 bit positions for the "zero" or "one" inputs, as controlled by the select line.

Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
MC10H159	J,N,NL(20)	Com

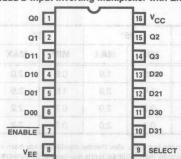
Logic Diagram

MC10H159 Quad 2-Input Inverting Multiplexer with Enable

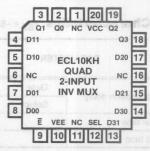


Pin Configurations

MC10H159 Quad 2-Input Inverting Multiplexer with Enable



MC10H159



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TWX: 910-338-2376

2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2374

Monolithic MM

X = Don't care.

Appointe maximam matinge	
Supply voltage V _{EE} (V _{CC} = 0)	-8.0 to 0 V _{dc}
Input voltage V _I (V _{CC} = 0)	0 V _{dc} to V _{EE}
Output Ourrent.	
Continuous	50 mA
Surge	100 mA

Operating Conditions

SYMBOL	PARAMETER					CIAL	UNIT
VEE	Supply voltage			-5.46	-5.2	-4.94	V
TA	Operating temperature range)		0		75	°C
TSTG	Storage temperature range	Plastic	of Manelithic Memories' new ECs.	-55	ngai(150	00
		Ceramic	Supremy generator chemics and an under	-55	or Palur orlay di	165	- °C

Electrical Characteristics V_{EE} = -5.2 V $\pm 5\%$ (See Note)

	OL PARAMETER -		0°		25°		75°		UNIT
SYMBOL			MIN	MAX	MIN	MAX	MIN	MAX	UNII
I _E			Power supply current	_	58	restamilio-	53	glin a a nily	58
675	Input current HIGH	Pin 9	_	475	mov field	295	171	295	μА
linH eq.		Pins 3-7 and 10-13		515	ero Tirk	320	151.	320	
linL	Input current LOW	Secretary Section	0.5	_	0.5	-	0.3	-	μΑ
VOH	HIGH output voltage)	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
VOL	LOW output voltage		-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
VIH	HIGH input voltage	TD follows are were	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
VIL	LOW input voltage		-1.95	-1.48	-1.95	-1.48	-1.75	-1.45	Vdc

Switching Characteristics V_{EE} = -5.2 V, $\pm 5\%$ (See Note)

SYMBOL	PARAMETER		0°		25°		75°		
			MIN	MAX	MIN	MAX	MIN	MAX	UNIT
^t pd		Data	0.5	2.2	0.5	2.2	0.5	2.2	
	Propagation delay Select Enable	Select	1.0	3.2	1.0	3.2	1.0	3.2	ns
		1.0	3.2	1.0	3.2	1.0	3.2		
t _r ,t+	Rise time		0.5	2.2	0.5	2.2	0.5	2.2	ns
t _f ,t-	Fall time		0.5	2.2	0.5	2.2	0.5	2.2	ns

Note: Each ECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established.

The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50 Ω resistor to -2.0 V.

ECL 10KH High-Speed **Emitter-Coupled Logic Family** MC10H160 12-Bit Parity Generator-Checker

Features/Benefits

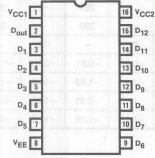
- Propagation delay, 2.5 ns typical
- · Power dissipation, 320 mW typical
- Noise margin 150 mV
- Voltage compensated
- ECL 10K-compatible

Description

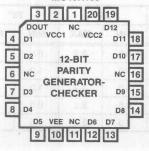
The MC10H160 is a member of Monolithic Memories' new ECL family. The MC10H160 is a 12-bit parity generator-checker. The output goes high when an odd number of inputs are high providing the odd parity function. Unconnected inputs are pulled to a logic low allowing parity detection and generation for less than 12 bits. The MC10H160 is a functional/pin out duplication of the standard ECL 10K family part with 100% improvement in propagation delay and no increase in power-supply current.

Pin Configuration

MC10H160 12-Bit Parity Generator-Checker



MC10H160

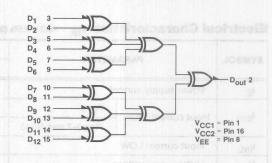


Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
MC10H160	J,N,NL(20)	Com

Logic Diagram

MC10H160 12-Bit Parity Generator-Checker



Function Table

INPUT SUM OF HIGH LEVEL INPUTS	OUTPUT PIN 2
Even	LOW
Odd	HIGH

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sociate maximalii riatingo	
wer supply V _{EE} (V _{CC} = 0 V)8.0 V to 0	Vdc
out voltage V _I (V _{CC} = 0 V)	VEE
tput Current:	
Continuous) mA
Surge) mA

Operating Conditions

SYMBOL	PARAMETER COMMERCIA MIN TYP MA						
VEE	Supply voltage	Telepolit .	-5.46 -	5.2 -4.94	V		
TA	Operating temperature range		0	+75	°C		
-	SAFORE SAFORE	Plastic	-55	+150	200		
TSTG	Storage temperature range	Ceramic	-55	+165	°C		

Electrical Characteristics V_{EE} = -5.2 V \pm 5% (See Note)

SYMBOL	PARAMETER		si goti C	l°	2	5°	75°		UNIT
STMBUL			MIN	MAX	MIN	MAX	MIN	MAX	DINIT
IE .	Power supply current		-	88	_	78	angitus.	86	mA
I _{inH} Input current HIGH	Pins 3,5,7,10,12,14	ert It :	391	D HUDSING	246	27 46 BI TI	246	AUE &	
	input current HIGH	_	457	tem oo rd	285	uch all eine	285	μΑ	
linL	Input current LOW	X X X X X N	0.5	_	0.5	_	0.3	_	μΑ
VOH	HIGH output voltage	X X X H X	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
VOL	LOW output voltage	e.sT.Inab × X	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
VIH	HIGH input voltage		-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
VIL	LOW input voltage	nar guilli olgani	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

Switching Characteristics V_{EE} = -5.2V $\pm 5\%$ (See Note)

SYMBOL	PARAMETER	0	0°		25°		75°	
		MIN	MAX	MIN	MAX	MIN	MAX	UNIT
^t pd	Propagation delay	1.1	3.1	1.1	3.3	1.2	3.5	ns
t _r , t+	Rise time	0.55	1.5	0.55	1.6	0.75	1.7	ns
t _f , t-	Fall time	0.55	1.5	0.55	1.6	0.75	1.7	ns

Note: Each ECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50 Ω resistor to -2.0 V.

ECL 10KH High-Speed Emitter-Coupled Logic Family MC10H161 Binary to 1-of-8 Decoder

Features/Benefits

- · Propagation delay, 1 ns typical
- · Power dissipation, 315mW typical
- Noise margin 150 mV
- Voltage compensated
- ECL 10K-compatible

Description

The MC10H161 is a high-speed Binary to 1-of-8 Decoder. This device is a member of Monolithic Memories' expanding ECL 10KH family. This ECL device is designed to decode a three-bit word to a one-of-eight line output. The selected output will be low while all other outputs will be high. The enable inputs, when either or both are high, force all outputs high.

The MC10H161 is a true parallel decoder. No series gating is used internally, eliminating unequal delay time found in other decoders. The MC10H161 is useful in high-speed multiplexer/demultiplexer applications.

This ECL 10KH part is a functional/pinout duplication of the standard ECL 10K part with 100% improvement in propagation delay, and no increase in power-supply current.

Pin Configuration

MC10H161 Binary to 1-of-8 Decoder

Ordering Information

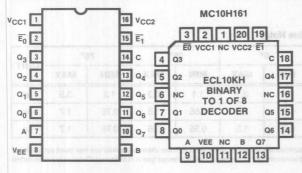
PART NUMBER	PACKAGE	TEMPERATURE
MC10H161	J,N,NL(20)	Com

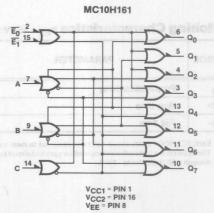
Truth Table

INPUTS INPUTS					OUTPUTS COTTO									
E ₁	E ₀	С	В	A	Q ₀	Q ₁	Q ₂	Q ₃	Q ₄	Q ₅	Q ₆	Q ₇		
L	L	L	L	L	L	Н	Н	Н	Н	Н	Н	Н		
L	(L)	L	L	Н	Н	L	Н	Н	Н	Н	Н	Н		
L	L	L	Н	L	Н	Н	L	Н	Н	Н	Н	Н		
L	L	L	Н	Н	Н	Н	Н	L	Н	Н	Н	Н		
L	L	Н	L	L	Н	Н	Н	Н	L	Н	Н	Н		
L	L	Н	L	Н	Н	Н	Н	Н	Н	L	Н	Н		
L	L	Н	Н	L	Н	Н	Н	Н	Н	Н	L	Н		
L	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L		
Н	X	X	X	X	Н	Н	Н	Н	Н	Н	Н	Н		
X	Н	X	X	X	Н	Н	Н	Н	Н	Н	Н	Н		

X = Don't Care

Logic Diagram





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TWX: 910-338-2376

Monolithic MM Memories Imitter Coupled Logic Family

Absolute Maximum Ratings

Supply voltage VEE (VCC = 0) Input voltage V (VCC = 0) Output Current:	. 0 Vdc to VEE
Continuous	
Surge	100 mA

Operating Conditions

SYMBOL	P	COMME MIN TY		UNIT	
VEE	Supply voltage	a seemal	-5.46 -5	.2 -4.94	V
TA	Operating temperature range	TURKI	0	75	°C
74 BD	c' 3 A Qa Qa Qa Qa Qa Qa	Plastic	-55	150	°C
TSTG	Storage temperature range	ed Blaary to 1-of-8 Decoder. This simple	-55	165	DM sri

Electrical Characteristics V_{EE} = -5.2 V ±5% (See Note)

SYMBOL	DADAMETER		jo ministra	2	5°	valeb rits	UNIT	
STMBUL	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNII
I _E	Power supply current		84	Elaub Jua	76	nut is a fue	84	mA
linH	Input current HIGH		465	rem e dt in	275	i mi <u>w</u> n sg	275	μΑ
l _{inL}	Input current LOW	0.5	_	0.5	Assidne se	0.3	-	μΑ
V _{OH}	HIGH output voltage	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	V _{dc}
V _{OL}	LOW output voltage	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	V _{dc}
V _{IH}	HIGH input voltage	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	V _{dc}
V _{IL}	LOW input voltage	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	V _{dc}

Switching Characteristics V_{EE} = -5.2V ±5% (See Note)

SYMBOL	PARAMETER		0°		25°		75°		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	UNIT
	Propagation delay Data Pins 7, 9, 14 Enable Pins 2, 15	Data Pins 7, 9, 14	0.6	2.0	0.65	2.1	0.7	2.2	3 50
^t pd		0.8	2.3	0.8	2.4	0.9	2.5	ns	
t _r , t+	Rise time		0.55	1.7	0.65	1.8	0.7	1.9	ns
t _f , t-	Fall time	11	0.55	1.7	0.65	1.8	0.7	1.9	ns

Note: Each ECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50 Ω resistor to -2.0 V.

ECL 10KH High-Speed Emitter Coupled Logic Family MC10H162 Binary to 1-of-8 Decoder

Features/Benefits

- Propagation delay 1 ns typical
- Power dissipation, 315 mW typical
- Noise margin 150 mV
- Voltage compensated
- ECL 10K-compatible

Description

The MC10H162 is a high-speed Binary to 1-of-8 Decoder. This device is a member of Monolithic Memories' ECL 10KH family. This ECL device is designed to convert a three-bit word to one-of-eight output lines. The selected output will be high while all other outputs are low. The enable inputs, when either or both are high, force all outputs low.

The MC10H162 is a true parallel decoder. This eliminates unequal parallel path delay times found in other decoder designs. This device is ideally suited for high-speed multiplexer/demultiplexer applications.

This ECL 10KH part is a functional/pinout duplication of the standard ECL 10K part with 100% improvement in propagation delay and no increase in power-supply current.

Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
MC10H162	J,N,NL	Com

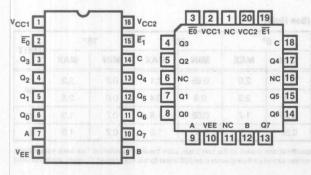
Truth Table

- 1	INPUTS				51 91	ulate	0	UTPL	JTS			
ĒΟ	Ē1	С	В	A	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7
L	L	L	L	L	Н	L	L	L	L	L	L	L
L	L	L	L	Н	L	Н	L	L	L	L	L	L
L	L	L	Н	L	L	L	Н	L	L	L	L	L
L	L	L	н	Н	L	L	L	Н	L	L	L	L
L	L	Н	L	L	L	L	L	L	Н	L	L	L
L	L	Н	L	Н	L	L	L	L	L	Н	E	L
L	L	Н	Н	L	L	L	L	L	L	L	Н	L
L	L	Н	Н	Н	L	L	L	L	L	L	L	Н
Н	X	X	X	X	L	L	L	L	L	L	L	L
X	Н	Х	X	X	L	L	- Lu	L	L	L	L	L

X = Don't Care.

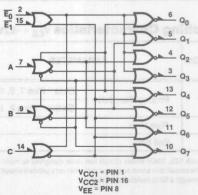
Pin Configurations

MC10H162 Binary to 1-of-8 Decoder (Inverting)



Logic Diagram

MC10H162 Binary to 1-of-8 Decoder



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TWX: 910-338-2376

Monolithic MM Memories

Supply voltage VEE (VCC = 0) -8.0 V to 0 Vdc Input voltage V _I (VCC = 0) 0 Vdc to VEE
Output Current:
Continuous
Surge

Operating Conditions

SYMBOL		PARAMETER				
VEE	Supply voltage		-5.46 -5	5.2 -4.94	V	
TA	Operating temperature range	OM 81-7	0	75	°C	
		Plastic	-55	150	00	
TSTG Storage tempera	Storage temperature range	Ceramic	-55	165	°C	

Electrical Characteristics V_{EE} = -5.2 V $\pm 5\%$ (See Note)

	and the second	0. serveror		2	5°	75°		UNIT
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNII
I _E	Power supply current		84	-	76	_	84	mA
linH	Input current HIGH	p	465	-	275	_	275	μΑ
linL	Input current LOW	0.5	1+1	0.5	_	0.3	_	μΑ
VOH	HIGH output voltage	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
VOL	LOW output voltage	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
VIH	HIGH input voltage	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
VIL	LOW input voltage	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

Switching Characteristics V_{EE} = -5.2V $\pm 5\%$ (See Note)

SYMBOL	PARAMETER		0°		25°		75°		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	UNII
	Propagation delay Data Enable	Data	0.7	2.0	0.7	2.1	0.8	2.5	
^t pd		0.8	2.3	0.8	2.4	0.9	2.6	ns	
t _r , t+	Rise time		0.6	1.8	0.6	1.9	0.6	2.0	ns
t _f , t-	Fall time		0.6	1.8	0.6	1.9	0.6	2.0	ns

Note: Each ECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established.

The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50 Ω resistor to -2.0 V.

Typical Applications

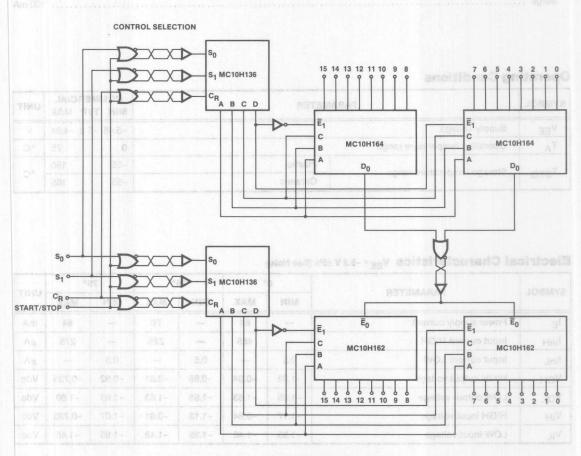
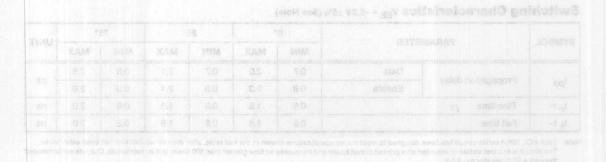


Figure 1. High Speed 16-Bit Multiplexer/Demultiplexer



ECL 10KH High-Speed Emitter-Coupled Logic Family MC10H164 8-Line Multiplexer

Features/Benefits

- · Propagation delay, 1 ns typical
- · Power dissipation, 310 mW typical
- Noise margin 150 mV
- Voltage compensated
- ECL 10K-compatible

Description

The MC10H164 is a member of Monolithic Memories' ECL family. This ECL 10KH part is a functional/pinout duplication of the standard ECL 10K part, with 100% improvement in propagation delay, and no increase in power supply current.

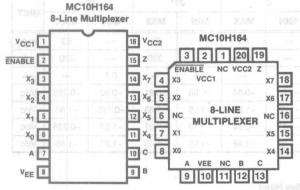
Pin Configuration

Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
MC10H164	J,N,NL(20)	Com

The MC10H164 is designed to be used in data multiplexing and parallel-to-serial conversion applications. Full parallel gating provides equal delays through any data path. The MC10H164 incorporates an output buffer, eight inputs and an enable. A high on the enable forces the output low. The open emitter output allows the MC10H164 to be connected directly to a data bus. The enable line allows an easy means of expanding to more than eight lines using additional MC10H164s.

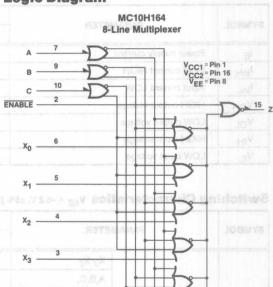
Logic Diagram



Truth Table

EJ.An	ADI	DRESS INP	UTS	OAM:			
ENABLE	С	В	A	Z			
Las	ь	8.dL	to L	X0			
en L as	L	a cL	8.6 H	X1			
L	L	а Н	, L	X2			
L	L	н	Н	X3			
L	Н	L	L	X4			
L	Н	L	Н	X5			
L	Н	Н	5.0° L	X6			
at vero re j anjahoo	muni H lupa k	mer Hart e	certe H prop	X7			
Н	X	Х	X	L			

X = Don't Care



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Monolithic Memories

TWX: 910-338-2376

14-59

Supply voltage V _{EF} (V _{CC} =0)	-8.0 V to 0 V _{dc}
Input Voltage V _I (V _{CC} =0)	0 V _{dc} to V _{EE}
Output current:	
Continuous	50 mA
Surge	

Operating Conditions

SYMBOL	PARAMETER		COMMERCIAL MIN TYP MAX	UNIT
VEE	Supply voltage		-5.46 -5.2 -4.9	4 V
TA	Operating free-air temperature		0 7	°C
ald A. sidad	ercordo sense and ordon confer eight imposeend an e	Plastic	-55 15	
TSTG	Storage temperature range	Ceramic	-55	°C

Electrical Characteristics V_{EE} = -5.2 V±5% (See Note)

	497H015H	0°		25	5°	7	LIBUT	
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNI
I _E	Power supply current	- A - - -	83	P.339	75		83	mA
linH	Input current HIGH	a	512		320	1 -	320	μΑ
linL	Input current LOW	0.5	3 4004 2	0.5	x T++D	0.3	- 1	μΑ
VOH	HIGH output voltage	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
VOL	LOW output voltage	-1.95	-1.63	-1.95	-1.63	-0.735	-1.60	Vdc
VIH	HIGH input voltage	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
VIL	LOW input voltage	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

Switching Characteristics V_{EE} = -5.2 V, ±5% (See Note)

	PARAMETER		(0°		25°		75°	
SYMBOL			MIN	MAX	MIN	MAX	MIN	MAX	UNIT
		X ₀ -X ₇	1.0	2.8	0.7	2.7	0.7	2.9	
		A,B,C,	1.0	3.8	0.7	3.6	0.7	3.9	
t _{pd}	Propagation delay	Data	0.7	2.4	0.8	2.5	0.9	2.6	ns
		Address	1.0	2.8	1.1	2.9	1.2	3.2	-
		Enable	0.4	1.45	0.4	1.5	0.5	1.7	-
t _r ,t+	Rise time Fall time		0.6	1.8	0.6	1.9	0.6	2.0	ns
t _f ,t-			0.6	1.8	0.6	1.9	0.6	2.0	ns

Note: Each ECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50 Ω resistor to -2.0 V.

ECL 10KH High-Speed Emitter Coupled Logic Family MC10H166 5-Bit Magnitude Comparator

Features/Benefits

- · Propagation delay, Data-to-Output, 2.0 ns typical
- · Power dissipation, 440 mW typical
- Noise margin 150 mV
- Voltage compensated
- ECL 10K-compatible

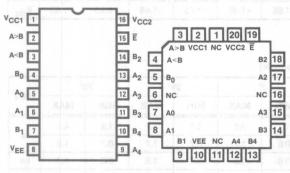
Description

The MC10H166 is a member of Monolithic Memories' ECL 10KH family. This device is a 5-Bit Magnitude Comparator and is a functional/pinout duplication of the standard ECL 10K part with 100% improvement in propagation and no increase in power-supply current.

The MC10H166 is a high-speed expandable 5-bit comparator for comparing the magnitude of two binary words. Two outputs are provided: A < B and A > B. The A = B function can be obtained by wire-ORing these outputs (a low level indicates A = B) or by wire-NORing the outputs (a high level indicates A = B). A high level on the enable function forces both outputs low.

Pin Configurations

MC10H166
5-Bit Magnitude Comparator



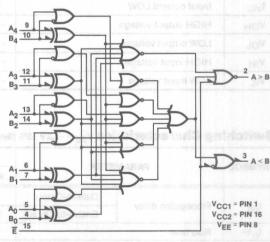
Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE		
MC10H166	J,N,NL	Com		

Truth Table

aO	INPU	TS	OUT	PUTS
Ē	Α	В	A < B	A > B
Н	X	Х	L	L
L	Word A	= Word B	L	L
L	Word A	> Word B	prog Losso	Н
L	Word A	< Word B	Н	L

Logic Diagram



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Monolithic MM Memories

MC10H166

Absolute Maximum Ratings

Supply voltage VEE (VCC = 0) Input voltage VI (VCC = 0)	 	-8.0 V to 0 Vdc
Output Current:		
Continuous	 	50 mA
Surge	 	100 mA

Operating Conditions

SYMBOL	PAR	COMMERCIAL MIN TYP MA	LIMIT	
VEE	Supply voltage	-5.46 -5.2 -4.9)4 V	
TA	Operating temperature range	Operating temperature range		5 °C
-		Plastic	-55 15	
TSTG	Storage temperature range Ceramic		-55 16	°C

Electrical Characteristics V_{EE} = -5.2 V ±5% (See Note)

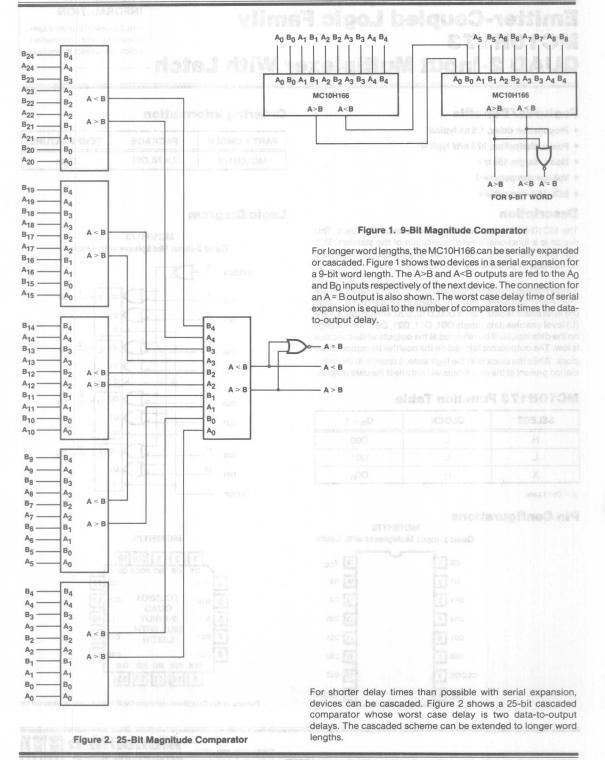
Ordering Information

	World A < World B	0	0°		25°		75°	
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
I _E	Power supply current	_	117	ol z i y duc	106	ot ne llo nul	eld117 or	mA
linH	Input current HIGH	20.d _	350	-	220	_	220	μА
linL	Input current LOW	0.5	-	0.5	- 3	0.3	ug <u>E</u> no	μΑ
Vон	HIGH output voltage	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	V _{dc}
VOL	LOW output voltage	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	V _{dc}
VIH	HIGH input voltage	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	V _{dc}
VIL	LOW input voltage	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

Switching Characteristics V_{EE} = -5.2V ±5% (See Note)

SYMBOL	PARAMETER		0°		2	5°	75°		
STMBUL			MIN	MAX	MIN	MAX	MIN	MAX	UNIT
• c 6865	VD-passetion date:	Data-to-Output	1.1	3.5	1.1	3.7	1.2	4.1	173.8
^t pd	Propagation delay	Enable-to-Output	0.6	1.7	0.7	1.7	0.7	1.8	ns
t _r , t+	Rise time		0.6	1.5	0.6	1.6	0.6	1.7	ns
t _f , t-	Fall time		0.6	1.5	0.6	1.6	0.6	1.7	ns

Note: Each ECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-Ω resistor to -2.0 V.



ECL 10KH High-Speed Emitter-Coupled Logic Family MC10H173 **QUAD 2-Input Multiplexer With Latch**

PRELIMINARY INFORMATION

This document contains specifications and information which are subject to change.

Features/Benefits

- Propagation delay, 1.5 ns typical
- Power dissipation, 275 mW typical
- Noise margin 150 mV
- Voltage compensated
- ECL 10K-compatible

Description

The MC10H173 is a guad 2-input multiplexer with latch. This device is a functional/pinout duplication of the standard ECL 10K part, with 100% improvement in propagation delay and no increase in power-supply current.

It incorporates common clock and common data select inputs. The select input determines which data input is enabled. A high (H) level enables data inputs D00, D10, D20, and D30 and a low (L) level enables data inputs D01, D11, D21, D31. Any change on the data input will be reflected at the outputs while the clock is low. The outputs are latched on the positive transition of the clock. While the clock is in the high state, a change in the information present at the data inputs will not affect the data outputs.

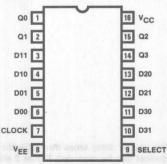
MC10H173 Function Table

SELECT	CLOCK	Q _n = 1
Н	L	D00
L	L	D01
X	Н	Q0 _n

X = Don't care.

Pin Configurations

MC10H173 Quad 2-Input Multiplexer with Latch

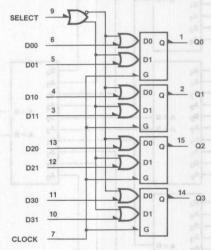


Ordering Information

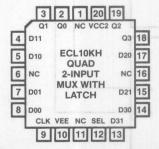
PART NUMBER	PACKAGE	TEMPERATURE
MC10H173	J,N,NL(20)	Com

Logic Diagram

MC10H173 Quad 2-Input Multiplexer with Latch



MC10H173



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TWX: 910-338-2376



Supply voltage, V _{EE} (V _{CC} = 0)	-8.0 to 0 V _{dc}
Input voltage, V _I (V _{CC} = 0)	0 V _{dc} to V _{EE}
Output Current:	
Continuous	50 mA
Surge.	100 mA

Operating Conditions

SYMBOL	OK SMALL TP	COMMERCI MIN TYP M		
VEE	Supply voltage	-5.46 -5.2 -	4.94 V	
TA	Operating temperature range	0.0000	0	75 °C
_	PET PROPERTY.	Plastic	-55	150
TSTG	Storage temperature range	Ceramic	-55	165 °C

Electrical Characteristics V_{EE} = -5.2 V ± 5% (See Note)

OVERDOL	Account of the control of the contro		0°		25°		75°		UNIT
SYMBOL	PARAM	PARAMETER		MAX	MIN	MAX	MIN	MAX	UNII
E	Power supply current		_	73	_	66	DMT -	73	mA
e vola - pr		Pins 3-7 and 10-13	_	510	183	320	01-016-10	320	
linH	Input current HIGH	Pin 9	_	475	-	300	100	300	μΑ
linL	Input current LOW	- 87 - pY	0.5	_	0.5	_	0.3	_	μА
VOH	HIGH output voltage	V 20 1 1 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
VOL	LOW output voltage	\$1 - KX	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
VIH	HIGH input voltage		-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
VIL	LOW input voltage		-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

Switching Characteristics V_{EE} = -5.2 V, $\pm 5\%$ (See Note)

OVMBOL	PARAMETER		0°		25°		75°		
SYMBOL			MIN	MAX	MIN	MAX	MIN	MAX	UNIT
		Data	0.7	2.3	0.7	2.3	0.7	2.3	
t _{pd}	Propagation delay	Clock	1.0	3.7	1.0	3.7	1.0	3.7	ns
07		Select	1.0	3.6	1.0	3.6	1.0	3.6	
t _{set}	Setup time	Data	0.7	_	0.7	- Par	0.7	31-	ns
set		Select	1.0	-	1.0	707	1.0	9	110
thold	Hold time	Data	0.7	1 - 1	0.7	_X178	0.7	1	ns
'noia	Tiola time	Select	1.0	-	1.0	_	1.0	8_	
t _r , t+	Rise time		0.7	2.4	0.7	2.4	0.7	2.4	ns
t _f , t-	Fall time		0.7	2.4	0.7	2.4	0.7	2.4	ns

NOTE: Each ECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50Ω resistor to -2.0 V.

ECL 10KH High-Speed Emitter-Coupled Logic Family MC10H174 Dual 4-to-1 Multiplexer

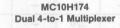
Features/Benefits

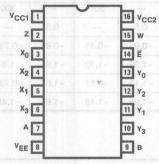
- Propagation delay 1.5 ns typical
- Power dissipation, 305 mW typical
- Noise margin 150 mV
- Voltage compensated
- ECL 10K-compatible

Description

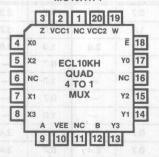
The MC10H174 is a Dual 4-to-1 Multiplexer. This device is a member of Monolithic Memories' new ECL family. This device is a functional/pinout duplication of the standard ECL 10K part with 100% improvement in propagation delay, and no increase in power-supply current.

Pin Configuration





MC10H174

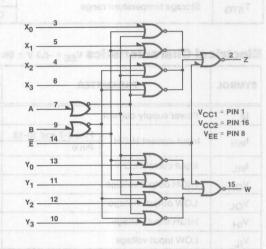


Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
MC10H174	J,N,NL(20)	Com

Logic Diagram

MC10H174



Function Table

ENABLE	ADDRESS	INPUTS	PUTS OUTPU	
Ē	В	Α	Z	W
Н	Х	X	L	L
L	L	L	X ₀	Yo
L	L	Н	X ₁	Y ₁
L	Н	Emit dr	X ₂	Y ₂
L	н	Н	Х3	Y3

X = Don't care.

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TWX: 910-338-2376
TWX: 910-338-2374

Monolithic Memories

Supply voltage V _E (V _{CC} = 0) Input voltage V _I (V _{CC} = 0) Output Current:	0 Vdc to VEE
Output Current: Continuous Surge	50 mA

Operating Conditions

SYMBOL	2 (CS), MA,M,L	PARAMETER	COMMERCIAL MIN TYP MAX	UNIT
VEE	Supply voltage	Alternatives B	-5.46 -5.2 -4.94	V
TA	Operating temperature range	The Morelland	0 75	°C
0.0		-55 150	0.0	
	Storage temperature range	Ceramic	-55 165	°C

Electrical Characteristics V_{EE} = -5.2 V ±5% (See Note)

CVMDOL	m ser mes color ser en grand a retreat de l'apparin	noiter to the sit is agos	do 0° que lewid o		2	5° 00 00	75°		UNIT																											
SYMBOL	PARAMETER		MIN	MAX	MIN	MAX ®	MIN	MAX	UNIT																											
lE .	Power supply current		Power supply current —	_ 80 _ 73	_ 80 - 73	_ 80 _ 73 		_ 80 _ 73 _ <u>8</u>	_ 80 · _ 73	_ 80 _ 73 _ _	_ 80 _ 73 _ _	_ 80 _ 73 _	_ 80 _ 73 _ _	_ 80 <u>_</u> 73	_ 80		_ 80	_ 80	_ 80	_ 80	_ 80	_ 80	- 80 - 73 - 3	- 80 - 73 - 3 - 3 - 3 - 3 - 3 - 3 - 3 - 3 -	- 80 - 73	- 80 - 73 -	_ 80 _ 73 _	- 80 - 73 - 8	- 80 - 73 -	_ 80 -	_ 80	_ 80	80 - 73 - 3	ar all terin	80	mA
Input current HIGH	Pins 3 - 7 and 9 - 13		475	_	300	- 3	300																													
	'inH	Pin 14	_	670	_	420	The same	420	μА																											
linL	Input current LOW	Ø1	0.5	_	0.5		0.3	_	μΑ																											
VOH	HIGH output voltage	0-	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc																											
VOL	LOW output voltage		-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc																											
v_{IH}	HIGH input voltage		-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc																											
VIL	LOW input voltage	the same of the sa	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc																											

Switching Characteristics V_{EE} = -5.2 V, $\pm 5\%$ (See Note)

SYMBOL	PARAMETER		0°		2	25°		75°		
			MIN	MAX	MIN	MAX	MIN	MAX	UNIT	
t _{pd}	Personal Property and Property	Data (All others)	0.7	2.4	0.8	2.3	0.9	2.6	T a	
	Propagation delay Select (A,B) Pin 7	Propagation delay Select (A,B) Pin 7, 9 Enable Pin 14	Propagation delay Select (A,B) Pin 7, 9 1	pagation delay Select (A,B) Pin 7, 9 1.0 2.	2.8	1.1	2.9	1.2 3.2	3.2	ns
			0.4	1.45	0.4	1.50	0.5	1.70		
t _r , t+	Rise time		0.5	1.5	0.5	1.6	0.5	1.70	ns	
t _f , t-	Fall time		0.5	1.5	0.5	1.6	0.5	1.70	ns	

Note: Each ECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm maintained. Outputs are terminated through a 50Ω resistor to -2.0 V.

MC10H175 Quint Latch

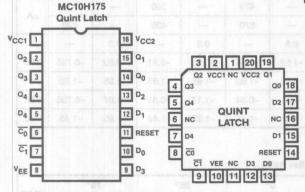
Features/Benefits

- Propagation delay, 1.2 ns typical
- Power dissipation, 400 mW typical
- Noise margin 150 mV
- Voltage compensated
- ECL 10K-compatible

Description

The MC10H175 is a member of Monolithic Memories' ECL family. The MC10H175 is a quint D-type latch with common reset and clock lines. This ECL 10KH part is a functional/pinout duplication of the standard ECL 10K part, with 100% improvement in propagation delay, and no increase in power-supply current.

Pin Configuration



Truth Table

D	C ₀	C ₁	RESET	Q _{n+1}
L	L	L	X	L
Н	L	L	X	Н
X	Н	X	L	Qn
X	X	Н	L	Qn
X	Н	X	artin, a (eH bernal e	desident in Law
X	X	Н	Н	L

X = Don't Care

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Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
MC10H175	J,N,NL(20)	Com

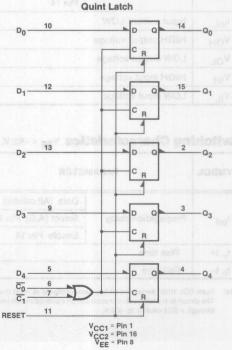
Application Information

The MC10H175 is a high-speed, low-power quint latch. It features five D-type latches with common reset and a common two-input clock. Data is transferred on the negative edge of the clock and latched on the positive edge. The two clock inputs are ORed together.

Any change on the data input will be reflected at the outputs while the clock is low. The outputs are latched on the positive transition of the clock. While the clock is in the high state, a change in the information present at the data inputs will not affect the output information. The reset input is enabled only when the clock is in the high state.

Logic Diagram

MC10H175



Monolithic Memories

Supply Voltage V_{EE} (V_{CC} = 0) —8 Input Voltage V_{I} (V_{CC} = 0) Output Current:	0 V _{dc} to V _{EE}
Continuous Surge	50 mA

Operating Conditions

SYMBOL	PAI	MIN	MMERC TYP	IAL MAX	UNIT	
VEE	Supply voltage	a'i' nifurii	-5.46	-5.2	-4.94	٧
TA	Operating temperature range	Operating temperature range			75	°C
T _{STG}	Charles Large Lie descriptive	Plastic	-55		150	°C
	Storage temperature range	Ceramic (1907) 20 d responsivi of the	-55	rdne m	165	TOM

Electrical Characteristics V_{EE} = -5.2 V ±5% (See Note)

01/11/01	CHARACTERISTIC		0	0° 0, salt o la 100 25° not sm			oksi fusi 7	Con the	
SYMBOL	CHARAC	CHARACTERISTIC		MAX	MIN	MAX	MIN	MAX	UNIT
lE	Power supply current		- a	107	ener ci loro	97	w - 05	107	mA
Input current HIGH	Pins 5,6,7,9,10,12,13	- 4	565	ingion on	335	nau <u>r.</u> sq	335	A	
	Pin 11		_	1120	_	660	_	660	μΑ
linL	Input current LOW	1	0.5	_	0.5	_	0.3	_	μΑ
VOH	HIGH output voltage		-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
VOL	LOW output voltage	-	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
VIH	HIGH input voltage		-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
VIL	LOW input voltage		-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

Switching Characteristics V_{EE} = -5.2 V, ±5% (See Note)

CVMDOL	PARAMETER		an to (0° 2		5°	75°		
SYMBOL			MIN	MAX	MIN	MAX	MIN	MAX	UNIT
	hound	Data	0.6	1.6	0.6	1.6	0.6	1.7	lian .
^t pd	Propagation delay Clock Reset	Clock	0.7	1.9	0.7	2.0	0.8	2.1	ns
		1.0	2.2	1.0	2.3	1.0	2.4	Section 1	
^t set	Setup time		1.5	ia n ai	1.5	- 5	1.5	_	ns
^t hold	Hold time		0.8	-	0.8	30000	0.8		ns
t _r , t+	Rise time		0.5	1.8	0.5	1.9	0.5	2.0	ns
t _f , t-	Fall time		0.5	1.8	0.5	1.9	0.5	2.0	ns

Note: Each ECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50 Ω resistor to -2.0 V.

ECL 10KH High-Speed Emitter Coupled Logic Family MC10H176 **Hex D Master-Slave Flip-Flop**

Features/Benefits

- Propagation delay 1.7 ns typical
- Power dissipation, 460 mW typical
- Noise margin 150 mV
- Voltage compensated
- ECL 10K-compatible

Pin Configurations

Description

The MC10H176 is a member of Monolithic Memories' ECL 10KH family. This ECL device includes six high speed master-slave D-type flip-flops with one common input clock for all six. Data enters into the master during the LOW state of the clock and is transferred to the slave during the positive-going clock transition. Thus, outputs may change only on a positive-going Clock transition. A change in information present at the data (D) input will not affect the output information any other time due to the master-slave construction of this device.

This ECL 10KH part is a functional/pinout duplication of the standard ECL 10K part, with 100% improvement in clock frequency and propagation delay and no increase in powersupply current.

Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
MC10H176	J,N,NL(20)	Com

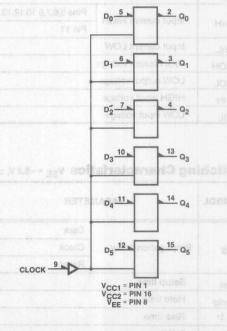
Truth Table

C	na outs p onet pr	Q _{n+1}
L	temper,Xure range	eganois Qn etat
H*	L	L
H*	Н	Н

X = Don't Care

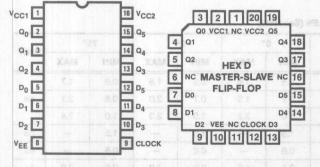
Logic Diagram

MC20H176 Hex D Master-Slave Flip-Flop



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MC10H176 Hex D Master-Slave Flip-Flop



TWX: 910-338-2376

2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2374

A clock H is a clock transition from a low to a high state

Emitter-Coupled Logic Family

Absolute Maximum Ratings

Supply voltage V _E E (V _{CC} = 0)	
Output Current:	MADER TIMES DESCRIPTION
Continuous	50 mA
Surge	100 mA

Operating Conditions

SYMBOL		PARAMETER		MERCIAL TYP MAX	UNIT
VEE	Supply voltage		-5.46	-5.2 -4.94	V
TA	Operating temperature range		0	75	°C
_	Stores to many time	Plastic a si epir alb sir? Jool 9 ymp0 ba	-55	150	0.0
TSTG	Storage temperature range	Ceramic Vilms HMOT JOE to	-55	165	°C

Electrical Characteristics V_{EE} = -5.2 V ±5% (See Note)

CVMDOL	PARAMETER		0°		25°		75°		
SYMBOL			MIN	MAX	MIN	MAX	MIN	MAX	UNIT
I _E	Power supply current		_	123		112	7-9	123	mA
		Pins 5,6,7,10,11,12	_	425	Tank	265	-	265	
linH	Input current HIGH	Pin 9	_	670	2 [23]	420	1-1	420	μΑ
linL	Input current LOW	61 61	0.5	_	0.5	_	0.3		μΑ
Vон	HIGH output voltage		-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	V _{dc}
VOL	LOW output voltage	86 (60 - 91 - 92 × 93)	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	V _{dc}
VIH	HIGH input voltage	G 19 - 19 - 19 - 19 - 19 - 19 - 19 - 19	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	V _{dc}
VIL	LOW input voltage		-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	V _{dc}

Switching Characteristics V_{EE} = -5.2V ±5% (See Note)

SYMBOL	quiring http://speed.it/fillmetid.go/resign.com/ing	0°		25°		75°		
	PARAMETER EXTENDED A PARAMETER EXTENDED A PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
t _{pd}	Propagation delay	0.9	2.1	0.9	2.2	1.000	2.4	ns
t _{set}	Setup time as a set so we read reported	1.5	-13	1.5	GAS <u>IN</u> A-1	1.5	33 -	ns
^t hold	Hold time	0.9		0.9	-	0.9	7] -	ns
t _r , t+	Rise time was been so used as in 801H010M a	0.5	1.8	0.5	1.9	0.5	3 2.0	ns
t _f , t-	Fall time	0.5	1.8	0.5	1.9	0.5	2.0	ns
ftog	Toggle frequency	250	_	250	Net House	250	_	ns

Note: Each ECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established.

The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50 Ω resistor to -2.0 V.

Look-Ahead Carry Block

Features/Benefits

- · Propagation delay, 1 ns typical
- Power dissipation, 300 mW typical
- Noise margin 150 mV
- Voltage compensated
- ECL 10K-compatible

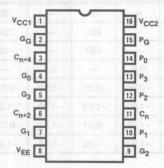
Description

The MC10H179 is a Look-Ahead Carry Block. This device is a member of Monolithic Memories' ECL 10KH family.

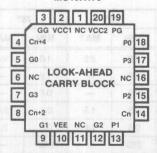
This ECL 10KH part is a functional/pinout duplication of the standard ECL 10K part with 100% improvement in propagation delay, and no increase in power-supply current.

Pin Configuration

MC10H179 Look-Ahead Carry Block



MC10H179

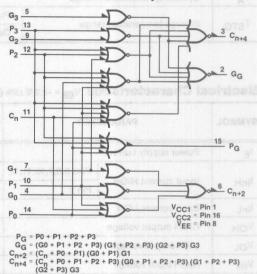


Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
MC10H179	J,N,NL(20)	Com

Logic Diagram

MC10H179 Look-Ahead Carry Block



Application

The MC10H179 is a high-speed, low-power, standard ECL complex function that is designed to perform the look-ahead carry function. This device can be used with the MC10H181 4-bit ALU directly, or with the MC10H180 dual arithmetic unit in any computer, instrumentation or digital communication application requiring high-speed arithmetic operation on long words.

When used with the MC10H181, the MC10H179 performs a second order or higher look-ahead. Figure 2 shows a 16-bit look-ahead carry arithmetic unit. Second order carry is valuable for longer binary words. As an example, addition of two 32-bit words is improved from 30 nanoseconds with ripple-carry techniques. A block diagram of a 32-bit ALU is shown in Figure 1. The MC10H179 may also be used in many other applications. It can, for example, reduce system package count when used to generate functions of several variables.

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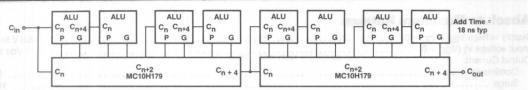


Figure 1. 32-Bit ALU with Carry Look-Ahead

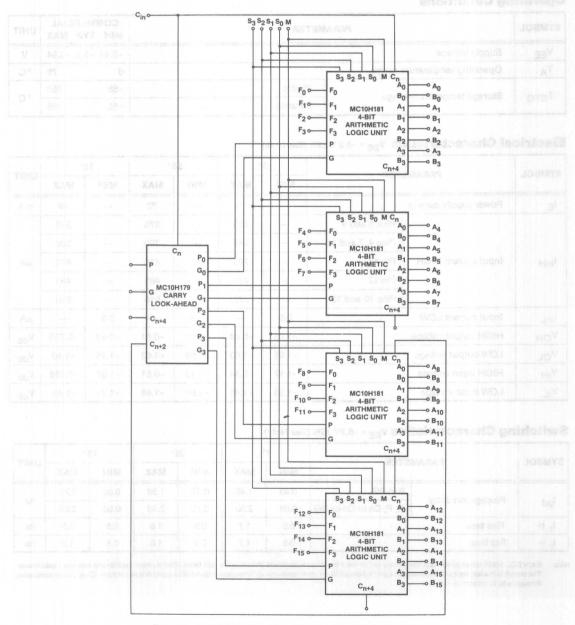


Figure 2. 16-Bit Full Look-Ahead Carry Arithmetic Logic Unit

Supply voltage VEE (VCC = 0)	-8.0 V to 0 Vdc
Input voltage V _I (V _{CC} = 0)	0 Vdc to VEE
Output Current:	
Continuous	50 mA
Surge	100 mA

Operating Conditions

SYMBOL	PARAMETER		COMMERCI.	LIMIT
VEE	Supply voltage		-5.46 -5.2 -4	4.94 V
TA	Operating temperature range		0	75 °C
_	0A 0 0A	Plastic	-55	150
TSTG Storage temperature range	Ceramic	-55	165 °C	

Electrical Characteristics V_{EE} = -5.2 V ±5% (See Note)

OVMOOL	200	60	0	10	2	5°	7	5°	
SYMBOL	PARAM	PARAMETER		MAX	MIN	MAX	MIN	MAX	UNIT
IE .	Power supply current			79		72	_	79	mA
		Pins 5 and 9		465	-	275	_	275	
		Pins 4, 7 and 11	427	545	p=	320	_	320	
linH	Input current HIGH	Pin 14	963	705	189	415	_	415	μΑ
		Pin 12		790	ET ann	465	_	465	
4A 00	Pins 10 and 13		870	DASH4	510	_	510		
linL	Input current LOW		0.5	HE	0.5	2000	0.3	_	μΑ
VOH	HIGH output voltage		-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	V _{dc}
VOL	LOW output voltage	,0 M g8 ,0 g8 y0	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	V _{dc}
V _{IH}	HIGH input voltage	63 63	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	V _{dc}
VIL	LOW input voltage	A MC10010M	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	V _{dc}

Switching Characteristics V_{EE} = -5.2V ±5% (See Note)

CVIADOI	DADA	Then ²)°	2	5°	7	5°	
SYMBOL	PARA	METER	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
	D	P to PG	0.40	1.40	0.40	1.50	0.50	1.70	
¹ pd	Propagation delay	G, P, Cn to Cn or GG	0.60	2.30	0.70	2.40	0.80	2.60	ns
t _r , t+	Rise time	10"	0.5	1.7	0.5	1.8	0.5	1.9	ns
t _f , t-	Fall time		0.5	1.7	0.5	1.8	0.5	1.9	ns

Note: Each ECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50 Ω resistor to -2.0 V.

ECL 10KH High Speed Emitter Coupled Logic Family MC10H209 Dual 4-5 Input OR/NOR Gate

Features/Benefits

- · Propagation delay, 0.75 ns typical
- 125 mW typical (no load)
- Noise margin 150 mV
- Voltage compensated
- ECL 10K-compatible

Ordering Information

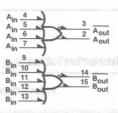
PART NUMBER	PACKAGE	TEMPERATURE
MC10H209	J,N,NL	Com

Logic Diagram

Description

The MC10H209 is a member of the Monolithic Memories' ECL 10KH Family. This ECL device is a dual 4-5 input OR/NOR gate. This device is a functional/pinout duplication of the standard ECL 10K family part, with 100% improvement in propagation delay and no increase in power supply current.

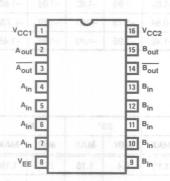
MC10H209 Dual 4-5 Input OR/NOR Gate



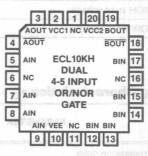
V_{CC1} = Pin 1 V_{CC2} = Pin 16 V_{EE} = Pin 8

Pin Configuration

MC10H209 Dual 4-5 Input OR/NOR Gate



MC10H209



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Input voltage V _I (V _{CC} = 0) .	0)	
Output current:		
Continuous		50 mA
Surge		100 mA

Operating Conditions

SYMBOL	PAI	RAMETER	COMMERC MIN TYP	IAL MAX	UNIT
VEE	Supply voltage		-5.46 -5.20 -	-4.94	V
TA	Operating temperature range		0	75	°C
т	Storage temporature range (1995)	Plastic	-55	150	°C
TSTG	Storage temperature range	Ceramic	-55	165	

Electrical Characteristics V_{EE} = -5.2 V ±5% (See Note)

SYMBOL	PARAMETER	0°		25°		75°		UNIT
	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	ONI
lE .	Power supply current		_	-	30	o i n ana	gi - na	mA
linH	Input current HIGH		640	-	400	_	400	μΑ
linL	Input current LOW	0.5	-	0.5	ISH U TOI	0.3	-	μΑ
VOH	HIGH output voltage	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
V _{OL}	LOW output voltage	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
VIH	HIGH input voltage	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
V _{IL}	LOW input voltage	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

Switching Characteristics V_{EE} = -5.2 V ±5% (See Note)

SYMBOL	PARAMETER	0°		25°		75°		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	UNIT
^t pd	Propagation delay	0.4	1.15	0.4	1.15	0.7	1.15	ns
t _r	Rise time	0.4	1.5	0.4	1.5	0.4	1.6	ns
t _f	Fall time	0.4	1.5	0.4	1.5	0.4	1.6	ns

Note: Each ECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established.

The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-Ω resistor to -2.0 V.

ECL 10 KH High-Speed Emitter-Coupled Logic Family MC10H210/MC10H211 3-Input, 3-Output OR/NOR Gates

Features/Benefits

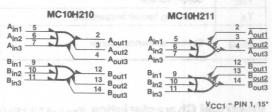
- · Propagation delay, 1.0 ns typical
- · Power dissipation, 160 mW typical
- Noise margin 150 mV (over operating voltage and temperature range)
- Voltage compensated
- ECL 10K-compatible

Description

The MC10H210 and MC10H211 are members of Monolithic Memories' ECL family. These devices are dual 3-input, 3-output "OR" and "NOR" gates respectively. These ECL 10KH parts are functional/pinout duplications of the standard ECL 10KH family parts, with 100% improvement in propagation delay and no increase in power supply current.

Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
MC10H210 MC10H211	J,N,NL,(20)	Com



MC10H210 3 2 1 20 19

AOUT1 NC VCC2 VCC1

ECL10KH

3-INPUT 3-OUTPUT BOUT1

OR GATE

AIN3 VEE NC BIN1 BIN2

9 10 11 12

MC10H211

BOUT2

NC 16

5

8

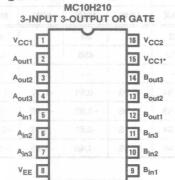
NC

AIN1

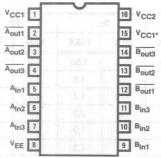
AIN2

VCC2 = PIN 16 VEE - PIN 8

Pin Configurations



MC10H211 3-INPUT 3-OUTPUT NOR GATE



* Pins 1 and 15 internally connected

AOUT2 VCC1 **BOUT3** 18 5 AOUT3 BOUT2 ECL10KH 6 NC NC 16 3-INPUT NOR GATE BOUT1 15 3-OUTPUT AIN1 BIN3 AIN3 VEE NC BIN1 BIN2 9 10 11 12

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TWX: 910-338-2376

Operating Conditions

SYMBOL	PARAMETER		COMMI MIN TY		UNIT
VEE	Supply voltage		-5.46 -5	.2 -4.94	V
TA	Operating free-air temperature		0	75	°C
	Sound trade to the second	Plastic	-55	150	
TSTG	Storage temperature range	Ceramic	-55	165	°C

Electrical Characteristics V_{EE} = -5.2 V ±5% (See Note)

SYMBOL	PARAMETER	0	0°		25°		75°	
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
I _E	Power supply current		42	v (87)	38	TI to	42	mA
linH	Input current HIGH	-1	720	y In.	450	T 110	450	μΑ
linL	Input current LOW	0.5		0.5	_	0.3	A -	μΑ
V _{OH}	HIGH output voltage	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
VOL	LOW output voltage	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
V _{IH}	HIGH input voltage	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
VIL	LOW input voltage	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

Switching Characteristics VEE = -5.2V ±5% (See Note)

	PARAMETER		0°		2	25°		75°	
SYMBOL			PARAMETER MIN	MAX	MIN	MAX	MIN	MAX	UNIT
N. BYE	3-INPUT	MC10H210	0.5	1.55	0.55	1.55	0.6	1.7	
^t pd	t _{pd} Propagation delay	MC10H211	0.7	1.6	0.7	1.6	0.7	1.7	ns
4 4.	Ar care	MC10H210 0.75 1.8	0.75	1.9	0.8	2.0			
t _r , t+	Rise time	MC10H211	0.9	2.0	0.9	2.2	0.9	2.4	ns
	Fall time	MC10H210	0.75	1.8	0.75	1.9	0.8	2.0	
ι _f , ι-	t _f , t- Fall time	MC10H211	0.9	2.0	0.9	2.2	0.9	2.4	ns

vote: Each ECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50 Ω resistor to -2.0 V.

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LOGIC CELL ARRAY Logic Cell Array 15-3

Logic Cell Array™

Introduction

The Logic Cell Array (LCA)™ is a CMOS integrated circuit with a flexible, uncommitted architecture and VLSI-level density. The LCA is manufactured on Monolithic Memories' 1.6 micron CMOS process. The device architecture as is shown in Figure 1, similar to that of a gate array, with an interior matrix of programmable logic blocks, a surrounding ring of I/O interface blocks and programmable interconnect used to define the overall device structure.

Unlike gate arrays, Logic Cell Array functionality is defined by the user simply by loading the internal writable storage cells with the configuration data. An additional benefit, reprogrammability in system, allows in-circuit-emulation to be used for design verification.

The M2064 family of Logic Cell Arrays has been developed to allow Monolithic Memories to offer a device and technology that offer both the density benefits of gate arrays and the programmability benefits of user-configurable devices. These parts have been designed for maximum flexibility in system applications and are easy to use.

Using the XACT** software development system, the designer can define and interconnect logic blocks to build larger-scale, multi-level logic functions. These are then connected to external circuitry. Interconnections throughout the Array are defined automatically by the development system, unless otherwise specified by the designer. Because the Logic Cell Array's logic functions and interconnections are established with memory cells, the array is never physically altered; instead it is simply reprogrammed.

XACT Evaluation Kit (LCA-MEK01)

Monolithic Memories offers evaluation software and documentation that will allow a designer to determine if his or her logic design fits and assess its performance as a Logic Cell Array. All that is needed is an IBM PC-XT, AT, or compatible, a three-button Mouse System or compatible mouse.

XACT Development System (LCA-MDS21)

The XACT Development System is the "power behind the machine." It will allow a designer to sit down with a concept and walk away with a completely tested, completely finished part.

The reason is that XACT functions as both a CAE and CAM system. The CAE part of the system allows the designer to simply draw out the design using a sophisticated graphics-based design editor. The CAM part then converts the drawing to code, similar to a PALASM-generated JEDEC file, that allows-programming with conventional programming hardware of an EPSOM containing the configuration data for system phototyping

The XACT Development System currently has 113 macros and, in addition, allows the user to define his or her own macro. To insure that internal timing constraints are satisfied, a Timing Analyzer is included to calculate propagation delays along any path within the Array.

As the design is being entered, the Automatic Design Checker insures that no design rules are violated, and when the design is completed, a final design rule check is performed.

LCA™, Logic Cell Array™ and XACT™ are trademarks of Xilinx Inc.

The XACT Development System

Contents:

- Editor
- Macro Library
- Design Checker
- Timing Analyzer
- Simulator
- Configuration File Generator
- Configuration File Formatter

In-Circuit-Emulator (LCA-MDS24)

The In-Circuit-Emulator is a software/hardware package that enables a designer to connect his or her target system to the work-station where a design has just been completed. The emulator package allows:

- User control and monitoring of device function
- · Interactive or file-driven setup and configuration
- Daisy-chain configuration capabilities for up to seven LCAs in a chain
- · Simultaneous in-circuit emulation of up to four devices
- · Single step capability for device clocks
- · Readback display of device internal register states
- · Dynamic reconfiguration capability.

The In-Circuit-Emulator comes with a single "pod". Up to three additional pods (LCA-MDS25) may be ordered for each emulator.

P-SILOS Simulation Package (LCA-MDS22)

After a design is completed, the next step is to simulate. Monolithic Memories offers an integrated simulation package manufactured by Simucad, called P-SILOS.

PART NUMBER	DESCRIPTION
LCA-MEK01	LCA Evaluation Kit
LCA-MDS21	LCA Development system
LCA-MDS22	LCA Simulator - P-SILOS
LCA-MDS24	LCA In-Circuit-Emulator
LCA-MDS25 LCA In-Circuit-Emulator Pod	
LCA-MTB01	LCA Demonstration Board

Table 1

The introduction of the Logic Cell Array will allow customers to reduce inventories of discrete components, reduce the time to market and development cost for new products, save money in manufacturing and spare parts inventory management, reduce test costs and improve system reliability.

nal design rule check is performed.

mx Inc.

Monolithic Memories

Configurable Logic Block TOAX and

The core of the Logic Cell Array is an 8x8 matrix of Configurable Logic Blocks. Each CLB provides four logic inputs, a clock input, a combinatorial logic section, two logic outputs, and a programmable storage element.

The inputs drive a combinatorial logic section that can perform any logic function from a simple gate to a three-out-of-four majority decoder.

The combinatorial portion accepts and generates both positiveand negative-true logic, eliminating the need for inverters or the routing of complementary signals.

The storage element can serve as a flip-flop (D-type) and can be programmed to have clock enable, synchronous set and reset, and various gated inputs. In addition, since all these options can be specified independently for each logic block, designers can mix asynchronous and synchronous logic in any combination.

where a design has just paen control

Interconnect

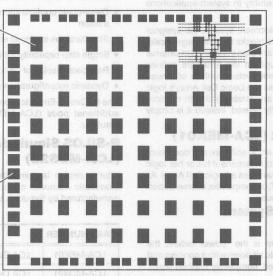
The Array's extraordinary flexibility is also the result of a twolayer metal network of lines that run horizontally and vertically between the logic and I/O blocks, and a variety of user-definable interconnection elements.

Definable interconnection points connect the inputs and outputs of logic and I/O blocks to nearby metal lines.

Crosspoint switches and interchanges are clustered at the intersection of every row and column of logic blocks. They link horizontal and vertical paths and allow signals to be switched from one path to another.

Finally, "long lines" run the length and breadth of the chip, bypassing interchanges but tying into logic blocks and other lines and distributing clocks and other critical signals with a minimum of propagation delay.

Interchanges and interconnection point assignments, as well as all routing are handled automatically by the XACT Development System Software. In addition, special graphics-based design tools are included to facilitate any necessary designer interaction.



Configurable I/O Block

External signals enter and leave the chip through general-purpose, user-definable I/O blocks positioned around the periphery of the array. Each block can be programmed independently to be an input, output or bidirectional pin with a tristate control on the output. When configured as an input, the designer can select TTL or CMOS thresholds. In addition, each I/O bloc contains an input register option whose clock line is common to all the other I/O blocks along the same edge of the die.

I/O blocks can also handle more than input and output functions. For example, the Input registers of unused I/O blocks can be used for read/write storage registers or as stages of a shift register.

Figure 1

Logic Cell Array™ M2064

Features/Benefits

- CMOS programmable Logic Cell Array (LCATM) for replacement of standard logic
- Completely reconfigurable by the user in the final system
- High performance
 - -20 MHz flip-flop toggle rate (-20 speed grade)
- -33 MHz flip-flop toggle rate (-33 speed grade)
- -50 MHz flip-flop toggle rate (-50 speed grade)
- User-configurable logic functions, interconnect and I/O for maximum flexibility
- 64 user-Configurable Logic Blocks (CLBs) providing usable gate equivalency of up to 1500 gates
- 58 individually-configurable I/O pins allowing any mix of inputs, outputs or bidirectional signals (68-pin package)
- . User-selectable TTL or HCMOS input threshold levels
- Multiple configuration modes for greatest flexibility and
 ease of use
- · Verification feature allows user to check configuration data
- User-selectable security feature prevents read-back of configuration data
- · Read-back of internal register states for system debug
- On-chip clock oscillator and clock buffer circuits provide flexible internal and external clocking functions
- Master reset of all internal register elements in addition to user-configurable Reset and/or Set control of individual CLB storage elements

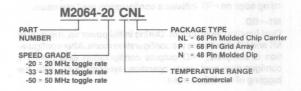
General Description

The M2064 is the first member of a family of configurable Logic Cell Arrays (LCAs) available from Monolithic Memories. These general purpose CMOS integrated circuit devices allow the user to rapidly implement complex digital logic functions directly without the requirement for masking or other vendor performed programming steps. Unique configuration circuitry allows complete reconfiguration within a user's final system to allow system changes "on-the-fly."

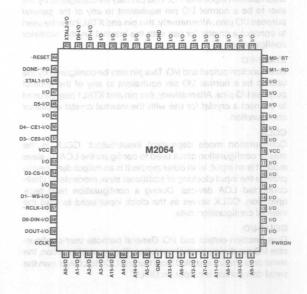
User configuration is controlled by internal storage elements. These are loaded with data bits which control definition of logic functions, configuration of I/O blocks, routing of internal signals, and other options. Configuration data can be loaded in one of several methods to minimize impact on overall system design.

CMOS technology optimized for system level performance provides LS-TTL compatible speeds with power consumption less than 10% of equivalent TTL systems. The use of innovative I/O buffers providing either TTL or CMOS input switching levels insures lowest possible power consumption in totally CMOS systems without any compromise in performance.

Ordering Information



PART NUMBER	DESCRIPTION
LCA-MDS21	XACT Development System
LCA-MDS22	P-SILOS Simulation Package
LCA-MDS24	LCA In-Circuit Emulator
LCA-MDS25	In-Circuit Emulator Pod
LCA-MEK01	XACT Evaluation Kit



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Monolithic Memories



Pin Description

1/0

User-configurable Input/Output pins.

~PWRDN

Input forces device into low power mode; operation is suspended.

MO-~RT

Dual function input. During initial power up, the state of M0 and M1 determines the configuration mode. After configuration, a rising edge on ~RT initiates a configuration read operation.

M1-~RD

Dual function input/output. During initial power up, the state of M1 and M0 determines the configuration mode. After configuration is complete, ~RD outputs configuration data during a configuration read back operation synchronously with the toggling of the CCLK input.

~RESET

Input. A low level on this input after configuration causes all register elements internal to the LCA to be forced to 0. If asserted prior to the start of configuration, causes the LCA to remain in the initialization state (configuration is not started). If asserted during configuration the LCA returns to the initialization state.

DONE-~PG

Dual function output/input. During configuration the LCA pulls DONE low and releases it when configuration is complete (output is open drain). After configuration is complete, a falling edge on ~PG initiates an LCA programming cycle (if enabled in the current configuration). This pin has an internal user-enabled pull-up resistor.

XTAL1-I/O

Dual function input and I/O. This pin may be configured by the user to be a normal I/O pin equivalent to any of the general purpose I/O pins. Alternatively, this pin and XTAL2 may be used to connect a crystal for use with the internal crystal oscillator configuration.

XTAL2-I/O

Dual function output and I/O. This pin may be configured by the user to be a normal I/O pin equivalent to any of the general purpose I/O pins. Alternatively, this pin and XTAL1 may be used to connect a crystal for use with the internal crystal oscillator configuration.

CCLK

Configuration mode dependent input/output. CCLK is the master configuration clock used to configure the LCA. In slave mode it is an input; in all other modes it is an output designed to provide the input clocking of additional slave mode daisy chain connected LCA devices. During a configuration read back operation, CCLK serves as the clock input used to read the internal configuration data.

DOUT-I/O

Dual function output and I/O. General purpose user-configurable I/O pin during normal operation. During configuration, the serial data stream supplied from the first LCA to LCAs down the serial daisy chain is output on DOUT.

~RCLK-I/O

Dual function output and I/O. General purpose user-configurable I/O pin during normal operation. During master mode configuration, a low level output on ~RCLK indicates that the external memory device is being accessed.

D0-DIN-I/O

Multi-function input and I/O. General purpose user-configurable I/O pin during normal operation. During master mode configuration, this pin is bit 0 of the 8-bit parallel input data bus (D0). During slave mode or peripheral mode configuration, this pin is the serial input data pin (DIN).

D1-~WS-I/O

Multi-function input and I/O. General purpose user-configurable I/O pin during normal operation. During master mode configuration, this pin is bit 1 of the 8-bit parallel input data bus (D1). During peripheral mode configuration, a low level on -WS indicates that a write operation is being performed by the controlling processor. See note.

D2-CS-I/O

Multi-function input and I/O. General purpose user-configurable I/O pin during normal operation. During master mode configuration, this pin is bit 2 of the 8-bit parallel input data bus (D2). During peripheral mode configuration, a high level on CS indicates that a write operation is being performed by the controlling processor. See note.

D3-~CE0-I/O

Multi-function input and I/O. General purpose user-configurable I/O pin during normal operation. During master mode configuration, this pin is bit 3 of the 8-bit parallel input data bus (D3). During peripheral mode configuration, a low level on ~CEO indicates that a write operation is being performed by the controlling processor. See note.

D4-~CE1-I/O

Multi-function input and I/O. General purpose user-configurable I/O pin during normal operation. During master mode configuration, this pin is bit 4 of the 8-bit parallel input data bus (D4). During peripheral mode configuration, a low level on ~CE1 indicates that a write operation is being performed by the controlling processor. See note.

D5-I/O to D7-I/O

Input and I/O. General purpose user-configurable I/O pins during normal operation. During master mode configuration, these pins are bits 5 through 7 of the 8-bit parallel input data bus (D5-D7).

A0-I/O to A15-I/O

Output and I/O. General purpose user-configurable I/O pins during normal operation. During master mode configuration these pins are address output pins (A0-A15) used to address the external storage element used for configuration data.

Note: to perform a peripheral mode write, the following logical combination is necessary: \sim WS \cdot CS \cdot \sim CE1.

Functional Description

The M2064 is a high-performance CMOS Logic Cell Array providing superior system performance with greatest user flexibility. Complete user-configurability provides an optimized solution to logic implementation problems.

The M2064 utilizes a unique Configurable Logic Block (CLB) structure as the basic functional building block of the device. Each CLB is a combination of a programmable logic function and a storage element. The CLB has the capability of performing any function of its inputs with the option of the output of the storage element included in the input field. User-defined logic is implemented in a matrix of sixty-four CLBs which are interconnected with user-configurable interconnect resources.

Fifty-eight independently configurable I/O Blocks; each of which can be a direct or latched input, a direct or open drain output, or a bidirectional I/O buffer; provide the interface to external circuits. Input voltage levels are user definable and may be either standard TTL or CMOS for all I/O Blocks, depending on the user's configuration choice.

User-definable path selector or multiplexers are utilized to select configuration options for the CLBs and I/O Blocks. These selectors are set in the desired state by the configuration data loaded into the device upon power up.

Logic

User logic is implemented in one or more CLBs which are general purpose 4-input, 2-output elements. Figure 1 shows a block diagram of a single CLB. Each element is composed of a 4-input combinational logic module with two outputs, a general purpose storage element, and routing selection logic. The module can generate any combinational logic function of the four inputs, or it can generate any two independent functions of any three of the four inputs. If a function of four inputs is selected, that same function will be available on both of the outputs of the combinational module. The inputs to the combinational module are three of the four inputs to the CLB (A, B and C) and either the D input to the CLB, or the Q output of the storage element.

The general purpose storage element has a data input, a clock input, a set direct input, a reset direct input and an output, Q. The storage characteristic may be defined as either a transparent latch or as an edge-triggered flip-flop. The data input is connected to one of the outputs of the combinational logic module. The set direct and reset direct inputs may be individually enabled or disabled.

The reset direct input, if enabled, may come from either the D input to the CLB, or from the G output of the combinational logic module. Set direct control, if enabled, can come from either the A input to the CLB or from the F output of the combinational logic module.

Clock for the storage element may be individually enabled or disabled and can be driven by the clock input, K, to the CLB, the C input to the CLB, or the G output of the combinational logic module. Final outputs, X and Y, from the CLB can be selected to be either of the two outputs, F and G, of the combinational logic module, or the Q output from the storage element.

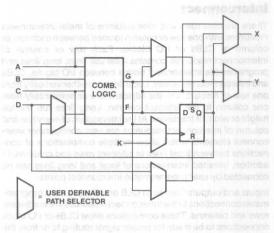


Figure 1. Block Diagram of a Single CLB

I/O Elements

The M2064 contains fifty-eight user-configurable I/O blocks for connection to external circuits. Each block is a general purpose device containing a three-state output buffer, an input buffer, and an input flip-flop as shown in Figure 2. The input buffer always reflects the status of the I/O pin or the contents of the input flip-flop. If the flip-flop is selected, data present on the I/O pin will be clocked to the input buffer by the I/O block clock signal. All I/O blocks on a particular edge of the device share a common I/O clock signal. The output buffer may be enabled, disabled, or under the control of the three-state connection.

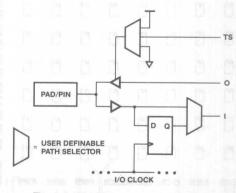


Figure 2. Block Diagram of an I/O Element

Interconnect

There are nine rows and nine columns of metal interconnect resources with one row or column located between each row or column of CLBs or I/O blocks. Each row or column of interconnect resources contains local use lines, long lines and programmable interconnect points between I/O blocks, CLBs and interconnect resources. Local lines run either vertically from one row of resources to the adjacent row or horizontally from one column to the adjacent column. Long lines run the full height or width of the device. At the intersection of every row and column of interconnect resources are user configurable interconnect elements which allow multiple combinations of connections between local lines in adjacent rows and columns. In addition, selected intersections of local and long lines can be connected by user programmable interconnect points.

Inputs and outputs from each CLB or I/O block have programmable connections to the interconnect resources in the adjacent rows and columns. These connections allow CLBs or I/O block connections to be made for proper signal routing to or from the I/O blocks or CLBs. In addition to the programmable connections to adjacent interconnect resources, there are direct connection paths which do not utilize the general interconnect resources. These paths allow selected connection between some I/O blocks and CLBs and between adjacent CLBs. For example, the outputs of a CLB in the interior of the matrix of CLBs may be connected to adjacent CLBs without using any interconnect resources.

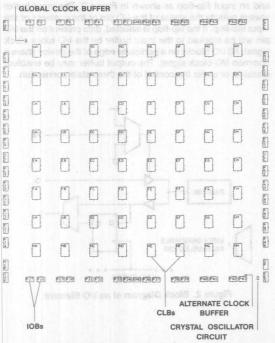


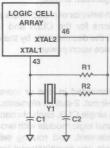
Figure 3. Overview Functional Layout of the M2064

Clock Generation and Buffering

The M2064 contains two special purpose clock buffers for generating and driving clock signals to multiple CLBs or I/O blocks

with negligible skew. The Global Clock Buffer, is dedicated to driving a matrix of long lines which have configurable connections to the K input of each CLB register. This clock buffer may be driven from an internally generated register source, or configured with a connection directly to an I/O block for driving it with an external clock signal. The output from the Global Clock Buffer may be configured to directly drive an I/O block for driving clock signals off the device.

The alternate clock buffer can be configured either as a simple buffer or as a buffer for the crystal oscillator. In the crystal oscillator mode, an externally connected crystal and optional passive components form a clock generator for use on the chip or for driving other external circuits (see Figure 4). When configured in the buffer mode, the alternate clock buffer can have either one or both of its input and output configured to directly drive, or be driven by, an I/O block. The output of the alternate clock buffer can drive long lines in any column of CLBs as well as local interconnect.



Suggested component values:

a Sittle Mariana	run mouls, of it can generate any two independent
R1	1-4 MΩ s it alugni not est to send ve
R2	no 0 - 1 KΩ id the notional error test betosis
C1, C2	0 5 - 20 pF 0 and of fugal 0 and radile bas (
Y1	1 - 10 MHz AT cut

Figure 4. Crystal Oscillator

Each CLB has a special clock input (K) which can be selected as the clock input of the storage element. Clock inputs to user selected CLBs can be configured to be driven from either the Global Clock Buffer, the oscillator/buffer or from other local interconnect. Clocks to the I/O blocks can be configured from either of the clock buffers or the local interconnect.

Programming

Configuration of the device may be performed in any one of three modes. The desired configuration mode is set by the state of the mode pins M0 and M1 at power up (see Table 1). All configuration data relating to CLB function definition, interconnect resource utilization, and I/O block programming must be loaded into the device prior to use. In the peripheral and slave modes the data is supplied in a serial stream in conjunction with the configuration clock signal, CCLK. In master mode, the device automatically loads data from an external memory device by supplying addresses and reading bytes of data. In all modes the data patterns required to create a specific configuration are the same

MODE SELECT PINS	MO	M1
Master LOW mode	0	0
Master HIGH mode	0 0	1 1
Peripheral mode	1	0
Slave mode	1	1

Note: During configuration, Pin 27 on the 68-pin package or Pin 7 on the 48-pin package must be held HIGH.

Table 1. Modes

Data patterns for a specific user-configuration are created with the Monolithic Memories XACT LCA Development System and can be output to a standard EPROM programmer or saved on disk for inclusion with other software. Users who are using the Monolithic Memories XACT debugging system can directly access the configuration data and load the device directly during a debug session. Because of the complexity of the data patterns and difficulty in generating them without a thorough knowledge of the device, users are discouraged from attempting to generate data patterns on their own. Data pattern files for M2064 devices contain 1536 bytes.

Special Features

The M2064 contains several special features which enhance its capacity for use in a wide variety of applications. Among these are the following:

Data Security

The M2064 configuration data contains special control bits which enable or disable configuration data security control. If enabled, the security control will prevent the read-back of configuration data after the initial configuration. There are two possible modes of operation under security control. One mode allows a single read-back after configuration to allow verification of the data. In the second mode, all access to the configuration data is prevented.

Reprogrammability

Configuration data changes are controlled by reprogramming control bits in the configuration data supplied to the device. If reprogramming is enabled, the user may supply new configuration data at any time by asserting the correct control sequence on the DONE-PG and M0 and M1 mode control pins. Alternatively, the user may elect to prevent reconfiguration of the device. When operating in this mode, the only method to remove the configuration is to remove all power from the device.

Inactive Power-down

In a system which is to remain in its current configuration through power loss, the M2064 may be forced into a low power inactive state by using the ~PWRDN pin. When held low, the LCA will retain all configuration data but will not operate. All clocks will be stopped and all outputs put into a high-impedance state. Power is reduced to a very low level, allowing a simple external battery arrangement to supply the required configuration data saving power (see electrical characteristics).

Configuration Data Read-back

A mechanism is provided in the M2064 to provide verification of stored configuration data. The configuration read-back is initiated by toggling the ~RT pin and clocking the CCLK pin. Each clock applied to CCLK will read out a configuration data bit on the ~RD pin. When all configuration data has been read out, the ~RD pin will return to its inactive state. The configuration data may be read at any time with no effect on the operation of the device. Once a configuration read-back has been initiated, all data must be read out of the device to insure that subsequent read-back operations will begin at the start of the configuration data.

Master Reset

After device configuration, the ~RESET pin becomes a master reset for all CLB and IOB storage elements in the device. Asserting this control signal will asynchronously reset all of the internal storage registers regardless of the operating condition of the circuit.

Development System

The Monolithic Memories Design System is an integrated package of design tools for developing configuration data for LCAs. All aspects of configuration are specified through interactive graphics software. Facilities to verify functionality and timing of the designed configuration insure that designs operate as desired.

XACT is a graphic design system used to specify LCA designs. It contains several standard and several optional software and hardware packages. The basic package runs on an IBM PC/XT or AT compatible computer with 640K memory, a color monitor and a mouse. The tools accessible from the executive, including the optional packages, are:

- · LCA Editor and Macros
- Timing Analyzer
- Simulator (P-Silos, optional)
- Configuration-File Generator
- Configuration-File Formatter
- XACTOR 2 In-circuit-emulator (optional).

XACTOR 2 consists of a software program plus a hardware attachment that allows control of up to four LCAs. The program contains commands for:

- Loading configuration data
- · Activating the Master Reset input
- Reconfiguring
- Single stepping the device clock
- Reading back configuration data and state of all 122 internal registers on any clock cycle.
- Real time system debug.

An evaluation kit is available which includes:

- Complete documentation of the Development System
- A sample LCA design
- XACT software package.

Contact your local Monolithic Memories Representative or Distributor for more information.

Absolute Maximum Ratings*

Supply voltage VCC	
Power down VCC	2 V to 7 V
Input voltage	0.5 V to V _{CC} 0.5 V
Voltage applied to three-state output	0.5 V to V _{CC} 0.5 V
Storage temperature range	65° C to +150° C
Lead temperature (soldering, 10 seconds)	

^{*}Note: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those listed under "Recommended Operating Conditions" is not implied. Exposure to "Absolute Maximum Ratings" conditions for extended periods of time may affect device reliability.

Operating Conditions

SYMBOL	Enterior of the exclusion delegated PARAMETER and point the only stop	MIN TYP MA	X UNIT
V _{CC}	Supply voltage relative to GND	4.75 5.2	5 V
VIHT	High level input voltage—TTL configuration	2.0	V
VIHC	High level input voltage—CMOS configuration	0.7	V
VILT	Low level input voltage—TTL configuration	method stall o wo dent no to.	8 V
VILC	Low level input voltage—CMOS configuration	0 0.	2 V
h _T igo ang	Input leakage current—TTL configuration	±1	μА
Ic	Input leakage current—CMOS configuration	feet pioega L±1.uea emparios la	μΑ
loz	Three-state output off current (V _{CC} = 5.5V)	±10	μΑ
tOP	Operating free-air temperature	0 7	0 °C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMET	ΓER	TEST CONDITION	MIN TYP MAX	UNIT
Vон	High level output voltage	je luovio-m s AC	V _{CC} = 4.75 V I _{OH} = -4.0 mA	3.86	V
VOL	Low level output voltag		V _{CC} = 4.75 V I _{OL} = 4.0 mA	0.32	V
	Quiescent operating	CMOS inputs	V _{CC} = 5.0 V	noldsnesi gaim 5	mA
cco	power supply current	TTL inputs	V _{CC} = 5.0 V	10	mA
ICCPD	Power down supply cui	rent	V _{CC} = 2.0 V	Consult factory	V

Note: All switching characteristics are at worst case conditions.

Power on Timing

The M2064 contains on-chip reset timing logic for power-up operation. To insure proper master mode system operation, VCC must rise from 2.0 V to minimum specification level in 10 ms or

less. For other modes, initiation of configuration must be delayed for 60 ms after VCC reaches the minimum specified level.

Switching Characteristics—CLB

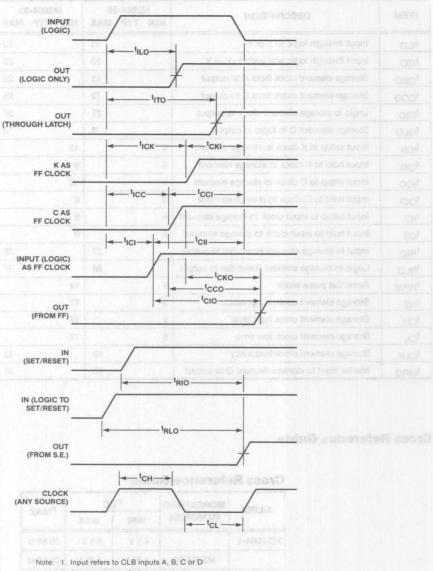
ITEM	DESCRIPTION	M2064-50 MIN TYP MAX	M2064-33 MIN TYP MAX	M2064-20 MIN TYP MAX	UNIT
^t ILO	Input through logic to X or Y	15	20	35	ns
t _{ITO}	Input through logic and latch to X or Y	20	25	45	ns
tCKO	Storage element clock from K to output	15	(УДИО ЭТВОЛ) 20	35	ns
tcco	Storage element clock from C to output	19	25	45	ns
tCIO	Logic to storage element clock to output	27	TUO 37	65	ns
^t QLO	Storage element Q to logic to output	8	13	30	ns
^t ICK	Input setup to K clock to storage element	8	12	22	ns
^t CKI	Input hold to K clock to storage element	0	CAS 0	0	ns
tICC	Input setup to C clock to storage element	9	12	18	ns
^t CCI	Input hold to C clock to storage element	0	6	10	ns
^t ICI	Input setup to input clock to storage element	4	6 200 3	10	ns
^t CII	Input hold to input clock to storage element	5	9	15	ns
t _{RIO}	Input to storage element Reset/Set to output	22	25	45	ns
t _{RLO}	Logic to storage element Reset/Set to output	28	78 ASEF CLOCK	65	ns
t _{RPW}	Reset/Set pulse width	9	12	20	ns
t _{RS}	Storage element control separation	9	17 ₁₀₀	30	ns
^t CH	Storage element clock high time	9	12 (3/14/0/34)	20	ns
^t CL	Storage element clock low time	9	12	20	ns
f _{CLK}	Storage element clock frequency	50	33	20	MHz
t _{MRQ}	Master reset to storage element Q to output	25	35	60	ns

Cross Reference Guide

Cross Reference Guide

XILINX	MONOLITHIC	V	(EDAUGE Y		
AILINA	MEMORIES	MIN	MAX	FMAX	
XC-2064-1		4.5 V	5.5 V	20 MHz	
	M2064-20	4.75 V	5.25 V	20 MHz	
XC-2064-2	191 X 04 Y Heroov element clock	4.5 V	5.5 V	33 MHz	
XC-2064-33	M2064-33	4.75 V	5.25 V	33 MHz	
XC-2064-50	M2064-50	4.75 V	5.25 V	50 MHz	

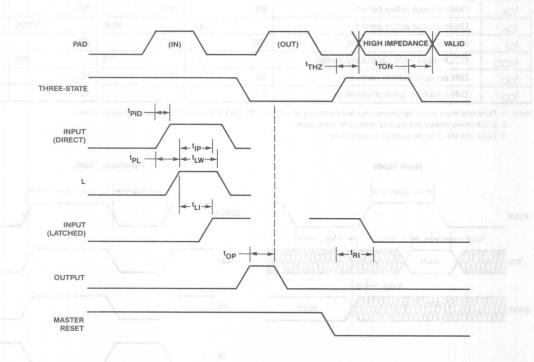
^{*}For commercial product only.



- 2. Output refers to CLB output X or Y
- 3. Clock refers to the CLB storage element clock
- 4. FF (Flip-Flop) or L (Latch) refers to the CLB storage element
- 5. Set and Reset refer to CLB storage element controls

Switching Characteristics-IOB avail - galanasa ages 9-- apiliste appared a palabate 2

ITEM	DESCRIPTION	M2064-50 MIN TYP MAX	M2064-33 MIN TYP MAX	M2064-20 MIN TYP MAX	UNIT
t _{PID}	Pad to input direct	008 8	12	antin XL00 20	ns
t _{PL}	Pad input setup to I/O clock	8 000	12	20 0 1200	ns
t _{LP}	Pad input hold to I/O clock	0	0	0 NOT 1500	ns
f	Frequency, I/O clock	50	250 pmen 0400 33	5 30 M 5 M C 20	MHz
t _{LW}	Pulse width input latch clock	9 94 95	12 km XLGO most	20	ns
t _{L1}	Input latch clock to input	15	milet AUOO mon 20	b alsb (UOO 30	ns
tOP	Output to pad output (three-state enabled)	12	15	mixam 4330 25	ns
t _{THZ}	Three-state inactive to high impedance	20	25	35	ns
t _{TON}	Three-state active to output on	20	25	40	ns
t _{RI}	Master Reset to latched input reset	25	30	50	ns



Note: 1. Output (O) refers to the output connection on the IOB

2. Input (I) refers to the input connection on the IOB

3. Three-state (T) refers to the three-state control on the IOB

Pad or Pin (P) refers to the device pin connected to the IOB

5. Latch (L) refers to the input Flip-Flop clock connection

Switching Characteristics—Programming - Slave Mode

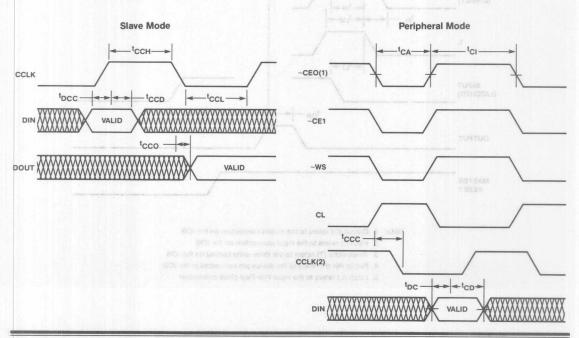
ITEM	DESCRIPTION XAA QY	M2064-50 MIN TYP MAX	M2064-33 MIN TYP MAX	M2064-20 MIN TYP MAX	UNIT
tcch	CCLK high time	300	300	500	ns
tCCL	CCLK low time	200	200 Apolo C/I of qu	300	ns
tCCL	CCLK low time	5000	5000	10000	ns
tDCC	DIN data setup to CCLK rising edge	25	25 /0000 C	50	ns
tCCD	DIN data hold from CCLK rising edge	40	40 Stoots Hafel fug	75	ns
tcco	DOUT data delay from CCLK falling edge	65	10000 65	001 Input latels el	ns
fcc	CCLK maximum frequency	(ball 2	stata-devici) fuqfi(2)	teq of fligtuO 1	MHz

Switching Characteristics—Programming - Peripheral Mode

ITEM	DESCRIPTION	M2064-50 MIN TYP MAX	M2064-33 MIN TYP MAX	M2064-20 MIN TYP MAX	UNIT
^t CA	Control input active period	200	200	300	ns
^t CA	Control input active period	5000	5000	10000	ns
tCI	Control input inactive period	150	150	250	ns
tccc	CCLK delay from control input edge	75	75	100	ns
tDC	DIN setup to control transition	35	35	50	ns
tCD	DIN hold from control transition	5	5	10	ns

Notes: 1. Peripheral mode timing determined from last control signal (~CE0, ~CE1, ~WS, CS) to transition to active or inactive state.

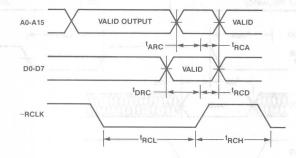
- 2. CCLK timing minima and maxima same as for slave mode.
- 3. CCLK and DOUT timing same as for slave mode.



Switching Characteristics—Programming - Master Mode and a second partial and a second partial

ITEM	DESCRIPTION	M2064-50 MIN TYP MAX	M2064-33 MIN TYP MAX	M2064-20 MIN TYP MAX	UNIT
t _{ARC}	Address invalid prior to ~RCLK edge	0	noV billev mon valle Voc	Super Page 1	ns
t _{RCA}	Address valid from ~RCLK edge	200	dthlw 200	300 and 180 an	ns
^t DRC	Data bus setup to ~RCLK edge	60 08	60 retailed of quied	100 sheld	ns
tRCD	Data bus hold from ~RCLK edge	0 10	nold from Macaer O et	Mode son 0	ns
t _{RCH}	~RCLK high	600	600 ribbin ariug ter	600	ns
t _{RCL}	~RCLK low 0001 0001	4000	4000	4000	ns

Note: Timing for DOUT and CCLK out is same as for slave mode.

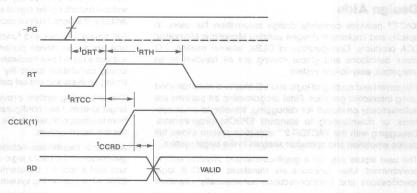


Switching Characteristics—Program Readback

ITEM	DESCRIPTION	M2064-	50 MAX	M206 MIN TY		M2064 MIN TYP		UNIT
t _{RTH}	Read trigger (RT) high time	150	g-mem-an	150		250		ns
^t RTCC	Delay from RT assertion to first CCLK	60		60	- ENO	100	1-111	ns
t _{CCRD}	Delay from CCLK edge to RD data valid		60	5.00°	60		100	ns
^t DRT	Wait period from DONE to RT assertion	75		175		300	le see	ns

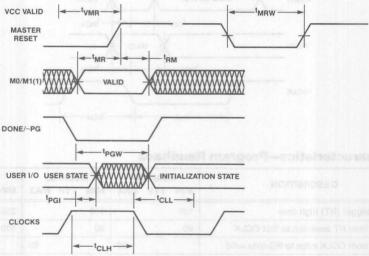
Notes: 1. Timing for CCLK is same as for slave programming mode.

2. DONE/~PG output/input must be high (device programmed) prior to assertion of ~PG.



Switching Characteristics—General

ITEM	DESCRIPTION	M2064-50 MIN TYP MAX	M2064-33 MIN TYP MAX	M2064-20 MIN TYP MAX	UNIT
tVMR	Master Reset delay from valid V _{CC}	150	150	250	ns
^t MRW	Master Reset pulse width	150	150 × 10 / 10 / 10 / 10 / 10 / 10 / 10 / 1	250	ns
t _{MR}	Mode control setup to Master Reset	60	60 24.03 - 44.0	100	ns
^t RM	Mode control hold from Master Reset	7 00	7gbs XLIOR mont	10	ns
^t PGW	Program control pulse width	6000	6000	6000	ns
^t PGI	Program control to I/O initialized	7000	7000	7000	ns
^t CLH	Clock buffer input high time	9	12	20	ns
^t CLL	Clock buffer input low time	9	12	20	ns
^f CL	Clock buffer input frequency	50	33	20	MHz



Test Conditions:

Outputs loaded with rated DC current and 50-pF capacitance to GND.

Design Aids

XACT™ provides complete design automation for users to specify and implement designs utilizing Monolithic Memories' LCA products. Configuration of CLBs, internal routing, I/O block definitions and global routing are all handled in an integrated, easy-to-use system.

Placement and routing of logic and I/O blocks is accomplished using interactive graphics. Final programming bit patterns are automatically produced for debugging, transfer to other systems, or downloading to standard EPROM programmers. Debugging with the XACTOR 2™ emulation system allows full device emulation and operation analysis in the target system.

The user inputs data via a graphics-oriented physical editing environment. User functions are translated into CLB logic specifications and interconnections automatically. Standard

logic libraries and other macro capabilities can be utilized for rapid design entry.

Physical placement and hard connections are performed with the graphics placement and connection capabilities. Final device layout and routing are visible and can be modified without disturbing the logical arrangement. Logical connectivity and physical layout rules checking are performed automatically.

Full timing analysis and functional simulation of user configurations allows device performance and functional checking without external test hardware. In addition, point-to-point path timing calculation capability is provided to simplify general timing analysis and critical path determination.

The debugging system provides full emulation in the user's target system. User configurations may be transferred directly from the design phase into the target system and tested through the emulation system.

Additional capabilities include a tool for automatic hard copy generation of the user's logic design and physical implementation and a tool for transferring programming bit patterns to EPROM programming systems.

Recommended Sockets

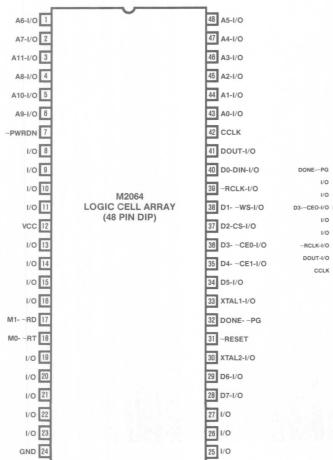
The following 68-pin PLCC sockets have been evaluated by Monolithic Memories and have been found to exhibit acceptable connectivity, device retention and device extraction characteristics:

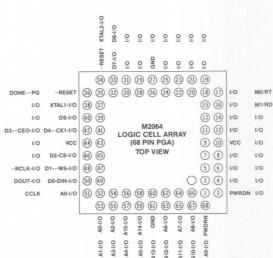
VENDOR	DESCRIPTION	PART NUMBER
AMP	PCB solder tail, tin plate	821574-1
AMP	Surface mount, tin plate	821542-1
Burndy	PCB solder tail, tin plate	QILE68P-410T
Midland- Ross	PCB solder tail, tin plate	709-2000-068-4-1-1

The following 68-pin PLCC sockets are also available:

VENDOR	DESCRIPTION	PART NUMBER 213-068-001	
Methode	PCB solder tail, tin plate		
Methode	Surface mount, tin plate	213-068-002	

- Notes: 1. The standard device extraction tools supplied with the XACT development system will work with all of the above sockets.
 - 2. All of the above PCB solder tail sockets have the same hold pattern and pinout.





a learnaid behaviorumanek

The following G-pin PLOC sockers have been evaluated by Monolishic Membries and have been found to exhibit acceptable connectability, device retention and device extraction characteristics.

ou fail		
	The state of the second second second	Name of the last o

Vestoro Surface mount, tin plate 213-088-001

Vestoro Surface mount, tin plate 213-088-001

Vestoro Surface mount, tin plate 213-088-002

One senders device extraction tools supplied with the XACT

development system title vork with all of the poor a sone of a second system.

2. All of the above PC is solder for sockurs have the cone independence and phospic.



		Output Enable and Disable Time
1	Introduction	
2	Military Products Division	The propagation delay time between the specified reference counts on this pool and adaptive voltage waveforms with the cree-state output changing from a high-impedance roll) state to the delined nion (or low) lave.
3	PROM	
4	PLE™ Devices	
5	PAL® Devices	
6	HAL®/ZHAL™ Devices	
7	System Building Blocks/HMSI™	
8	FIFO	
9	Memory Support	
10	Arithmetic Elements and Logic	IGA is the output analose sucess time of memory devices, tipp in the output diseble (easible recovery) time of mam- devices.
11	Multipliers	Propagation Time
12	8-Bit Interface	Propagation delay time, top: The time between the specified reference points on the ling
THE REAL PROPERTY.	a based disa flancatod beritasia seninggo, basasa at	
13	Double-Density PLUS™ Interface	Propagation delay one, low-to-high-lovel output, tot.M.
14	ECL10KH	The time between the appealined reference points on the impland outful voltage, waveforms with the output changing fro the association to be defined high level.
15	Logic Cell Array	Prophysition delay lime, his n-by-low-level output, (pyl The time between the specified reference, conts on the ing
16	General Information	and output vollage weselfame with the output of anging to the dailined high level to the defined low level.
	and the control of th	tan is the address (to outpla) success time or memory device.
	Advance Information	Pulse water ty
18	Package Drawings	The time invital between specified reforence points on it leading and railing agree of the pulse waveform.
19		

Clock Frequency

Maximum clock frequency, fmax

The highest rate at which the clock input of a bistable circuit can be driven through its required sequence while maintaining stable transitions of logic level at the output with input conditions established that should cause changes of output logic level in accordance with the specification.

Current

High-level input current, IIH

The current into* an input when a high-level voltage is applied to that input.

High-level output current, IOH

The current into* an output with input conditions applied that according to the product specification will establish a high level at the output.

High-level output current, ICEX

The high-level leakage current of an open collector output.

Low-level input current, IIL

The current into* an input when a low-level voltage is applied to that input.

Low-level output current, IOL

The current into* an output with input conditions applied that according to the product specification will establish a low level at the output.

Off-state (high-impedance-state) output current (of a three-state output), \mathfrak{t}_{OZ}

The current into* an output having three-state capability with input conditions applied that according to the product specification will establish the high-impedance state at the output.

Short-circuit output current, los

The current into* an output when that output is short-circuited to ground (or other specified potential) with input conditions applied to establish the output logic level farthest from ground potential (or other specified potential).

Supply current, I_{CC}

The current into* the V_{CC} supply terminal of an integrated circuit

*Current out of a terminal is given as a negative value.

Hold Time

Hold time th

The interval during which a signal is retained at a specified input terminal after an active transition occurs at another specified input terminal.

- NOTES: 1. The hold time is the actual time between two events and may be insufficient to accomplish the intended result. A minimum value is specified that is the shortest interval for which correct operation of the logic element is guaranteed.
 - The hold time may have a negative value in which case the minimum limit defines the longest interval (between the release of data and the active transition) for which correct operation of the logic element is guaranteed.

Output Enable and Disable Time

Output enable time (of a three-state output) to high level, tpZH (or low level, tpZL)

The propagation delay time between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to the defined high (or low) level.

Output enable time (of a three-state output) to high or low level, tpzx

The propagation delay time between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to either of the defined active levels (high or low).

Output disable time (of a three-state output) from high level, t_{PHZ} (or low level, t_{PLZ})

The propagation delay time between the specified reference points on the input and output voltage waveforms with the three-state output changing from the defined high (or low) level to a high-impedance (off) state.

Output disable time (of a three-state output) from high or low level, tpxz

The propagation delay time between the specified reference points on the input and output voltage waveforms with the three-state output changing from either of the defined active levels (high or low) to a high-impedance (off) state.

t_{EA} is the output enable access time of memory devices.
t_{ER} is the output disable (enable recovery) time of memory devices.

Propagation Time

Propagation delay time, tpD

The time between the specified reference points on the input and output voltage waveforms with the output changing from one defined level (high or low) to the other defined level.

Propagation delay time, low-to-high-level output, tpl H

The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined low level to the defined high level.

Propagation delay time, high-to-low-level output, tpHI

The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined high level to the defined low level.

tAA is the address (to output) access time of memory devices.

Pulse Width

Pulse width, tw

The time interval between specified reference points on the leading and trailing edges of the pulse waveform.

Setup Time

Setup time, tell

The time interval between the application of a signal that is maintained at one specified input terminal and a consecutive active transition at another specified input terminal

- NOTES: 1. The setup time is the actual time between two events and may be insufficient to accomplish the setup. A minimum value is specified that is the shortest interval for which correct operation of the device is guaranteed.
 - The setup time may have a negative value in which case the minimum limit defines the longest interval (between the active transition and the application of the other signal) for which correct operation of the device is guaranteed.

Voltage

High-level input voltage, VIH

An input voltage within the more positive (less negative) of the two ranges of values assumable by a binary variable.

NOTE:

A minimum is specified that is the least positive value of high-level voltage for which operation of the logic element within specification limits is guaranteed.

High-level output voltage, VOH

The voltage at an output terminal with input conditions applied that will establish a high level at the output. The actual input conditions needed are determined by the individual product specification.

Input clamp voltage, VIC

An input voltage in a region of relatively low differential resistance that serves to limit the input voltage swing.

Low-level input voltage, VIL

An input voltage level within the less positive (more negative) of the two ranges of values assumable by a binary variable.

NOTE

A maximum is specified that is the most positive value of low-level input voltage for which operation of the logic element within specification limits is guaranteed.

Low-level output voltage, VOL

The voltage at an output terminal with input conditions applied that will establish a low level at the output. The actual input conditions needed are determined by the individual product specification.

Negative-going threshold voltage V_{T-}

The voltage level at an input that causes a transition as the input voltage falls from a level above the positive-going threshold voltage, V_{T+} .

Positive-going threshold voltage, V_{T+}

The voltage level at an input that causes a transition as the input voltage rises from a level below the negative-going threshold voltage, V_{T-} .

Truth Table Explanations

H = high level (steady-state)

L = low level (steady-state)

= transition from low-to-high level

= transition from high-to-low level

X = don't care (any input, including transitions)

Z = off (high-impedance) state of a three-state output

a...h = the level of steady-state inputs at inputs A through H respectively

Q₀ = level of Q before the indicated steady-state input conditions were established

 $\overline{\mathbb{Q}}_0$ = complement of \mathbb{Q}_0 or level of $\overline{\mathbb{Q}}$ before the indicated steady-state input conditions were established

 Q_n = level of Q before the most recent active transition indicated by \downarrow or !

If, in the input columns, a row contains only the symbols H, L, and/or X, this means the indicated output is valid whenever the input configuration is achieved and regardless of the sequence in which it is achieved. The output persists as long as the input configuration is maintained.

If, in the input columns, a row contains H, L, and/or X together with 1 and/or I, this means the output is valid whenever the input configuration is achieved and the indicated transition has occured (the transition(s) must occur following the achievement of the steady-state levels). If the output is shown as a level (H, L, Q_0 , or \overline{Q}_0), it persists as long as the steady-state input levels and the levels that terminate indicated transitions are maintained. Unless otherwise indicated, input transitions in the opposite direction to those shown have no effect at the output.



Setup Time

Setup time, L

The time interval between the application of a signal that is maintained at one specified input terminal and a consecutive active transition at another specified input terminal.

- IOTES: 1. The satup time is the actual time between two events and may be insufficient to accomplish the satup. A minimum value is specified that is an enorthes interval for which correct operation of the device is guaranteed.
- 2. The samp time may have a negative value in which case the minimum first defines the longest interval perhaps and the application of the transition and the application of the dearer is guaranteed device is guaranteed.

ioliage

Nigh-tevel input voltage, Vist

An input vollage within the more positive (less negative) of the two ranges of veltues assumable by a binary vertable.

IOTE: A minimum is specified that is the least positive value of high-level voltage for which operation of the logic diement within specification limits is guaranteed.

High-level output vollage, VOH

The voltage at an output terminal with input conditions applied that will establish a high level at one output. The actual input conditions needed are determined by the individual product specification.

Dir. ospinia namina della della

An input voltage in a region of relatively low differential resistance that serves to limit the input voltage swing.

Loss level import voltage. V

An input voltage level within the less positive (more negative) of the two renders of volume assumable by a bivery variable.

MOTE: A maximum is specified that is the most positive value of low-level input voltage for which operation of the logic slement within specification limits is guaranteed.

low-land output voltage, Voltage

The vallage at an output terminal with Input conditions applied that will estudien a low level at the ortput. The actual input conditions needed are determined by the individual product specification.

-V contloy blodgerett palco-syllapsiv

The voltage level at an input trait causes a francition as the Input voltage fails from a level above the positive-going threshold voltage. Ver.

Positive-going threshold voltage, Vyv.

The voltage level start input that causes a transition as the input voltage rices from a level below the negative-going inneahold voltage, $V_{T,\omega}$

Truth Table Exclorations

- Abuta oneate) feval dolo a H
- = low-level (steady-state)
- level doisent-well med-postlened. 5
- X r don't care (any input, including transitions)
- way are required a to state to conscious solutions to the
- a.h = the level of steady-state inputs at inputs A Inrough B means hapter
- (i) = level of Q before the indicated steray-state input conditions were established
- complement of Q₀ or level of δ before the indicate.
 Steady state top it conditions were sats blished.
- $\Omega_0 = {\rm level}$ of Q before the most recent active transition indicated by Lori

f. in the liquit columns, a row contains only the synthols H. L. and for X. This means the indicated output is valid whenever use the configuration is achieved and regardless of the sequence in which it is achieved. The output persists as long as the input configuration is maintenad.

It in the insut columns, a row contains H, E, and/or X togethe with a row orly the output is valid whenever the upput configuration is achieved and the indicated transition has occurred (thetransition(s) must occur following the achievement of the steady-sate levels). If the output is shown as a level (H-L, O_D, or C_{OD}), it persists as long as the steady-sate input levels and the levels that terminate indicated transitions are nainballed. Output is such that the steady sate in the and the levels that terminate indicated, input mentions in the opposite direction to those shown have no effect at the output





Introduction **Military Products Division PROM** PLE™ Devices **PAL®** Devices HAL®/ZHAL™ Devices 6 System Building Blocks/HMSI™ 8 **FIFO Memory Support Arithmetic Elements and Logic** Multipliers 8-Bit Interface Double-Density PLUS™ Interface 15 ECL10KH **Logic Cell Array General Information Advance Information Package Drawings** Representatives/Distributors 19

ADVANCE INFORMATION

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////////////////////////////////ADVANCE INFORMATION

Features/Benefits

- 10 ns maximum propagation delay
- . 8 ns maximum delay from clock input to data output
- fMAY = 55.5 MHz
- Advanced oxide-isolated technology
- Programmable replacement for TTL logic
- · Reduces chip count by greater than 4:1
- · Instant prototyping and easier board layout
- Programmable on standard programmers
- Programmable three-state outputs
- · Security fuse prevents duplication
- 20-pin DIP and PLCC packages

Description

The PAL20D Series provides the highest speed available for TTL PAL devices. The 10 ns maximum propagation delay is a 33% speed improvement over the 20B Series from Monolithic Memories, at no increase in power consumption. The 20D Series is functionally compatible with the earlier 20, 20A and 20B Series.

The PAL20D Series utilizes Monolithic Memories' advanced oxide-isolated process and proven TiW fuse link technology.

Areas of Application

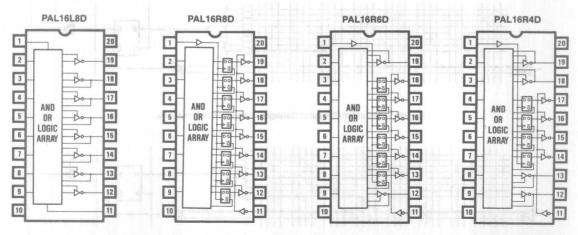
- Control logic for mainframe and super-minicomputers
- Computer-aided graphics
- High-performance communication equipment
- · High-speed test instruments

Features

The PAL20D Series includes the four standard 20-pin PAL device architectures. All four devices have sixteen array inputs and eight outputs, with varying numbers of registers: zero (16L8), four (16R4), six (16R6), and eight (16R8). The combinatorial outputs on the registered devices, and six of the outputs on the 16L8, are I/O pins that can be individually programmed as inputs or outputs. Each output register, a D-type flip-flop, also feeds back into the array, for implementation of synchronous state machine designs. Registered outputs are enabled by an external input, while the combinatorial outputs use a product term to control the enable function.

These features allow a great deal of flexibility for the design engineer when using the devices. The four different devices offer an optimized number of registers, while the number of inputs and combinatorial outputs can be balanced for the particular application. All of these features are automatically handled by the CAD software used to describe the design. Monolithic Memories' PALASM®2 software and third-party CAD tools all offer full support for these products.

Pin Configurations



This document contains information on a product under development at Monolithic Memories Inc. The information is intended to help you to evaluate this product. Monolithic Memories reserves the right to change or discontinue work on this proposed product without notice.

PAL® and PALASM® are registered trademarks of Monolithic Memories.

TWX: 910-338-2376

2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2374



Ordering Information

PAL16 R 8DCN STD PROGRAMMABLE -PROCESSING ARRAY LOGIC STD = Standard XXXX = Hi-Rel FAMILY NUMBER OF PACKAGE ARRAY INPUTS N = Plastic DIP = Ceramic DIP **OUTPUT TYPE** Molded chip carrier R = Registered L = Active Low TEMPERATURE RANGE C = 0° C to +75° C M = -55° C to +125° C NUMBER OF OUTPUTS SPEED-D = 10 ns

fMAX Parameters

The parameter f_{MAX} is the maximum speed at which the PAL device is guaranteed to operate. Because flexibility inherent to PAL devices allows a choice of clocked flip-flop designs, for the convenience of the user, f_{MAX} is specified to address two major classes of synchronous designs.

The simplest type of synchronous design can be described as a data path application. In this case, data is presented to the data terminal of the flip-flop and clocked through; no feedback is employed (Figure 1). Under these conditions, the frequency of

Programming

The PAL20D Series is programmable on the same standard programmers as the rest of the 20-pin PAL device products. No upgrades are necessary. The configuration required is the same as that for the standard 20, 20A, and 20B Series.

Logic Development Software

The following logic development software packages can be used for configuring the PAL20D Series:

PALASM®, from Monolithic Memories

ABEL™, from Data I/O Corporation

CUPL™, from Assisted Technology, Inc.

operation is limited by the greater of the data setup time (t_{SU}) or the minimum clock period (t_W high + t_W low). This parameter is designated t_{MAX} (no feedback).

For synchronous sequential designs, i.e., state machines, where logical feedback is required, inputs to flip-flop data terminals originate from the device input pins or flip-flop outputs via the internal feedback paths (Figure 2). Under these conditions, f_{MAX} is defined as the reciprocal of $(t_{SU} + t_{CLK})$ and is designated f_{MAX} (feedback). For the PAL20D Series, this value calculates as $1/(10+8) = 55.5 \; \text{MHz}.$

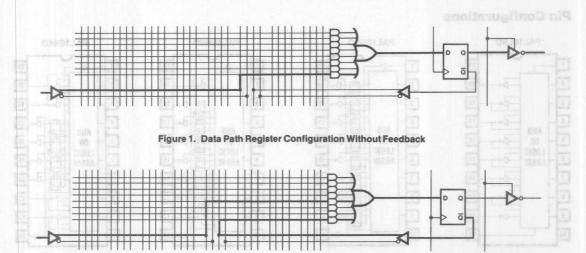


Figure 2. State Machine Configuration With Feedback

ABEL™ is a trademark of Data I/O Corporation.
CUPL™ is a trademark of Assisted Technology, Inc.

Features/Benefits

- · CMOS technology provides zero standby power
- · 25 ns maximum propagation delay (20L8, 20R4, 20R6 and 20R8)
- · Low power mask-programmed alternative for most 24-pin PAL® devices
- Space-saving 24-pin SKINNYDIP® or 28-pin PLCC and LCC
- Available in Commercial, Industrial and Military operating ranges

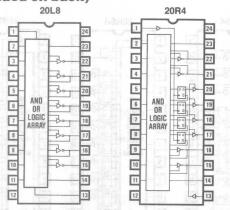
Description

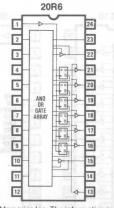
The ZHAL24A Series is a mask-programmed, zero-power option to most of the 24-pin PAL devices. The ZHAL24A Series offers not only higher density than the ZHAL20 Series, but also improved speed, matching the bipolar speeds of the Small 24 and Medium 24A, 24XA and 24RS PAL device series.

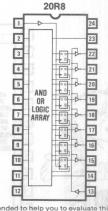
Design Procedures

ZHAL device prototyping can be done using standard PAL devices before converting to the ZHAL device for production. ZHAL devices are fabricated by Monolithic Memories with a custom mask defined by a user-supplied HAL® device Design Specification. The ZHAL24A Series utilizes a unique architecture that can implement 90% of the 24-pin PAL device patterns. To determine whether a given pattern will fit, run the ZHAL24 option in the PALASM®2 software package. Patterns that could not fit in the ZHAL20 Series will fit in the 20-pin option of the ZHAL24A Series.

ZHAL24A Device Options (continued on back)







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Areas of Application

- Portable computers
- Battery-operated instrumentation
- Low-power industrial or military equipment
- Standard CMOS/TTL logic replacement
- CMOS gate array alternative

Preliminary Data

(Commercial operating conditions, 20L8, 20R4, 20R6 and 20R8) (other families may differ)

tpn = 25 ns

tCLK = 15 ns

 $t_{SU} = 25 \text{ ns}$

ZERO-POWER HARD ARRAY LOGIC

OUTPUT TYPE

INPUTS

SPEED

NUMBER OF ARRAY-

Active Low

Registered

Registered

NUMBER OF OUTPUTS

Blank = Standard = High Speed

Complementary

XOR Registered

Shared Terms

Shared Terms

fMAX = 28.5 MHz

VOH = 3.76 V at IOH = -6 mA (HCT compatible)

VOL = 0.4 V at IOL = 8 mA

ICC (standby) = $100 \mu A$

ICC (operating) = 5 mA at 1 MHz (+ 3 mA per additional 1 MHz)

Ordering Information

ZHAL20L8 A C NS STD P01234

PATTERN NUMBER PROCESSING STD = Standard XXXX = Hi-Rel

PACKAGE

NS = Plastic SKINNYDIP

SKINNYDIP

Plastic Leaded Chip Carrier

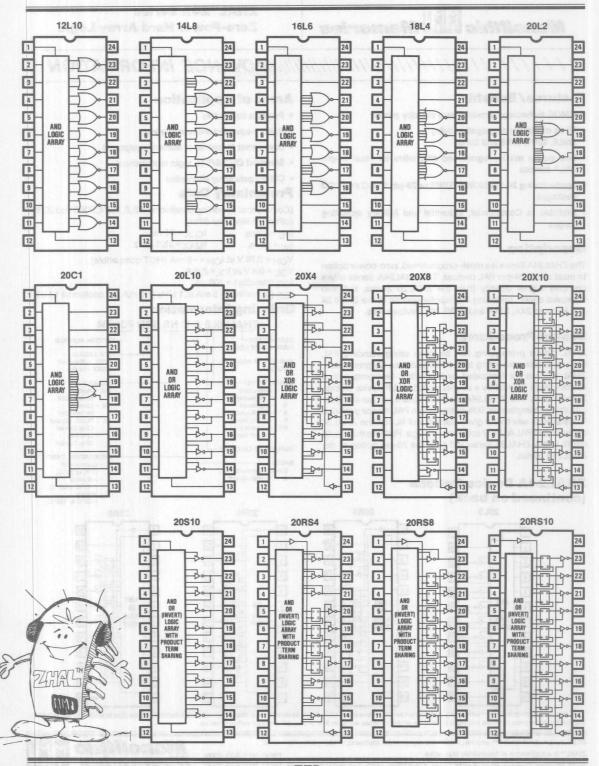
Chip Carrier

TEMPERATURE RANGE

(0°C to 75°C)

Industrial (-40°C to 85°C)

Military (-55°C to 125°C)



Features/Benefits

- 20 logic inputs; 12 external, 8 feedback
- · 8 outputs
- Programmable output polarity
- · ECL technology for ultra-high speed
- · 32 product terms with term sharing
- 10KH ECL compatible
- 50 Ω termination drive
- Input pull-down resistors
- Voltage compensated
- 24-pin SKINNYDIP® package
- Programmable using standard TTL programmers

Description

The PAL10H20P8 is a 10KH compatible ECL PAL® device having twelve dedicated inputs and eight outputs with feedback. A programmable AND array and a fixed OR array make possible a wide variety of logic functions.

Device functionality can be specified using standard sum-ofproducts expressions. Logic development software is then used to transform the Boolean equations into a fuse map for use in programming the device.

Features

Each output has a polarity fuse. Programmable polarity allows the user to optimize his design equations without using DeMorgan's theorem to give the correct output polarity. This can simplify the design and save product terms.

The programmable AND array contains a total of thirty-two product terms. Product terms are arranged in groups of eight. The terms in each group can be shared mutually exclusively between two output cells.

Device Programmer Support

The PAL10H20P8 can be programmed using the following systems:

Data I/O LogicPak™ V04, P/T Adapter 303A-ECL Family Pinout Code 22-42 Kontron EPP-80, Family Pinout Code 22-42

Logic Development Software Support

The following logic development software packages can be used for configuring the PAL10H20P8:

PALASM® 2, Ver. 2.19, from Monolithic Memories, Inc. ABEL™, Ver. 2.0, from Data I/O Corp.

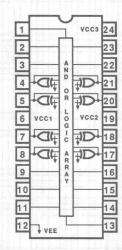
Preliminary Data

6.0 ns propagation delay 210 mA maximum IEE current

Areas of Application

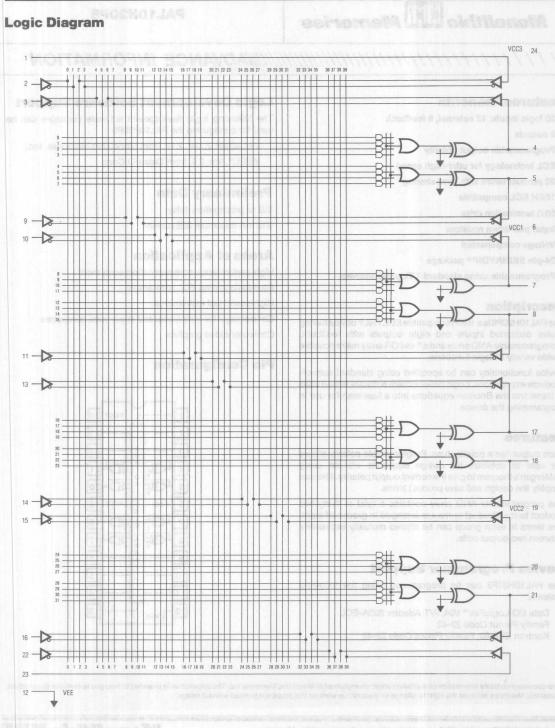
High-performance communication equipment
Glue logic joining ECL gate arrays
High-speed test instruments
Control logic for mainframe and super-mini computers
Computer-aided graphics

Pin Configuration



17

This document contains information on a product under development at Monolithic Memories Inc. The information is intended to help you to evaluate this product. Monolithic Memories reserves the right to change or discontinue work on this proposed product without notice.



//////////ADVANCE INFORMATION

circuits to be used for direct replacement of discrete CMOS as

Features/Benefits

- CMOS technology provides zero standby power
- Lowest power 24-pin PAL® device family; consumes only 3 mA/MHz
- 35 ns maximum propagation delay
- Programmable replacement for CMOS/TTL logic
- · Reduces chip count by greater than six to one
- Instant prototyping and easier board layout
- . HC/HCT compatible for use in CMOS or TTL systems
- Offered over both the Commercial and Industrial temperature ranges
- Low-cost, one-time programmable SKINNYDIP® and PLCC packages save board space

Description

The CMOS ZPAL24 Series offers the first family of PAL devices with true CMOS power consumption. Under standby conditions (inputs and clock not changing), the devices consume a maximum current of $100~\mu$ A, less than 1% that of the quarter-power PAL devices. This low power consumption allows the devices to be powered by a battery almost indefinitely.

While operating, the devices consume additional power only when the inputs or clock change. Power consumption is directly proportional to the frequency of changes to the inputs. I_{CC} is therefore specified as 3 mA per 1 MHz of operating frequency, starting from 5 mA at 1 MHz. Thus, the maximum current at 8 MHz would be 5 mA + 7x3 mA, or 26 mA.

The devices have HC and HCT compatible inputs and outputs for use in CMOS and TTL systems. This feature allows the ZPAL

Standard CMOS/TTL logic replacement

Features

ASS BOSED

well as TTL logic.

Areas of Application

· Battery-operated instrumentation

Low-power industrial equipment

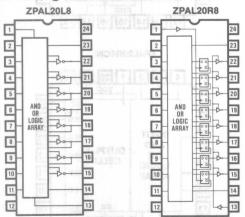
Portable computers

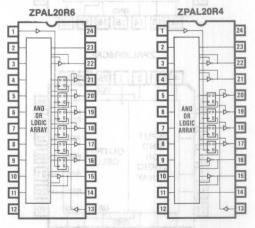
The CMOS ZPAL24 Series includes the four standard 24-pin PAL device architectures. All four devices have twenty array inputs and eight outputs, with varying numbers of registers: zero (20L8), four (20R4), six (20R6), and eight (20R8). The combinatorial outputs on the registered devices, and six of the outputs on the 20L8, are I/O pins that can be individually programmed as inputs or outputs. Each output register, a D-type flip-flop, also feeds back into the array, for implementation of synchronous state machine designs. Registered outputs are enabled by an external input, while the combinatorial outputs use a product term to control the enable function.

The basic PAL device architecture is a programmable AND array feeding a fixed OR array. The programmable AND array consists of a set of cells similar to those used in EPROMs. Erasable by UV light, the cells can be programmed and erased in the factory to ensure 100% programming and functional yields.

Windowed packages will be made available in the future, allowing erasure in the field. Windowed packages allow easy prototype testing and reconfiguration.

Pin Configurations



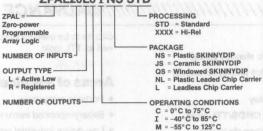


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Ordering Information

ZPAL20L8 I NS STD

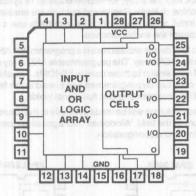


Programming

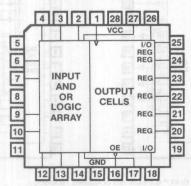
The ZPAL24 Series is programmable using the same standard programmers used for other PAL devices. The CMOS programming algorithm is different from that for the bipolar PAL devices, and requires a different family code.

PLCC Logic Symbols

ZPAL20L8CNL



ZPAL20R6CNL



Logic Development Software

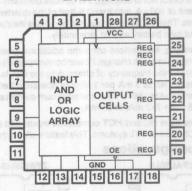
The following logic development software packages can be used for configuring the ZPAL24 Series:

PALASM®2, from Monolithic Memories

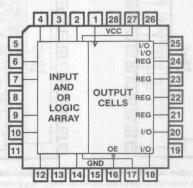
ABEL™, from Data I/O Corporation

CUPL™, from Assisted Technology

ZPAL20R8CNL



ZPAL20R4CNL



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Features/Benefits

- . User-programmable synchronous state machine
- 25 MHz maximum frequency for compatibility with 12.5 MHz processors
- 14 inputs (8 external), 8 outputs, 128 states
- PAL® array optimizes product terms and states
- · Internal feedback adds versatility and control
- · Optimized for four-way branching
- User-selectable asynchronous initialize or asynchronous enable function
- · Power-up reset for start-up in known state
- Diagnostics-On-Chip™ shadow register eases chip and board-level testing
- PROSE device software makes it easy to "write your sequencer in PROSE"
- Programmed on standard logic programmers
- · Security fuse prevents pattern duplication
- Space-saving 24-pin 300-mil SKINNYDIP® and 28-pin PLCC and LCC packages

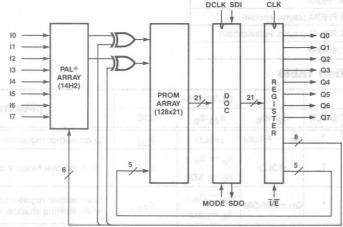
Description

The PMS14R21 programmable sequencer is the first member of the PROSE (PROgrammable SEquencer) family. The PMS14R21 is a high-speed, 14-input, 8-output state machine. It consists of a 128x21 PROM array preceded by a 14H2 PAL array. The PAL array is efficient for a large number of input conditions, while the PROM array is optimal for a large number of product terms and states. The combination allows a very efficient state machine with a large number of inputs and state bits. The PAL array, with eight product terms per output, operates on the eight conditional and six state inputs to select two control bits to the PROM. Two Exclusive-OR gates between the two arrays help to minimize product terms and redundant states. Five lines feed back from the PROM to form the primary address for the next state. The PROM stores up to 128 states of eight outputs and thirteen feedback control signals.

Applications

- High speed sequential logic
- Peripheral controller
- Cache control sequencer
- Signal processing sequencer
- Industrial control





Definition of Signals

		CLK	Clock for output register
10-17	Primary inputs to the PAL array	DCLK	Clock for diagnostic register
Q0-Q7	Outputs from the register	MODE	Selects diagnostic functions
T/E	Programmable asynchronous initialize (I)	SDI	Serial data input to shadow register
	or asynchronous enable (E)	SDO	Serial data output from shadow register

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TWX: 910-338-2376

2175 Mission College Blvd. Santa Clara. CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2374





PROSE Part Numbering System

PMS14R21 A C NS STD PROCESSING PREFIX -PMS = Programmab STD = Standard Memory-based XXXX = Hi-Rel Sequencer PACKAGE NS = Plastic SKINNYDIP NUMBER OF ARRAY INPUTS JS = Ceramic SKINNYDIP NL = Plastic Leaded **OUTPUT TYPE-**Chip Carrier R = Registered Leadless Chip Carrier NUMBER OF REGISTERS OPERATING CONDITIONS C = 0°C to 75°C PERFORMANCE--55°C to 125°C Blank = standard enhanced

Diagnostics-On-Chip Feature

The PMS14R21 is the newest member of the Diagnostics-On-Chip family. These devices incorporate a serial shadow register on-chip which facilitates board-level testing. The shadow register has a Serial Data Input (SDI), Serial Data Output (SDO) and its own clock (DCLK). The MODE control configures the shadow register either in parallel with the output register or in serial shift mode (see function table). Other devices with this feature are listed below.

Diagnostics Family Members

	and beginning the property of
PART NUMBER	DESCRIPTION
53/63DA441	1Kx4 PROM (async. enables)
53/63DA442	1Kx4 PROM (async./sync. enables)
53/63DA841	2Kx4 PROM
53/63D1641	4Kx4 PROM (async. enable)
53/63DA1643	4Kx4 PROM (async. initialization)
54/74S818	8-bit register

Software Support

PROSE device software from Monolithic Memories provides full support for the PMS14R21. Based on PALASM® 2 syntax, the software automatically converts a state machine description directly into the PAL and PROM array fuse maps, for downloading to a programmer. The syntax supports both Mealy and Moore state machine models, and makes optimal use of the features of the PROSE device. Simulation support is also provided, both for design checking and for generation of test vectors for device testing. Additional support is available from third-party software vendors, including the ABEL™ package from Data I/O.

Programming

Both the PAL and PROM arrays are programmed on standard logic programmers using the JEDEC programming format. The TiW fuses program from the low to the high state. Programming also sets the architectural fuse which selects between asynchronous initialize or asynchronous output enable; the unprogrammed state is initialize. If asynchronous initialize is selected, asserting the pin low will set all outputs and feedback bits high.

Power-up Reset

Power-up reset is provided for system start-up in a known state. It has the same effect as initialization; all output register bits go high.

Diagnostic Function Table

	INPU	UTS		7 0 44	OUTPUTS		OPERATION
MODE	SDI	CLK	DCLK	Q ₂₀ -Q ₀	S ₂₀ -S ₀	SDO	OPERATION
L	X	1	*	Qn ← PROM	HOLD	S ₂₀	Load output register from PROM array
L	х	*	1	HOLD	$S_n \leftarrow S_{n-1}$ $S_0 \leftarrow SDI$	S ₂₀	Shift shadow register data
L	X	t	t	Qn ← PROM	$S_n \leftarrow S_{n-1}$ $S_0 \leftarrow SDI$	S ₂₀	Load output register from PROM array while shifting shadow register data
Н	X	1	*	$Q_n \leftarrow S_n$	HOLD	SDI	Load output register from shadow register
н	L	* Tell		HOLD	$s_n \leftarrow Q_n$	SDI	Load shadow register from output bus and feedback
Н	Н	*	1	HOLD	HOLD	SDI	†No operation

^{*} Clock must be steady or falling.

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[†] Reserved operation for 54/74S818 8-Bit Diagnostic Register.

Features/Benefits

- 10 input/output macrocells
- Programmable registered or combinatorial outputs
- Dual independent feedback paths allow I/O with combinatorial or feedback register outputs
- Programmable flip-flops allow J-K, S-R, T or D types
- Programmable output polarity story suggested and the story of the
- Register set and register reset can be asynchronous or synchronous
- · Automatic register preset on power up
- Varied product term distribution
- Up to 16 product terms per output
- Pin compatible functional superset of 22V10
- Maximum propagation delay
 - 25 ns "A"
 - 35 ns "STD"
- 24-pin 300-mil-wide SKINNYDIP® package or 28-pin chip carriers save space

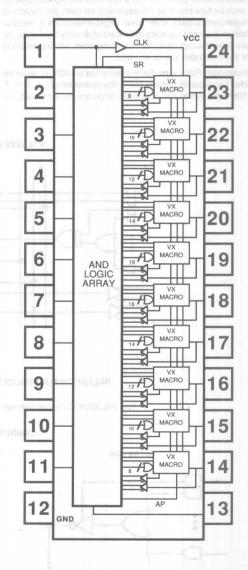
General Description

The PAL32VX10 is a high-density Programmable Array Logic device which implements the familiar sum of products transfer function via a user-programmable AND array and a fixed OR array. Featured are ten highly flexible input/output macrocells which are user configurable for combinatorial or registered operation. Each flip-flop is also programmable to be either J-K. S-R, T, or D-types for optimal design of state machines and other synchronous logic. In addition, a unique dual feedback architecture allows I/O capability for each macrocell in both combinatorial or registered configurations, even when register feedback is present, and allows implementation of buried registers while preserving the macro input function. Supplied in space-saving 300-mil-wide dual in-line packages or 28-pin chip carriers, the PAL32VX10 offers a powerful, space-saving alternative to SSI/MSI logic devices, while providing the advantage of instant prototyping over other semicustom approaches.

The PAL32VX10 is fabricated in Monolithic Memories' advanced, oxide isolated bipolar process for high speed and low power. TiW fuse links provide high reliability and programming yields. Special on-chip test circuits allow full AC, DC, and functional testing before programming. Preloadable output registers facilitate functional testing.

The PAL32VX10 can be programmed on standard PAL® device programmers, fitted with appropriate programming modules and configuration software. Design development is supported by Monolithic Memories' PALASM®2 software as well as by other programmable logic CAD tools available from third-party vendors.

Logic Symbol



PAL32VX10 macrocell are shown in the diagram below. Significant features of the macrocell are:

Dual Feedback Paths. Each macrocell has two completely independent feedback paths associated with each macrocell. One feeds back into the array from the macrocell output pin. The second feeds back into the array from the flip-flop output. This architecture provides I/O capability for both combinatorial and registered outputs, even when register feedback is needed. In addition, it allows registers to be loaded directly from outputs, and provides the capability for buried registers, while permitting use of the macrocell pin as an input.

Programmable Flip-Flops. Each macro has an XOR gate which provides the capability of emulating the operation of J-K, S-R, T, or D flip-flops. When J-K or S-R flip-flops are implemented, the between ofer and refur functions, according to the expression: $Q := Q :+: (J_1...J_m)*/Q+(K_1...K_n)*Q$

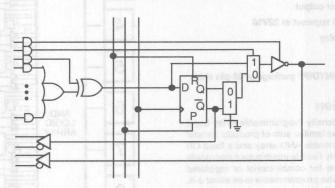
where (m+n) is the total number of product terms found in each macrocell.

Varied Product Term Distribution. The PAL32VX10 has a different number of product terms for each pair of macrocells. There are two macros each with 8, 10, 12, 14, or 16 product terms, to allow optimal use of the available product term resources.

Other Features:

- Macrocells programmable as registered or combinatorial
- Programmable output polarity
- · Preset and reset can be synchronous or asynchronous

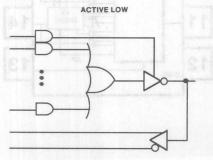
PAL32VX10 MACROCELL



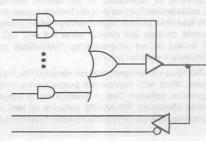
PAL32VX10 MACROCELL CONFIGURATION OPTIONS

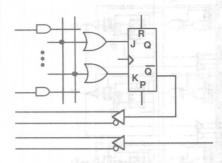
The PAL32VX10 can implement any of the architecture options shown

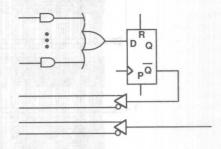
COMBINATORIAL I/O



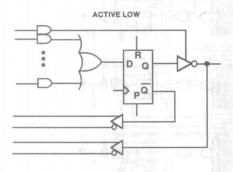


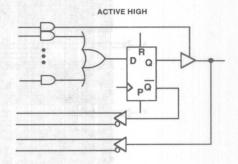




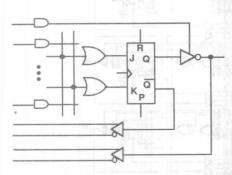


D REGISTER WITH I/O

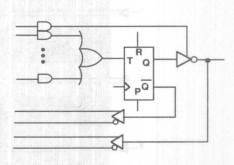




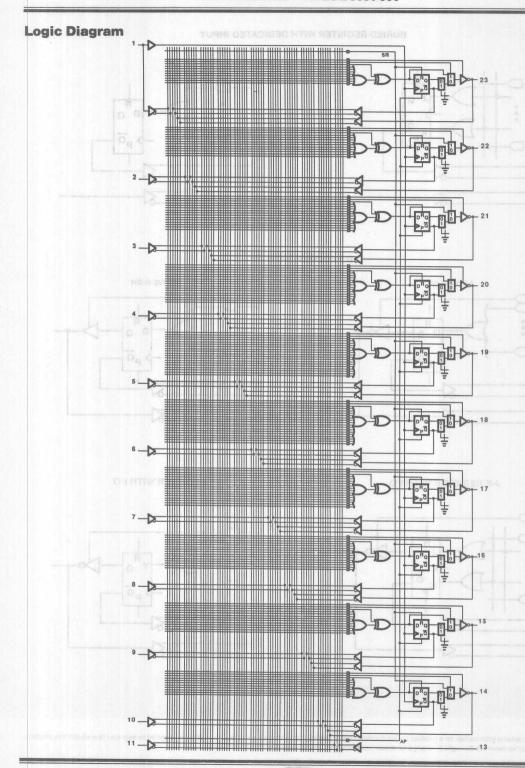
J-K REGISTER WITH I/O



T REGISTER WITH I/O



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Features/Benefits

- · Programmable replacement for conventional TTL logic
- · Reduces IC inventories and simplifies their control
- · Expedites and simplifies prototyping and board layout
- Saves space with 24-pin 0.3 inch SKINNYDIP® packages and 28-pin Plastic Leaded Chip Carriers (PLCC)
- Programmed on standard PROM programmers
- Reliable TiW fuses guarantee >99% programming yields
- Test and simulation made simple with PLEASM™ software
- Proposed JEDEC standard pinout
- Revised pinout with center VCC and GND for higher noise immunity

Description

The PLE5P16 and PLE6P16 are the two newest members of the Programmable Logic Element (PLE™) Family. A PLE device has a programmable OR-array, preceded by a fixed AND-array. This provides unlimited product terms and programmable polarity for each output, while maintaining the high speeds necessary for logic applications. The PLE Family complements the PAL® (Programmable Array Logic) Family, which has programmability in the opposite array.

The PLE5P16 has five inputs, sixteen outputs, and thirty-two product terms per output. The PLE6P16 has six inputs, sixteen

Typical Applications

- Address decoding
- Random logic replacement
- Code converters
- · Look-up tables (both trigonometric and arithmetic)
- Data scaling

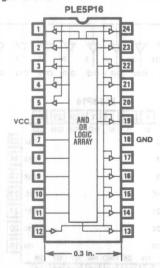
Preliminary Data

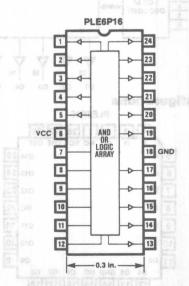
PARAMETER	PLE5P16 STANDARD	PLE6P16 STANDARD	
t _{PD} (ns)	15	15	
I _{CC} (mA)	180	190	

outputs, and sixty-four product terms per output.

The devices feature low-current PNP inputs and full Schottky clamping; the PLE5P16 has three-state outputs with an output enable. The fuses store a logical low and are programmed to the high state. Special on-chip circuitry and extra fuses provide pre-programming testing which assures high programming yields and high reliability.

Logic Symbols



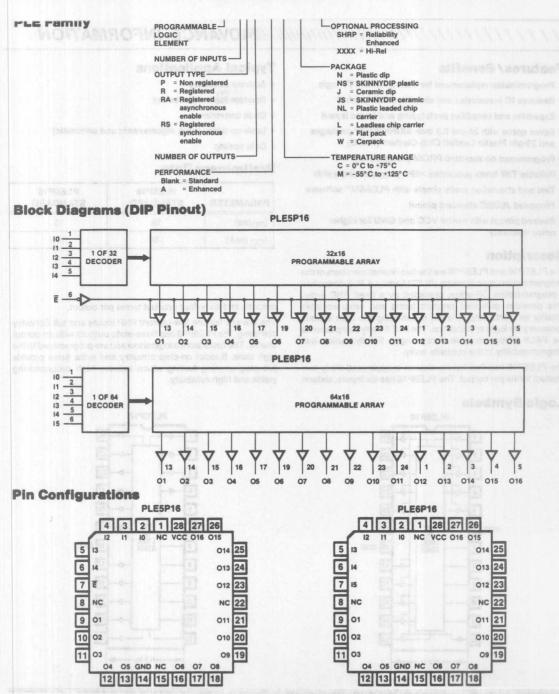


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Monolithic MM Memories



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Features / Benefits

- . Left/Right shift and rotate to any position within 1 cycle
- Expandable to any multiples of 16-bit paths
- . Works on sign magnitude and two's complement shift count inputs
- . High speed operation:

Data to output:

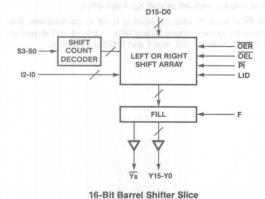
25 ns (max) Shift count to output: 30 ns (max)

- · Sticky bit available for floating point rounding operation
- · Bit insert and bypass operations

Applications

- · Mantissa adjustment for floating point addition/ subtraction and fixed point scaling in minicomputers, mainframes, array processors and digital signal processors
- · Positioning non-numeric patterns in image processing, word processing and symbol processing systems
- . Implement a funnel shifter for the Bit Block Transfer operation in graphics
- · Implement a compression-expansion engine using the modified Huffman coding method
- . Bit insertion for EDAC applications

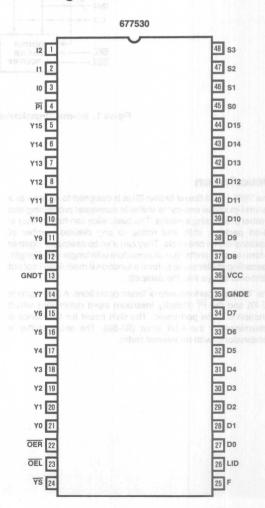
Block Diagram



Packaging Information

PART NUMBER	PACKAGE	TEMPERATURE
677530	D48	Commercial

Pin Configuration



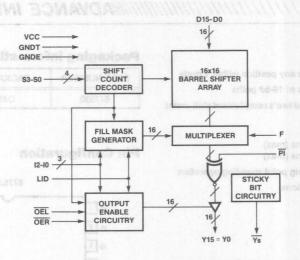


Figure 1. Internal Organization of the '7530 Barrel Shifter Slice

Description

The '7530 16-Bit Barrel Shifter Slice is designed to be used as a general-purpose one-cycle shifter in numerical processing and symbol processing systems. The basic slice can handle data in 16-bit packets, shift and rotate to any desired number of positions within one cycle. They can also be cascaded together to form a barrel shifter function module with longer word length. Cascading shifter slices to form a functional module will not put additional delays into the datapath.

The '7530 can perform nine different operations. A 3-bit opcode (I2-I0) and the $\overline{\text{PI}}$ (Polarity Insertion) input determines which function is to be performed. The shift count for the device is determined by the 4-bit input (S3-S0). The entire shifter is combinatorial with no internal states.

All data outputs (Y15-Y0) can be tristated. This output design is crucial to the cascading architecture because outputs from different barrel shifter slices will be tied together in an expanded array. The \overline{OER} , \overline{OEL} (Output Enable Right/Left) and the LID (Location IDentifier) input signals together determine the enable states of each individual output.

The F (Fill) input bit provides the signal to be inserted into the outputs.

The $\overline{\text{Ys}}$ output (Sticky Bit) is provided as an open collector output. It is the negation of the logical OR of all the bits shifted out during the shift left or shift right operation.

The \overline{PI} (Polarity/Insertion) input is used to complement the outputs for all the opcodes except when I = 010 when it is used to distinguish between Bit InserT and BYPass operation.

Architecture

As shown in Figure 1, the architecture of the '7530 Barrel Shifter Slice is centered around the internal barrel shifter array and the shift count decoder. The outputs of the array are fed into a mask generator which determines the enable states of each individual data outputs. These enable states are primarily determined by the LID (Location IDentifier) input signal that represents the location of each shifter slice when they are cascaded. The Location IDentifier will transform the actual operation of every shifter to make cascading possible. Please refer to the section Cascading Architecture for the Barrel Shifter Slice for a detailed description.

The output control circuitry consists of the polarity control, Fill bit insertion and Sticky Bit generation.

Two enable inputs, OEL and OER, provide the tristate control to the two portions of the output data separated by the left margin (D15) of the original input data.

Signal Description

D15-D0: Inputs. Input data to the Barrel Shifter Slice.

Y15-Y0: Outputs. Output data from the Barrel Shifter Slice.

I2-I0: Inputs. A 3-bit opcode to select one of nine possible operations for the device. Please see Table 1 for further detail.

S3-S0: Inputs. Shift count input. For opcodes 00X or 11X (i.e., I2I1I0 = 0, 1, 6 or 7), S3-S0 represent the magnitude of bit positions shifted or rotated. For opcodes 10X (i.e., I2I1I0 = 4 or 5), the number of bits to be shifted or rotated is given by the two's complement of the five-digit number: I2S3S2S1S0. Since I2 = 1 in both cases, only sixteen different bit positions (ranging from +1 to +16) are allowed within one cycle. For the opcodes X01 (i.e., I2I1I0 = 1 or 5), the shift count inputs can be considered in two ways: either as a rotate right two's complement I2S3S2S1S0 operation or as a rotate left S3S2S1S0 operation when I2 = 0.

 \overline{PI} : Input. Polarity/Insertion signal input. This signal serves two purposes. When the opcode is 010 (i.e., I2I1I0 = 2), it is used to resolve between Bit InserT operation (\overline{PI} = 0) and BYPass operation (\overline{PI} = 1). When the opcode is in some other states, \overline{PI} determines the output data polarity (\overline{PI} = 0 for complemented data, \overline{PI} = 1 for uncomplemented (true) data).

F: Input. Fill bit input. The value of this input is used to insert into positions left empty from shift operations, or insert into the designated bit positions for the Bit InserT and FILL operations.

Ys: Output. The inverse of the sticky bit. This is an open collector output signal. Functionally this signal is the negation of the logical OR of the bits shifted out in the shift left/right operations. In the Bit Insertion operation, Ys is the negation of the input bit that is replaced by the Fill bit.

LID: Input. Location IDentifier. The input to this pin can either be VCC, ground, or left open. In the case when the input is open, there is an internal resistor network to divide this signal to 2.5 V (VCC/2). The LID signal is used in the expansion scheme of the barrel shifter slices. Different barrel shifter slices can be cascaded in a two-dimensional array to form a barrel shifter module of wider path width. The LID input signal is required to be one of the above three states according to its position inside the array.

OEL, OER: Inputs. Output enable left and output enable right. These two signals will separately enable the left and the right halves of the output data separated by the left margin (D15) of the input word.

GNDE, GNDT: Power supply grounds. GNDE is the internal ECL circuit ground and GNDT is the internal TTL cricuit ground. These two ground signals should be routed separately in the system. The ECL ground is more sensitive to noise problems and should be bypassed with capacitive components to VCC.

VCC: Power supply. A +5 V power supply to the internal circuit of the Barrel Shifter Slice.

Function Tables

C	PCOD	E	POLARITY/	CO THE THE	ERATION PERFORMED	OUTPUT	ALTERNATE OF	PERATION
12	ol ₁	lo	INSERT	MN.	F LID PIN IS "OPEN" NAME	POLARITY	LID =	LID = GND
0	0	0	0	LSH	Left SHift	Complemented True	miote LRT (Sw helitis	FIL
0	0	1 an	0 m da	LRT	Left RoTate	Complemented True	LRT	LRT
0	1	0	0	BIT BYP	Bit InserT BYPass	True True	High Z High Z	High Z High Z
0	1 1 10	1	0	FIL	FILLEd testiles integrated in product in pro	Complemented True	High Z High Z	High Z High Z
1um	0	0	ened 0 est	RSC	Right Shift with two's— Complement shift count	Complemented True	FIL notigitate	RRC
1	0	1	0	RRC	Right Rotate with two's— Complement rotate count	Complemented True	RRC	RRC
1	do 1 de s facilis	0	0	RSH	Right SHift	Complemented True	FIL	RRT
1	1	1	0	RRT	Right RoTate	Complemented True	on GERRT A to 8	RRT

Figure 1. Shifter Instruction Set 10 of 10

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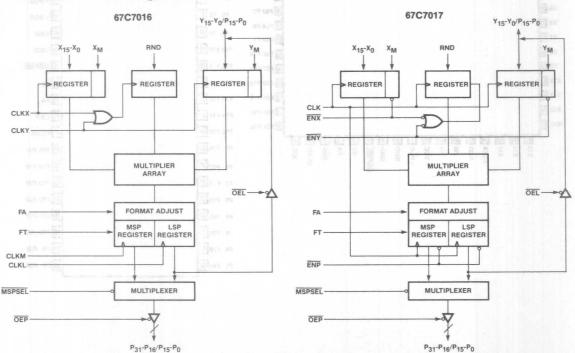
Features/Benefits

- 16x16 parallel multiplier
- · High speed multiply
 - 35 ns Max '7016-35/'7017-35
 - 45 ns Max '7016-45/'7017-45
 - 55 ns Max '7016-55/'7017-55
- Low power CMOS technology
 - Zero standby power
 - 7 mA per MHz active I_{CC} (Typical)
- . Mixed mode 2's complement, unsigned or mixed operand
- · '7017 is optimized for microprocessor systems, single clock with register enables
- Plug-in compatible with TRW MPY016H/K, AMD29516/A, 29517/A
- Single 5 V supply
- · Available in DIP or PLCC

Packaging Information

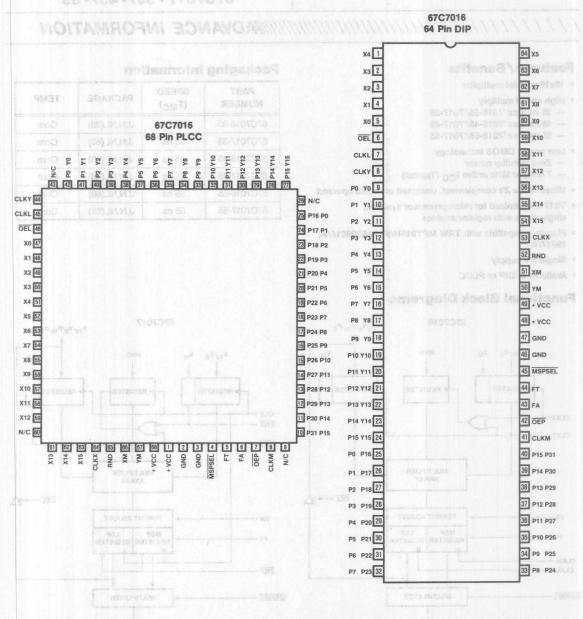
PART NUMBER	SPEED (T _{MC})	PACKAGE	TEMP
67C7016-35	35 ns	J,N,NL(68)	Com
67C7017-35	35 ns	J,N,NL(68)	Com
67C7016-45	45 ns	J,N,NL(68)	9 Com
67C7017-45	45 ns	J,N,NL(68)	Com
67C7016-55	55 ns	J,N,NL(68)	Com
67C7017-55	55 ns	J,N,NL(68)	Com

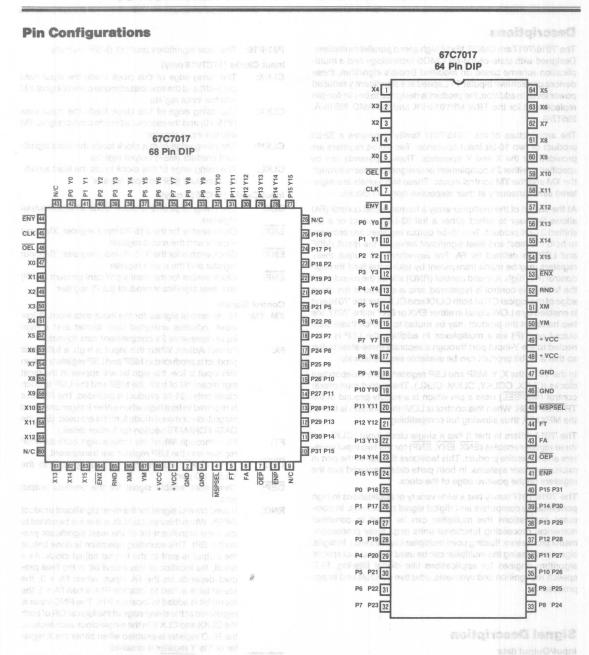
Functional Block Diagrams



This document contains information on a product under development at Monolithic Memories Inc. The information is intended to help you to evaluate this product. Monolithic Memories reserves the right to change or discontinue work on this proposed product without notice.

Pin Configurations





Descriptions

The '7016/7017 are CMOS 16x16 high speed parallel multipliers. Designed with state-of-the-art CMOS technology and a multiplication scheme based on modified Booth's algorithm, these devices can achieve bipolar TTL speed at a significantly reduced power level. In addition, the product is designed to be pin-for-pin replacement for the TRW MPY016H/K and the AMD 29516/A, 29517/A.

The architecture of the '7016/7017 family generates a 32-bit product of two 16-bit input operands. Two 16-bit registers are provided for the X and Y operands. These operands can be specified as either 2's complement or unsigned numbers through the XM and the YM control inputs. These two signals are registered simultaneously at their respective operand clocks.

At the output of the multiplier array a format adjust control (FA) allows the user to select either a full 32-bit product or a left shifted 31-bit product. Two 16-bit output registers are provided to hold the most and least significant halves of the result (MSP and LSP) as defined by FA. For asynchronous output these registers may be made transparent by taking the feed through control (FT) high. A round control (RND) allows the rounding of the MSP. This control is registered, and is entered at the rising edge of the logical OR of both CLKX and CLKY for the '7016 and is enabled by a LOW signal in either ENX or ENY in the '7017. the two halves of the product may be routed to a 16-bit three-state output port (P) via a multiplexer. In addition the LSP is connected to the Y-input port through a separate three-state buffer so that a 32-bit product can be available simultaneously.

In the '7016, the X, Y, MSP and LSP registers have independent clocks (CLKX, CCLKY, CLKM, CLKL). The output multiplexer control (MSPSEL) uses a pin which is a supply ground in the TRW MPY16H. When this control is LOW the function is that of the MPY16H, thus allowing full compatibility.

The '7017 differs in that it has a single clock input (CLK) and three register enables (ENX, ENY, ENP) for the two input registers and the entire product. This facilitates the use of the part in microprocessor systems. In both parts data is entered into the registers on the positive edge of the clock.

The '7016/7017 family has a wide variety of applications in high performance computers and digital signal processing. In computer applications this multiplier can be used to construct numerical processing functional units (e.g., array processors, matrix processors, floating point multiplier/dividers etc.). In digital signal processing the multiplier can be used to construct special algorithm engines for applications like digital filtering, FFT, speech recognition and synthesis, adaptive controls and image processing.

Signal Description

Input/Output data

X15-X0: 16 bit data inputs.

Y15-Y0: 16 bit data inputs. These inputs are multiplexed with

the least significant product (LSP) outputs.

P15-P0: The least significant product (LSP) outputs. These signals are multiplexed with the Y data inputs. The

product term is available when OEL is low. Alternatively, these outputs can be accessed from the MSP

output port when MSPSEL is high.

P31-P16: The most significant product (MSP) outputs.

Input Clocks (67C7016 only)

The rising edge of this clock loads the input data CLKX: (X15-X0) and the associated mode control signal XM

into the input register.

CLKY: The rising edge of this clock loads the input data (Y15-Y0) and the associated mode control signal YM

into the input register.

CLKM: The rising edge of this clock loads the most signifi-

cant product (MSP) output register.

CLKL: The rising edge of this clock loads the least significant product (LSP) output register.

Input Clocks (67C7017 only)

CLK: The rising edge of this clock loads all input/output

registers ENX: Clock enable for the X15-X0 input register, XM input

register and the round register. ENY: Clock enable for the Y15-Y0 input register, YM input

register and the round register. FNP-Clock enable for the most significant product (MSP) and least significant product (LSP) register.

Control Signals

XM, YM: Mode control signals for the input data word. A low input indicates unsigned data format and a high input represents 2's complement data format.

FA: Format Adjust. When this input is high, a full 32-bit product is produced in MSP and LSP registers. When this input is low, the sign bit will appear in the most significant bit of both the MSP and the LSP. In such cases only a 31-bit product is provided. The FA input is required to be a high when either integer unsigned magnitude or mixed mode formats are used. (See the DATA FORMATS section for further detail.)

FT: Flow-through. When this input is high, both the MSP register and the LSP register are transparent.

OEL: Three-state enable signal for routing LSP to the Y/LSP I/O ports.

OEP: Three-state enable signal for the product output

RND: Round control signal for the most significant product

(MSP). When this input is high, a one will be added to the most significant bit of the least significant product (LSP). This rounding operation is done before the output is sent to the format adjust clock. As a result, the location of this round bit in the final product depends on the FA input. When FA = 0, the round bit is added to location P14; when FA = 1, the round bit is added to location P15. The RND input is registered at the rising edge of the logical OR of both the CLKX and CLKY. In the single clock architecture. the RND register is enabled when either the X register or the Y register is enabled.

MSPSEL: When the MSPSEL input is low, the MSP is available for the output port. When this input is high, the LSP is

available at the output port.

Features/Benefits

- · Twos-complement, unsigned, or mixed operands
- · Full 32-bit product immediately available on each cycle
- High-speed 16x16 parallel multiplier
- · Latched or registered inputs/outputs
- Three-state output controls, independent for each half of the product
- Single +5 V supply (via multiple pins)
- Zero standby power CMOS technology
- Available in 84-terminal Leadless-Chip Carrier and 88-Pin-Grid-Array packages

Description

The 'C7555 and 'C7556 are high-speed 16x16 combinatorial multipliers which can multiply two 16-bit unsigned or signed twos-complement numbers on every cycle. Each operand X and Y has an associated mode-control line, XM and YM respectively. When a mode-control line is at a LOW logic level, the operand is treated as an unsigned 16-bit number; when the mode-control line is at a HIGH logic level, the operand is treated as a 16-bit signed twos-complement number. Additional inputs RS and RU allow the addition of a bit into the multiplier array at the appropriate bit positions for rounding.

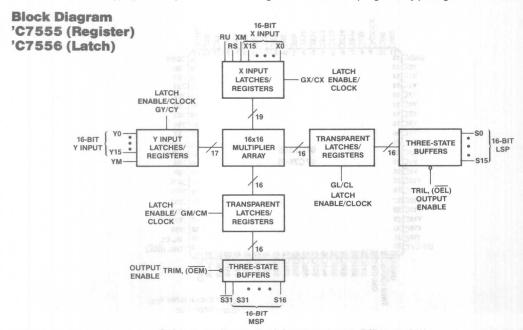
Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
67C7555	P88, L84	Com
67C7556	P88, L84	Com

The entire 32-bit double-length product is available at the outputs at one time.

The most-significant product bit, S31, is available in both true and complemented form to simplify longer-wordlength multiplications. The product outputs are three-state, controlled by assertive-low enables. The MSP outputs are controlled by the TRIM $(\overline{\text{OEM}})$ control input, while the LSP outputs are controlled by the TRIL $(\overline{\text{OEL}})$ control input. This allows one or more multipliers to be connected to a parallel bus or to be used in a pipelined system.

All inputs and outputs have transparent latches in the 'C7556. The latches become transparent when the input to the corresponding gate control line GX, GY, GM, GL is HIGH. If latches are not required, these control inputs may be tied HIGH, leaving the multiplier fully transparent for combinatorial cascading. The device uses a single +5 V power supply, and is available both in an 84-terminal leadless chip carrier (LCC) packalland in an 88-pin-grid-array package.



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	SUMMARY OF SIGNALS/PINS
X ₁₅ -0	Multiplicand 16-bit data inputs
Y ₁₅₋₀	Multiplier 16-bit data inputs
XM, YM	Mode-control inputs for each data word; LOW for unsigned data and HIGH for twos- complement data
S ₃₁₋₀	Product 32-bit output
S ₃₁	Inverted MS product bit (for expansion)
RS, RU	Rounding inputs for signed and unsigned data, respectively
GX/CX	Gate contro/clock for Xi, RS, RU
GY/CY	Gate control/clock for Yi
GL/CL	Gate control/clock for least-significant half
GM/CM	Gate control/clock for most-significant half of product
TRIL	Three-state control for least-significant half of product
TRIM	Three-state control for most-significant half of product

Multiplier Since

Rounding Inputs

INP	UTS	ADDS		USUALLY	USED WITH
RU	RS	215	214	XM	YM
L	L	No	No	X	X
L	Н	No	Yes	H†	H†
Н	Sirtuan	Yes	No	Pierra Luena	L
Н	Н	Yes	Yes	*	*

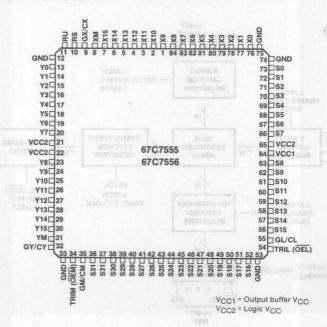
[†] In mixed mode, one of these could be low but not both.

Mode-Control Inputs

OPERATING MODE	INPU1	MODE- CONTROL INPUTS		
	X ₁₅₋₀	Y ₁₅₋₀	XM	YM
Unsigned	Unsigned	Unsigned	bn/L det	TOL:
Mixed	Unsigned	Twos-Comp.	oirlw st	Н
	Twos-Comp.	Unsigned	aH as	YL
Signed	Twos-Comp.	Twos-Comp.	Н	Н

private line is at a HIGH logic level, the operand is

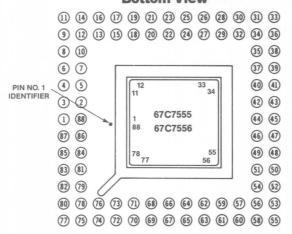
84-Terminal Leadless Chip Carrier Pinout



All V $_{CC}$ and GND pins must be connected to the respective V $_{CC}$ and GND connections on the board and should not be used for daisychaining through the IC.

^{*} Usually a nonsense operaion.

88 Pin-Grid-Array Pin Location Bottom View

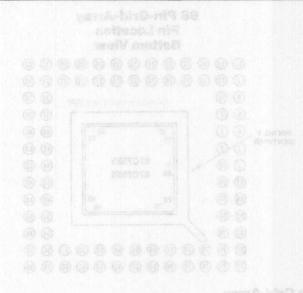


Pin-Guide for Pin Grid Array

PIN NUMBER	PIN NAME	PIN NUMBER	PIN NAME	PIN NUMBER	PIN NAME	PIN NUMBER	PIN NAME
1	Х9	23	N/C*	45	S25	67	VCC2†
2	X10	24	Y8	46	S24	68	N/C*
3	X11	25	Y9	47	S23	69	S7
4	X12	26	Y10	48	S22	70	S6
5	X13	27	Y11	49	S21	71	S5
6	X14	28	Y12	50	S20	72	S4
7	X15	29	Y13	51	S19	73	S3
8	XM	30	Y14	52	S18	74	S2
9	GX/CX	31	Y15	53	S17	75	S1
10	RS	32	YM	54	S16	76	S0
11	RU	33	GY/CY	55	GND	77	GND
12	GND	34	N/C*	56	TRIL (OEL)	78	N/C*
13	Y0	35	GND	57	GL/CL	79	GND
14	Y1	36	TRIM (OEM)	58	S15	80	X0
15	Y2	37	GM/CM	59	S14	81	X1
16	Y3	38	S31	60	S13	82	X2
17	Y4	39	S31	61	S12	83	Х3
18	Y5	40	S30	62	S11	84	X4
19	Y6	41	S29	63	S10	85	X5
20	Y7	42	S28	64	S9	86	X6
21	VCC2†	43	S27	65	S8	87	X7
22	VCC2†	44	S26	66	VCC1††	88	X8

^{*} Not connected. † V_{CC2} = Logic V_{CC}. †† V_{CC1} = Output buffer V_{CC}.

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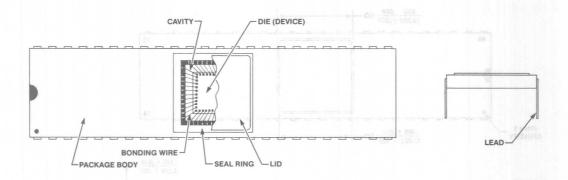
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Side Brazed Package



PACKAGE BODY

Alumina (Standard Dark)

BONDING WIRE

1.25 Mil Aluminum

LID

Gold Plated Kovar With Nickel Underplating

CAVITY/SEAL RING

Gold Over Nickel Over Tungsten

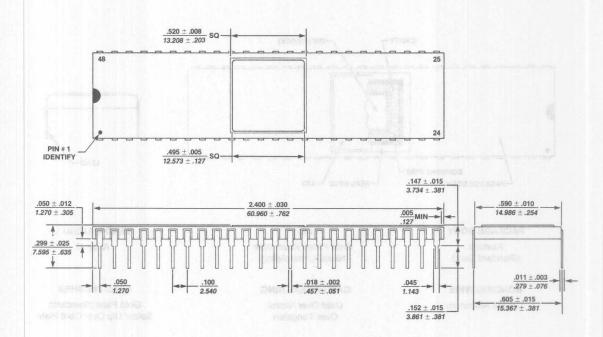
LEAD MATERIAL

Alloy 42

LEAD FINISHES

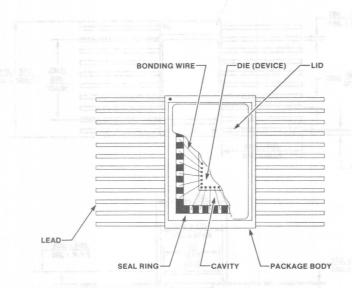
Gold Plate (Standard) Solder Dip Over Gold Plate

48D Side Brazed Ceramic DIP (1/2"x2 7/16")



UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES
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ALL TOLERANCES ARE ±.007 INCHES

Flat Pack



PACKAGE BODY

Alumina

BONDING WIRE

1.25 Mil Aluminum

LID

Gold Plated Kovar With Nickel Underplating

CAVITY/SEAL RING

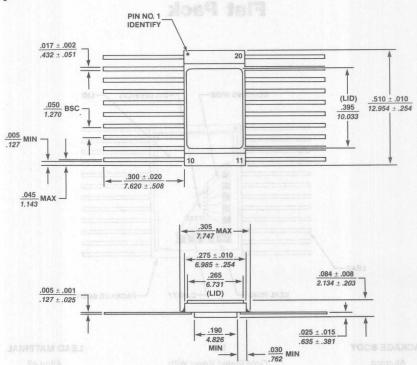
Gold Over Nickel Over Tungsten LEAD MATERIAL

Alloy 42

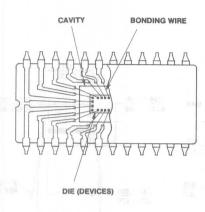
LEAD FINISHES

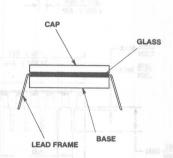
Gold Plate (Standard) Solder Dip Over Gold Plate

20F Flat Pack Mil-M-38510, Appendix C, F-9



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LEAD FRAME

Alloy 42

BONDING WIRE

1.25 Mil Aluminum

CAP AND BASE

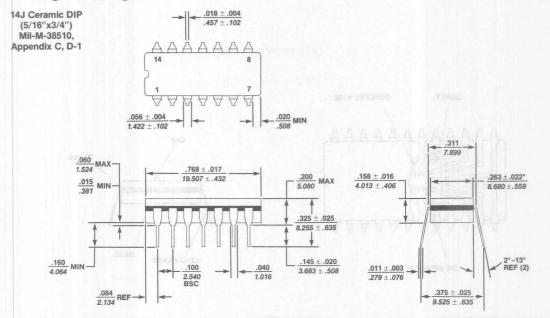
Pressed Alumina

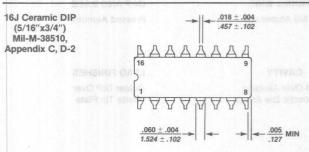
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Vitreous Solder Glass CAVITY

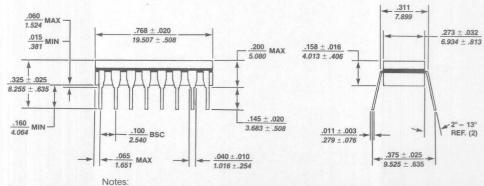
Gold Over Alumina For Eutectic Die Attach **LEAD FINISHES**

Solder DIP Over Matte Tin Plate

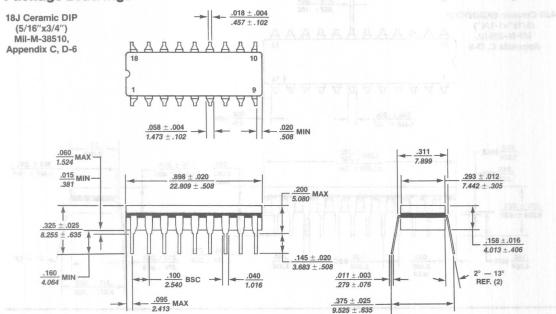


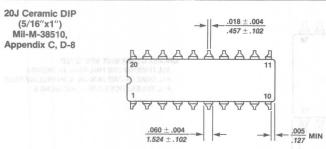


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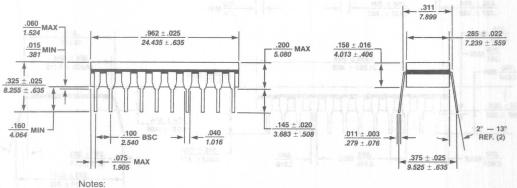


- Specified body dimensions allow for differences between SSI, MSI and LSI packages.
- Lead material tolerances are for tin plate finish only. Solder dip finish adds 2-10 mils thickness to all lead tip dimensions.

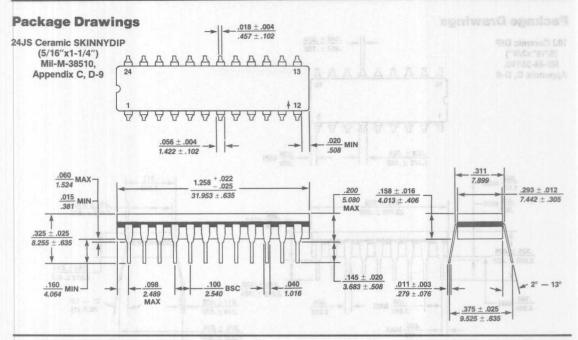


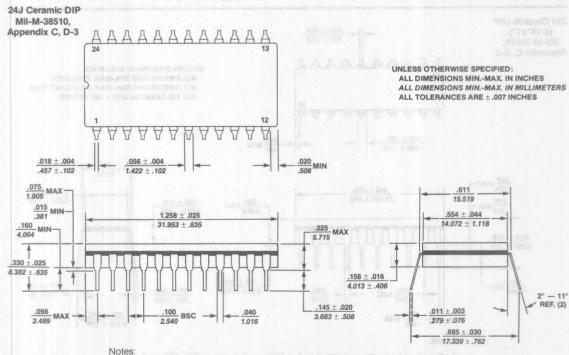


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ALL TOLERANCES ARE ± .007 INCHES



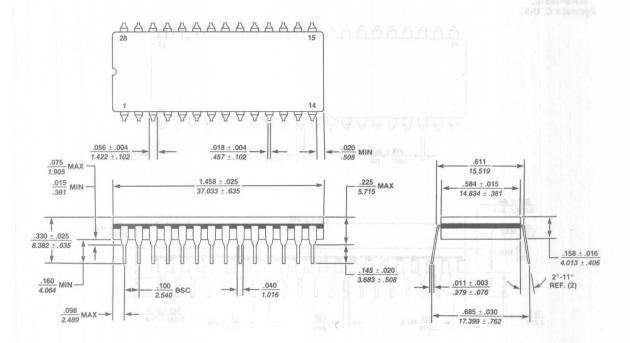
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- Lead material tolerances are for tin plate finish only. Solder dip finish adds
 2-10 mils thickness to all lead tip dimensions.





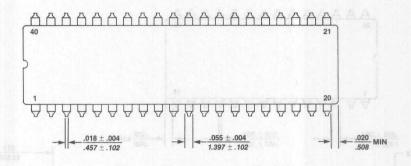
- 1. Specified body dimensions allow for differences between MSI and LSI packages.
- Lead material tolerances are for tin plate finish only. Solder dip finish adds 2-10 mils thickness to all lead tip dimensions.

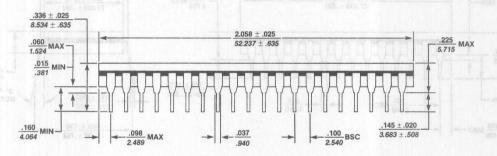
28J Ceramic DIP (1/2"x1 1/2")

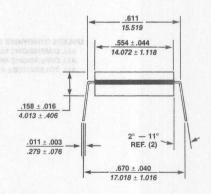


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40J Ceramic DIP (9/16"x2-1/16") Mil-M-38510, Appendix C, D-5





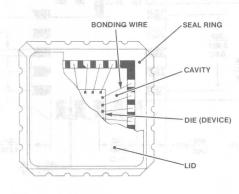


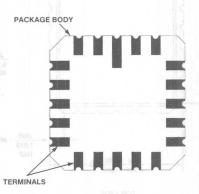
UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE ± .007 INCHES

Notes

- Specified body dimensions allow for differences between MSI and LSI packages.
- 2. Lead material tolerances are for tin plate finish only. Solder dip finish adds 2-10 mils thickness to all lead tip dimensions.

Leadless Chip Carrier





PACKAGE BODY

Alumina (Standard Dark)

BONDING WIRE

1.25 Mil Aluminum

LID

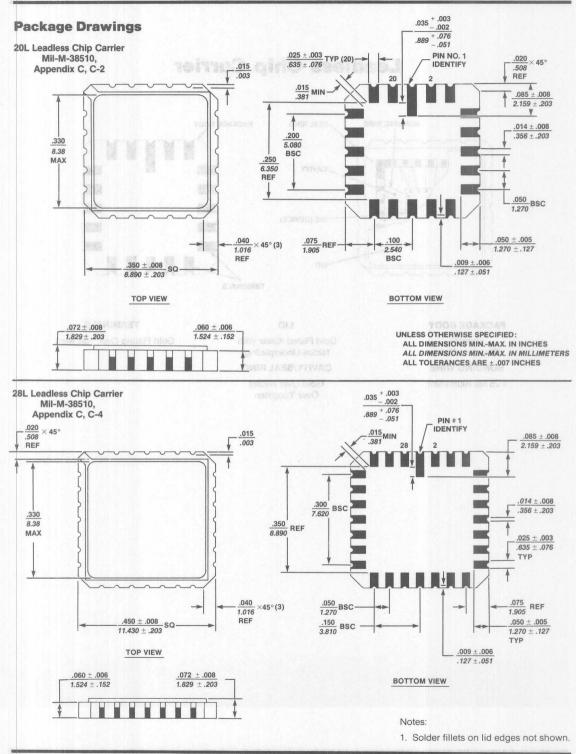
Gold Plated Kovar With Nickel Underplating

CAVITY/SEAL RING

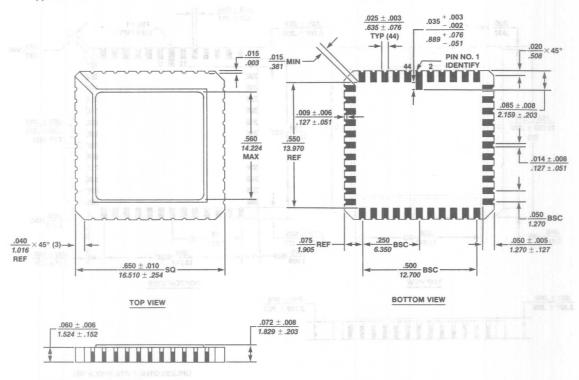
Gold Over Nickel Over Tungsten

TERMINALS

Gold Plating Over Tungsten

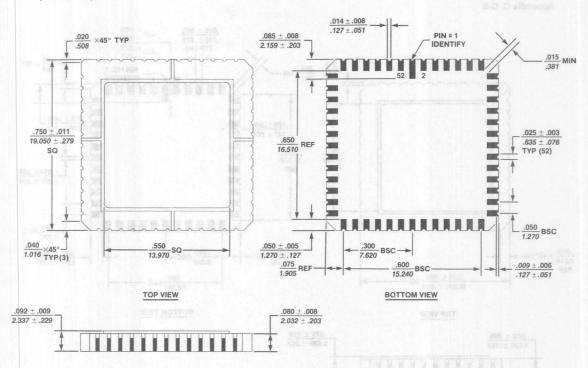


44L Leadless Chip Carrier Mil-M-38510, Appendix C, C-5



UNLESS OTHERWISE SPECIFIED: ALL DIMENSIONS MIN.-MAX. IN INCHES ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS ALL TOLERANCES ARE ± .007 INCHES

52L Leadless Chip Carrier (.750"x.750")

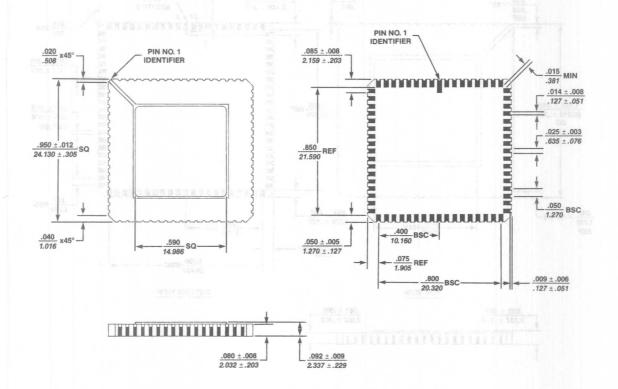


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ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE ± .007 INCHES

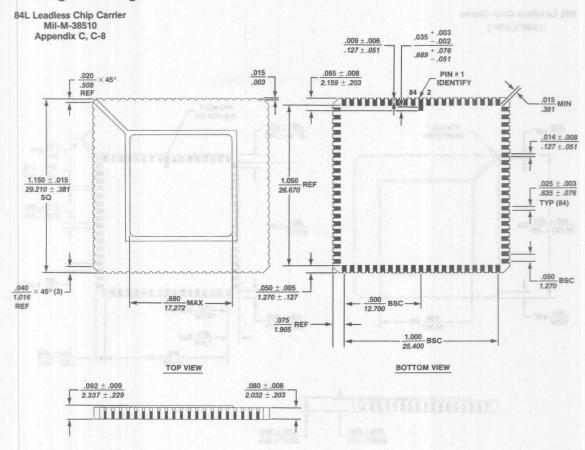
Notes:

1. Solder fillets on lid edges not shown.

68L Leadless Chip Carrier (.950"x.950")



UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE ± .007 INCHES

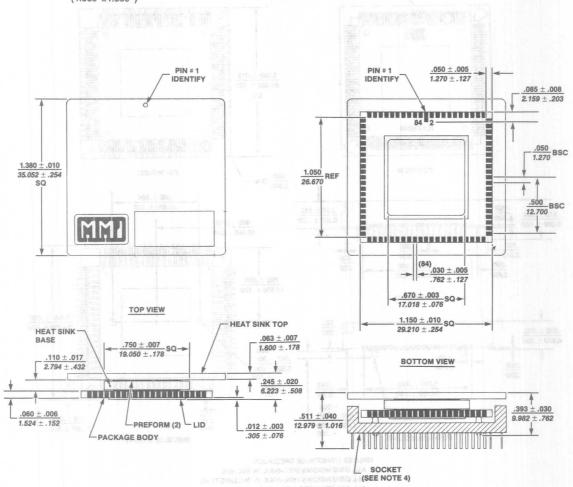


UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE ± .007 INCHES

Notes

1. Solder fillets on lid edges not shown.

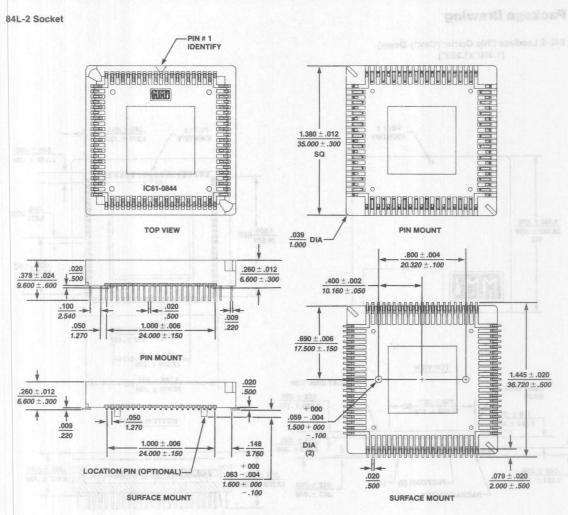
84L-2 Leadless Chip Carrier (Cavity Down) (1.380"x1.380")



UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE ± .007 INCHES

Notes

1. Solder fillets on lid edges not shown.

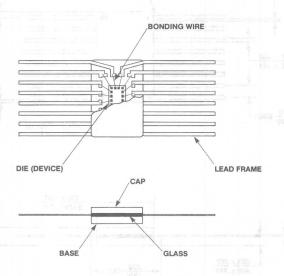


UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE ±.007 INCHES

Socket Specifications (all values from Yamaichi/Nepenthe data sheet):

1.	Insulation Resistance 1,000 M Ω minimum at 500 V DC
	Dielectric Withstanding Voltage
3.	Contact Resistance
4.	Rated Current Per Contact 1 A maximum
5.	Operating Temperature
6	Contact Force 85 grams min for each contact

Cerpack



LEAD FRAME

Alloy 42

BONDING WIRE

1.25 Mil Aluminum

CAP AND BASE

Pressed Alumina

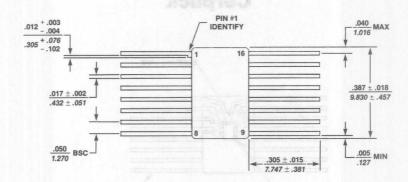
GLASS

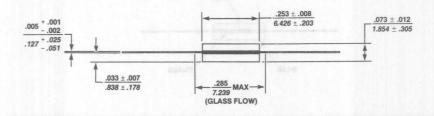
Vitreous Solder Glass CAVITY

Gold Over Alumina For Eutectic Die Attach LEAD FINISHES

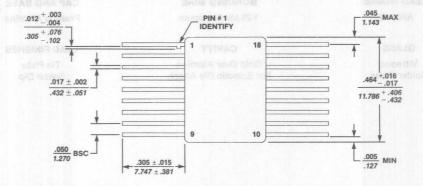
Tin Plate Solder Dip

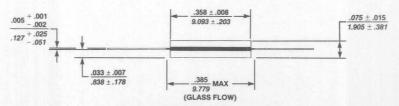
16W Cerpack Mil-M-38510, Appendix C, F-5





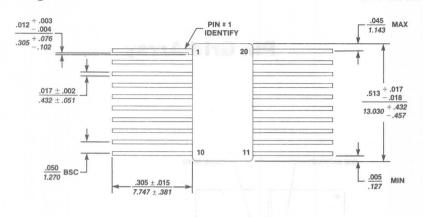
18W Cerpack

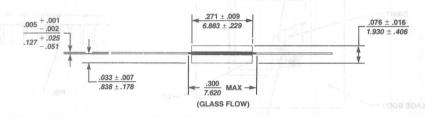




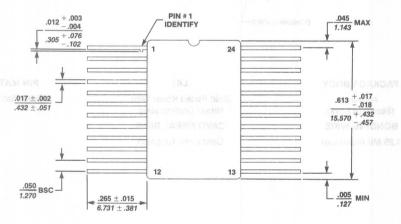
UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE ±.007 INCHES

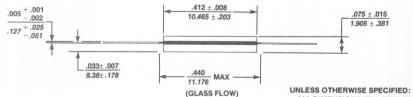
20W Cerpack Mil-M-38510, Appendix C, F-9





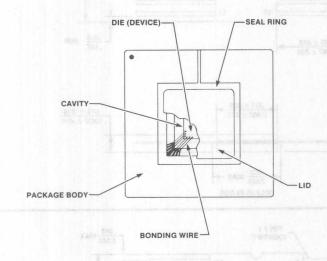
24W Cerpack Mil-M-38510, Appendix C, F-6

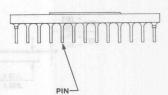




JNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE ± .007 INCHES

Pin Grid Array





PACKAGE BODY

Alumina (Standard Dark)

BONDING WIRE

1.25 Mil Aluminum

LID

Gold Plated Kovar With Nickel Underplating

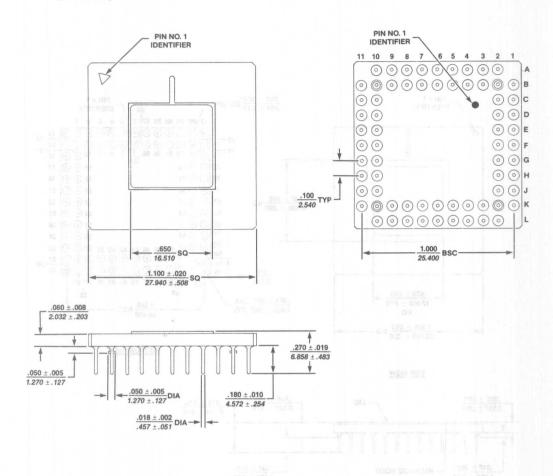
CAVITY/SEAL RING

Gold Over Tungsten

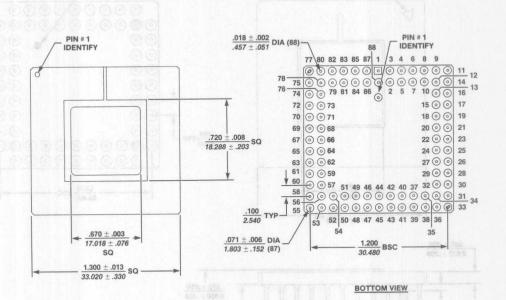
PIN MATERIAL

Gold Plated Kovar

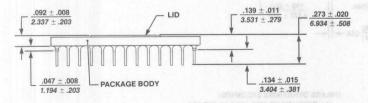
68P Ceramic Pin Grid Array (Cavity Up) (1.100x1.100)



UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE ± .007 INCHES

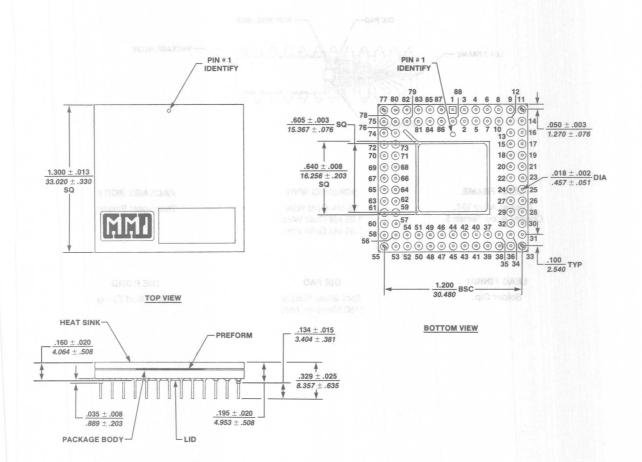


TOP VIEW



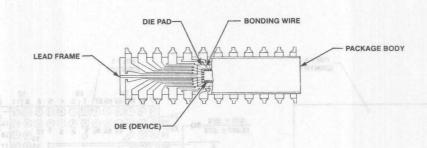
UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE ±.007 INCHES

88P-2 Pin Grid Array (Cavity Down) (1.300"x1.300")



UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE ± .007 INCHES

Molded DIP



LEAD FRAME

Copper Alloy 194. Copper Alloy Tamac 5.

BONDING WIRE

1.0 Mil Gold Wire. 1.25 Mil Gold Wire. 1.30 Mil Gold Wire.

PACKAGE BODY

Thermoset Plastic.

LEAD FINISH

Solder Dip.

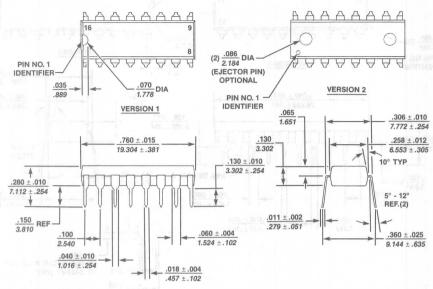
DIE PAD

Spot Silver Plating (150 Micro-Inches)

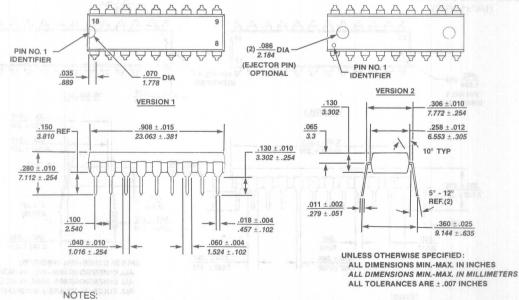
DIE BOND

Silver Filled Epoxy.

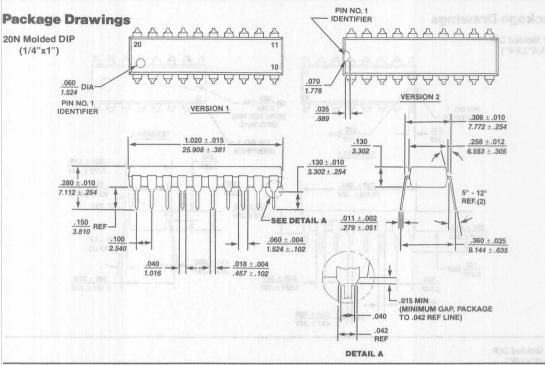
16N Molded DIP (1/4"x3/4")

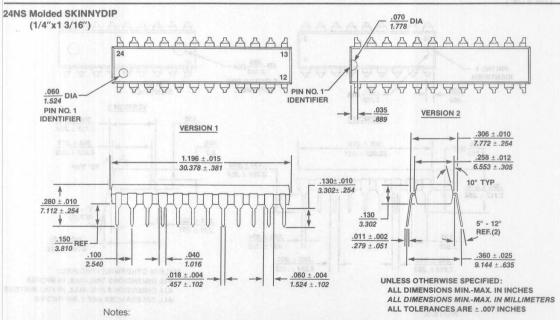


18N Molded DIP (1/4"x7/8")



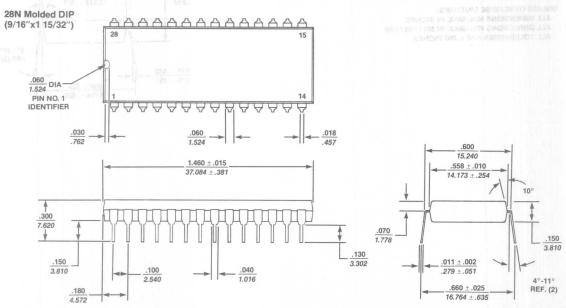
- 1. Lead material tolerances are for tin plate finish only. Solder dip finish adds 2-10 mils thickness to all lead tip dimensions.
- 2. Both Version 1 and Version 2 configurations are manufactured interchangeably.
- 3. Ejector pin marks on Version 1 are optional.





- Lead material tolerances are for tin plate finish only. Solder dip finish adds
 2-10 mils thickness to all lead tip dimensions.
- 2. Both version 1 and version 2 configurations are manufactured interchangeably.
- 3. Ejector pin marks on version 1 are optional.

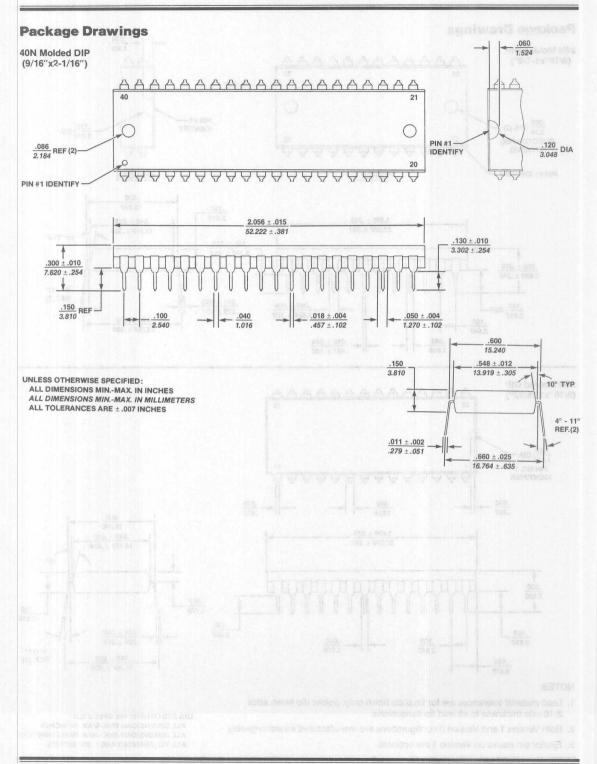
Package Drawings .060 1.524 24N Molded DIP (9/16"x1-1/4") PIN #1 -.086 2.14 DIA (2) .120 3.048 DIA IDENTIFY (EJECTOR PIN) OPTIONAL PIN #1 IDENTIFY **VERSION 1 VERSION 2** .600 15.240 .150 3.810 1.256 ± .015 .548 ± .012 31.902 ± .381 13.919 ± .305 10° TYP .130 ± .010 3.302 ± .254 .300 ± .010 7.620 ± .254 4° - 11° REF.(2) .011 ± .002 .150 3.810 REF .279 ± .051 1.524 ± .102 .660 ± .025 .100 16.764 ± .635 2.540 .018 ± .004 .457 ± .102



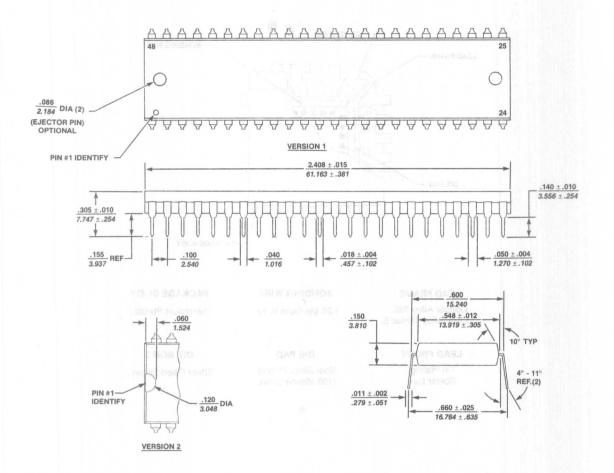
NOTES:

- Lead material tolerances are for tin plate finish only. Solder dip finish adds 2-10 mils thickness to all lead tip dimensions.
- 2. Both Version 1 and Version 2 configurations are manufactured interchangeably.
- 3. Ejector pin marks on Version 1 are optional.

UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE: .007 INCHES



48N Molded DIP (9/16"x2 13/32")



UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE ± .007 INCHES

Notes:

- Lead material tolerances are for tin plate finish only. Solder dip finish adds 2-10 mils thickness to all lead tip dimensions.
- 2. Both version 1 and version 2 configurations are manufactured interchangeably.
- 3. Ejector pin marks on version 1 are optional.

LEAD FRAME

Copper Alloy 195. Copper Alloy Tamac 5.

LEAD FINISH

Tin Plating. Solder Dip. **BONDING WIRE**

1.25 Mil Gold Wire

DIE PAD

Spot Silver Plating (150 Microinches).

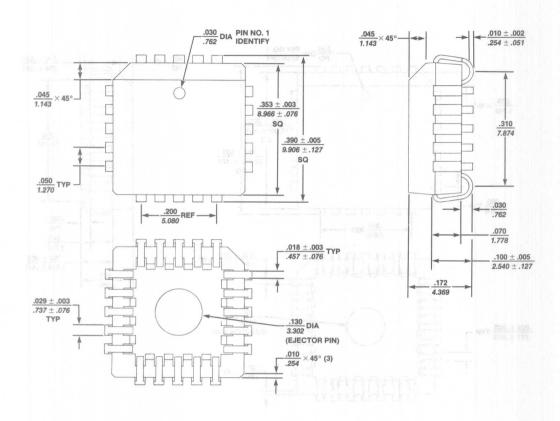
PACKAGE BODY

Thermoset Plastic.

DIE BOND

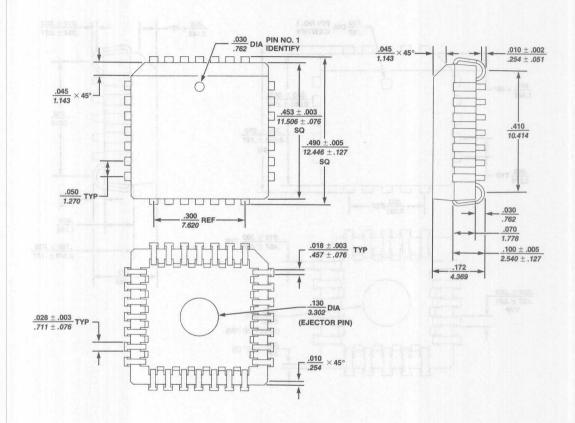
Silver Filled Epoxy.

20NL Molded Chip Carrier (.351"x.351")



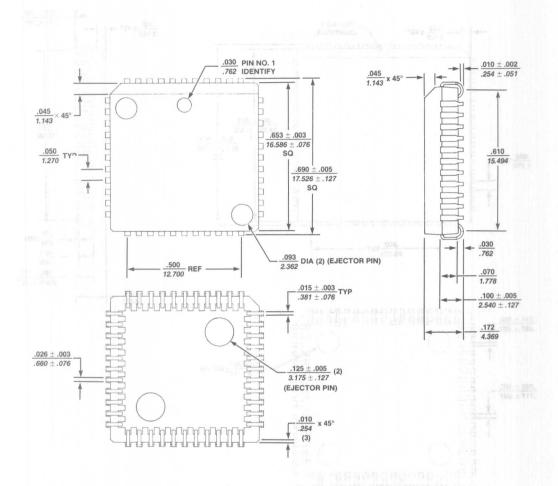
UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE ±.007 INCHES

28NL Molded Chip (.451"x.451")



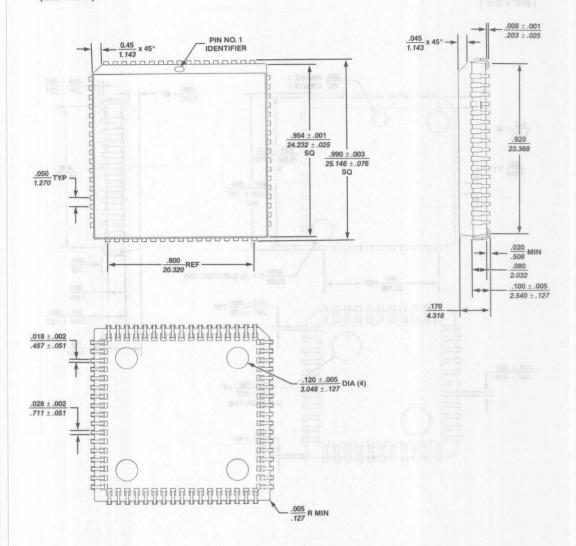
UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE ± .007 INCHES

44NL Molded Chip Carrier (.650"x.650")

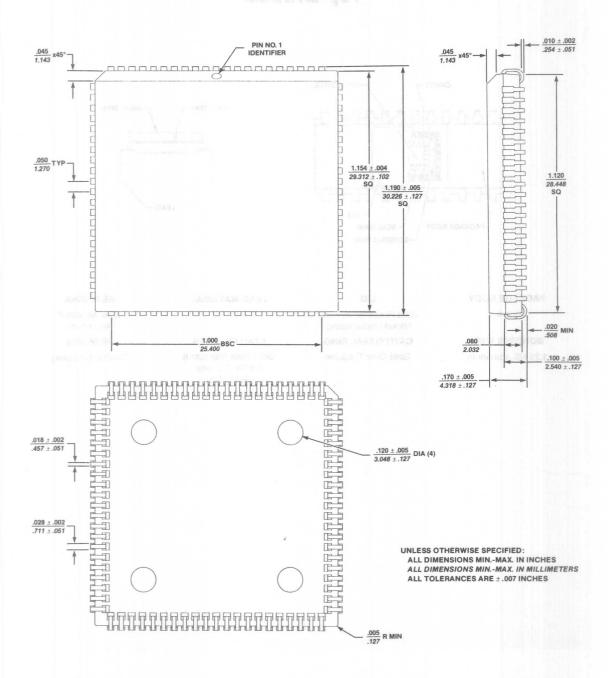


UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. TN INCHES
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE ± .007 INCHES

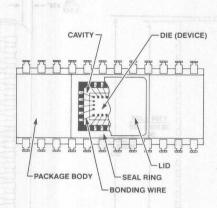
68NL Molded Chip Carrier (.950"x.950")

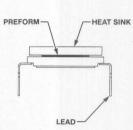


UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE ± .007 INCHES



Top Brazed





PACKAGE BODY

Alumina

BONDING WIRE

1.25 Mil Aluminum

LID

Gold Plated Kovar With Nickel Underplating

CAVITY/SEAL RING

Gold Over Tungsten

LEAD MATERIAL

Alloy 42

LEAD FINISHES

Gold Plate (Standard) Solder Dip Over Gold Plate HEAT SINK

Package Drawings

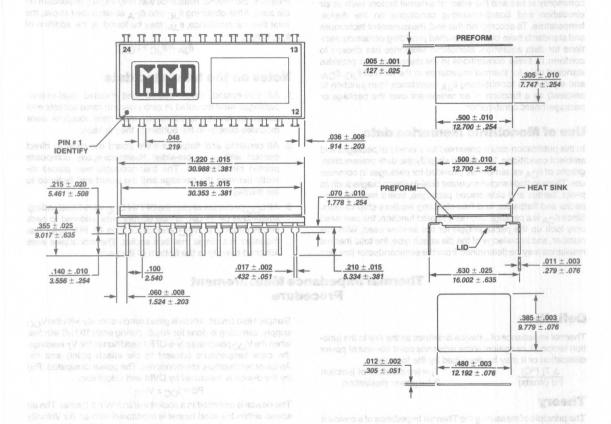
Blue Anodized Aluminum

PREFORM

Conductive Epoxy

24T Top Brazed Ceramic Dip and all sounds are of the sound and the sound (With Heat Sink) and a sound sound and the sound are sound as a sound

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UNLESS OTHERWISE SPECIFIED:
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ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE ± .007 INCHES

Power Dissipation Determination

Introduction

Thermal resistance for a packaged integrated circuit determines the operating temperature, and hence the performance and lifetime of the semiconductor device. For this reason, it is of interest to know the thermal impedance of the package configurations commonly in use and the effect of external factors such as air circulation and board-mounting conditions on the device temperature. To accomplish this end, measurement techniques and standards have been established providing certain conventions for data aquisition. Monolithic Memories has chosen to conform to these conventions in measurement and provides standard data for thermal impedance in the form of $\theta_{\rm JC}, \theta_{\rm CA}$, and a provision for obtaining $\theta_{\rm JA}$ (resistance from junction to ambient) as a function of air movement over the package or package/board combination.

Use of Monolithic Memories data

In this publication data is presented for a variety of packages and ambient conditions. In order to simplify the data presentation, graphs of θ_{CA} vs. airflow are provided for packages in common use. These include socket-mounted dual-in-line packages such as p-dip, cerdip, and side-brazed packages, board mounted cerpacks and flatpacks, and free-standing leadless-chip carriers. Since θ_{CA} is a package geometry related function, the user need only look up the package type for the air-flow used. With this number, and knowledge of the die attach type, the total thermal resistance may be determined from the semiconductor junction

to the ambient. Since the θ_{JC} is largely dependent on the package type and die attach type, a table has been constructed for easy use. (Although θ_{JC} is a die-size dependent variable for eutectic die attach, the effect of θ_{JC} on θ_{JA} is small enough that a constant may be used in most cases. For other die-attach methods, the thermal resistance was only slightly dependent on die size). After obtaining θ_{JC} and θ_{CA} as described above, the total thermal resistance, θ_{JA} , may be found by the addition of θ_{JC} to θ_{CA} as:

$\theta_{JA} = \theta_{JC} + \theta_{CA}$

Notes on the tabulated data

- All side-brazed, cerdip-sealed, and molded dual-in-line packages were mounted in zero insertion force sockets and placed transverse to the airstream. Thermocouples were mounted directly to the bottom of the package.
- All cerpacks and flatpacks were board mounted in direct contact with a double-sided fiberglass-epoxy composite printed circuit board. The thermocouple was placed directly between the package and the board and fastened to the package.
- All L_{CC} packages except the 84 PIN L_{CC} were freestanding, suspended by 28 GA. tinned copper wire soldered to pads corresponding to V_{CC} and GND. The 84 PIN L_{CC} was mounted in a single insertion socket. Thermocouples were attached directly to the bottom of the parts.

Thermal Impedance Measurement Procedure

Definition

Thermal impedance of a device is defined as the rise in the junction temperature against some reference point per unit of power dissipation or it may be described by the formula:

 Δ Tj (°C) Tj = temperature of junction Pd (Watts) Pd = power dissipation

Theory

The principle of measuring the Thermal Impedance of a device is based on measuring the temperature of the hottest junction on the die under power dissipation. This is done by using the substrate diode to monitor the chip temperature. By reverse biasing and forcing a small forward current (500 $\mu\text{A})$ through the device under test (between + V $_{\text{CC}}$ and ground), a large number of substrate diodes become forward-biased. By doing this, the hottest substrate diode junction is automatically detected, since it has the lowest voltage drop during this forward-biased condition. The forward voltage drop across the substrate diode is quite linear over a range of 25°C to 100°C. The hottest substrate diode is used as a "thermometer" to monitor the chip under power.

Procedure

A block diagram of the Thermal Impedance setup is shown in Figure 1. The substrate diode is forward biased by the Constant Current Source (–500 $\mu A)$. The V $_{CC}$ is supplied by the Power Supply, which is gated at 48.8 cycles/second, with a duty cycle of \simeq 99.5%. The V $_{F}$ of the substrate diode is 'sampled' by the

Sample/Hold circuit, which is gated synchronously with the V $_{CC}$ supply, sampling is done for 40 μS , during each 100 μS window when the V $_{CC}$ power supply is OFF. In addition to the V $_{F}$ readings, the case temperature (closest to die attach point) and the Ambient temperature are monitored. The power dissipated (Pd) by the device is measured by DVM and calculated:

The device is mounted in a socket within a Wind Tunnel. The air speed within the wind tunnel is monitored with an Air Velocity meter. The air speed is adjustable from 0 to 1000 feet/min. The use of a wind tunnel allows us to graph the temperature of the die, in relation to the cooling air speed. The worst case θ_{JA} is at 0 air speed (STATIC).

Summary

The Thermal Impedance measurement can be summarized as follows:

- 1). Calibration of the $\Delta V_F/^{\circ}C$ of the D.U.T. This is done by measuring the V_F at two different temperatures with the V_{CC} power supply OFF, and dividing the ΔV_F by the $\Delta^{\circ}C$.
- 2). Measurement of ΔV_F under operating conditions, under different air flow rates (0, 100, 500, 1000 ft/min.), while measuring °C case, °C ambient, I_{CC} and V_{CC}. The readings are recorded when the change in the case (°C case) temperature is less than 2% (of Δ °C case °C amb) over a time of 30 seconds.

3). Calculation of Thermal Impedance a) $\theta_{\rm JC}$ (Junction to case) Symbol of Definitions

V_{F1} = V_F @ low temp. cal. point (V_{CC} OFF)
V_{F2} = V_F @ high temp. cal. point (V_{CC} OFF)
°C₁ = Case °C @ low temp. cal. point (V_{CC} OFF)

°C₂ = Case °C @ high temp. cal. point (V_{CC} OFF)

V_{F3} = V_F under power, stablized

°C₃ = Case °C under power, stabilized

ord sort oc A = Ambient oc of other bus sort uge

s existed Pd = ICC x VCC starts no trabhas

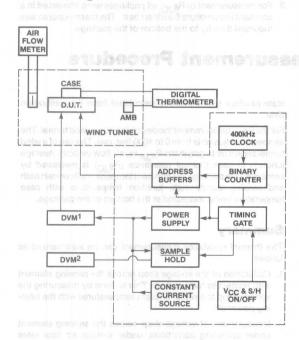
$$\theta_{JC} = \underbrace{\begin{bmatrix} (V_{F1} - V_{F3}) \\ (\overline{V_{F1} - V_{F2}}) \\ \overline{C_{2} - C_{1}} \end{bmatrix}}_{Pd} + (C_{1} - C_{3}) = \underbrace{C_{NN}}_{Pd}$$

b)
$$\theta_{CA} = \frac{({}^{\circ}C_{3} - {}^{\circ}C_{A})}{Pd}$$

c) θ_{JA} (Junction to ambient)

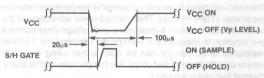
$$\theta_{JA} = \theta_{CA} + \theta_{JC} =$$
 °C/W

Block Diagram and fluorio bedning at



- 1). Digital Thermometer measures °C case and °C ambient
- 2). DVM:1 measures V_{CC} and I_{CC}
- 3). DVM² measures V_F of the substrate diode
- 4). BINARY counter creates A₀ thru A₁₁; $A_{\theta} = 100 \text{ kHz}, A_{1} = 50 \text{ kHz},$ A₂ = 25 kHz etc. synchronious.
- 5). Timing gate switches the power supply, address buffers, and sample/hold circuits.
- 6). Constant current source provides -500 μA to the V_{CC} pin for the V_F measurement.
- 7). The airflow meter measures the air velocity for airflow measurements.

F = 48.8 Hz DUTY CYCLE = 99.5%



introduction

Thermal resistance for a packaged integrated circuit determines the operating temperature and hence the performance and lifetime of the semiconductor device. For this reason, it is of interest to know the thermal resistance of the package configurations commonly in use and the effect of external factors such as air circulation and board-mounting conditions on the device temperature. To accomplish this end, measurement techniques and standards have been established providing certain conventions for data acquisition. Monolithic Memories has chosen to conform to these conventions in measurement and provides standard data for thermal resistance in the form of $R_{\theta JC}$ (resistance from junction to ambient) as a function of air movement over the package/board combination.

Use of Monolithic Memories Data

In this publication, data is presented for a variety of packages and ambient conditions. In order to simplify the data presentation, graphs of $R_{\theta,1\Delta}$ vs. airflow are provided for packages in

common use. I nese include socket-mounted pin grid arrays, dual-in-line p-dip, cerdip and side-brazed packages, board mounted cerpacks, flatpacks, leadless-chip carriers and plastic leaded chip carriers.

Resistance from junction to ambient $(R_{\theta,JA})$ is a package geometry and die size related function. The user need only look up the package type and die size for the air-flow used. Since the $R_{\theta,JC}$ is largely dependent on the package type and die size, a table has been constructed for easy use.

Notes on the Tabulated Data

- All side-brazed, cerdip-sealed, molded dual-in-line and pin grid array packages were mounted in zero insertion force sockets and transverse to the airstream.
- All cerpacks, flatpacks, LCC and PLCC packages were board mounted in direct contact with a double-sided fiberglassepoxy composite printed circuit board.
- For measurement of R_{θ JC}, all packages were immersed in a constant temperature fluorinert bath. The thermocouple was mounted directly to the bottom of the package.

Thermal Resistance Measurement Procedure

Definition

Thermal resistance of a semiconductor device is a measure of the ability of its mechanical structure (package) to provide for heat removal from the semiconductor element. It is defined as the rise in the junction temperature against some reference point per unit power of dissipation or it may be described by the formula:

$$R_{\theta JR} = \frac{T_{J} - T_{R}}{P}$$
 $R_{\theta JR} = \frac{T_{J} - T_{R}}{P}$
 $R_{JR} = \frac{T_{J} - T_{R}}{P}$
 $R_$

Thermal Measurement Technique

Thermal resistance is measured using the temperature sensitive parameter (TSP) method. This method takes advantage of the linear relation between temperature and voltage drop across a p-n junction to measure the average die temperature. Thermal resistance measurement can be done either using an actual device or with thermal test chips. For the purpose of this study, thermal test chips are used.

Each test chip consists of sensing elements and a heating element. Sensing elements are two sets of diode pairs. One diode pair is located at the center of each die and one pair is near a corner. The heating element is a polysilicon resistor which covers 95 percent of the die surface area. The resistor extends underneath the bond pads but not the sensing elements.

Initially, diodes are forward biased to a low level current source $(50~\mu\text{A})$ and the voltage drop is calibrated with respect to temperature. Then, the resistor is powered and the diode voltage drop is monitored until thermal equilibrium is reached. Steady

state junction temperature is calculated from the calibration data.

For the $R_{\theta JA}$ measurement the device is put in a wind tunnel. The air speed is adjustable from 0 to 1000 feet/min. The use of a wind tunnel allows us to graph the $R_{\theta JA}$ vs. air flow velocity. Average junction to case thermal resistance ($R_{\theta JC}$) is measured by immersing the package in a constant temperature fluorinert bath and sensing steady state junction temperature with case temperature being measured at the bottom of the package.

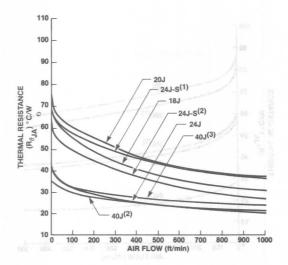
Summary

The thermal resistance measurement can be summarized as follows:

- Calibration of the voltage drop across the sensing element with respect to temperature. This is done by measuring the voltage drop at several different temperatures with the heating power off.
- 2. Measurement of voltage drop across the sensing element under operating conditions, under various air flow rates (from 0 to 1000 linear ft/min.), while measuring °C ambient and power input for calculation of $R_{\theta,IA}$.
- 3. Measurement of voltage drop across the sensing element under operating conditions, package immersed in constant temperature fluorinert bath, while measuring the case temperature at the bottom of the package and power input for calculation of R $_{ heta$ JC</sub>. The readings are recorded when the package has reached thermal equilibrium.
- Calculation of thermal resistance

a.
$$R_{\theta JA} = \frac{T_{J} - T_{A}}{P}$$
 b. $R_{\theta JC} = \frac{T_{J} - T_{C}}{P}$

Cerdip (J) Packages



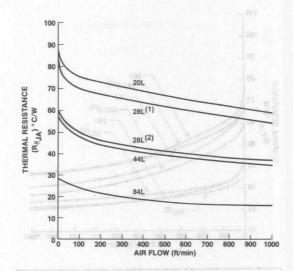
PACKAGE	DIE SIZE (mils) ²	R _d JC (°C/WATT)	
18J	22,500	6	
20J	5,625	14	
24J-S(1)	5,625	16	
24J-S(2)	11,250	9	
24J	50,625	3	
40J(3)	22,500	4	
40J(2)	50,625	2	

^{*} These are typical values for the given die size.

Other die size values to be supplied in the future.

Most Monolithic Memories products will be slightly lower.

Leadless Chip Carriers (L) Packages



	100000	1361	
PACKAGE	DIE SIZE (mils) ²	Rajc (°C/WATT)	
20L	5,625	(116,59	
28L(1)	5,625	20	
28L(2)	22,500	9	
44L	22,500	4	
84L†	50,625	(\$4.05	

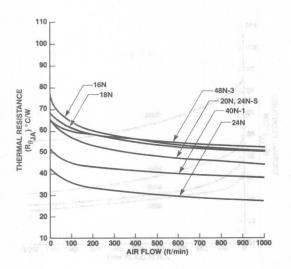
^{*} These are typical values for the given die size.

Other die size values to be supplied in the future.

Most Monolithic Memories products will be slightly lower.

[†] Cavity up.

Molded Dip (N) Packages



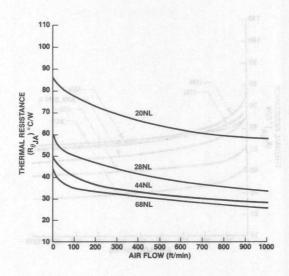
PACKAGE	DIE SIZE (mils) ²	R _θ JC (°C/WATT)	
16N	5,625	29	
18N	5,625	30	
20N	5,625	23	
24N	50,625	10	
24N-S	5,625	22	
40N-1	22,500	16	
40N-3	5,625	23	

^{*} These are typical values for the given die size.

Other die size values to be supplied in the future.

Most Monolithic Memories products will be slightly lower.

Plastic Leaded Chip Carrier (NL) Packages

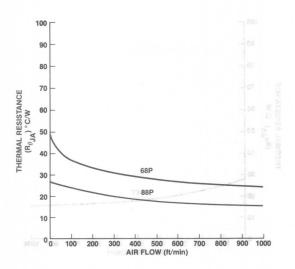


PACKAGE	DIE SIZE (mils) ²	R#JC (°C/WATT)
20NL	5,625	35
28NL	22,500	16
44NL	22,500	13
68NL	50,625	8

 ^{*} These are typical values for the given die size.
 Other die size values to be supplied in the future.

Most Monolithic Memories products will be slightly lower.

Pin Grid Array (P) Packages



PACKAGE	DIE SIZE (mils) ²	R#JC (° C/WATT)
88P†	50,625	4
68P	22,500	5

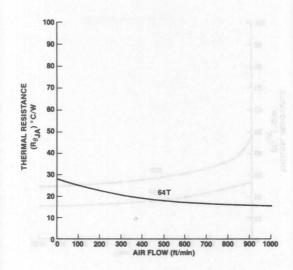
^{*} These are typical values for the given die size. I maint included on seed?

Other die size values to be supplied in the future.

Most Monolithic Memories products will be slightly lower. Modelligrad Management

† Cavity up.

Top Brazed (T) Ceramic Package

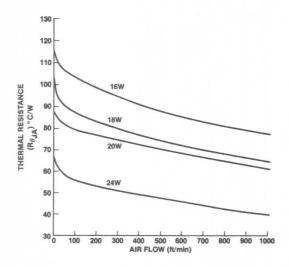


PACKAGE	DIE SIZE (mils) ²	R*JC (°C/WATT)
64T	50,625	3

^{*} These are typical values for the given die size.
Other die size values to be supplied in the future.

Most Monolithic Memories products will be slightly lower.

Cerpack (W) Packages

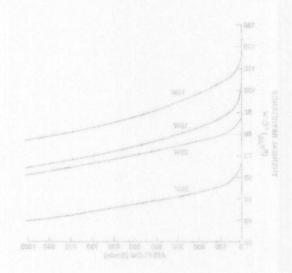


PACKAGE	DIE SIZE (mils) ²	R*JC (°C/WATT)
16W	5,625	21
18W	5,625	17
20W	5,625	15
24W	22,500	4

^{*} These are typical values for the given die size.
Other die size values to be supplied in the future.
Most Monolithic Memories products will be slightly lower.



Carpack (W) Packages



Råjc (°C/WATT	PACKAGE
21	tew
	WOS

